330mW AC or DC Tiny Flyback Converter Power Supply

National Semiconductor
RD-187
PowerWise® Design Lab Europe
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Introduction

This application note describes the design of a tiny Flyback power supply.

It's main purpose is to convert the rectified AC or DC Input to DC regulated output voltage. The power supply provides protection for this supply voltage, isolates the rest of the network from the output, limits the transient input voltage and protects against inrush current at plug in. The board fully complies to the EN55022 norm (Conductive average) and international safety standards. The secondary side is regulated at 3.3V. The controller is switching with a fixed frequency of 250 kHz. The heart of the power supply is the controller LM3481 current mode PWM from National Semiconductor.

The advantage of the proposed solution is using a standard off the shelf transformer, small solution size and high ambient operating temperature up to 85°C (105°C possible).

Based on the presented solution higher output power up to several Watt can also be achieved using the LM3481.

Features

The LM3481 integrates many features to simplify the Flyback converter implementation:

- Hysteretic under-voltage shutdown protects the power stage from excessive stress if the input voltage is below the required minimum operating level.
- Current mode control allows for simple type 2 control and protects the power MOSFET from over-current
- Integrated 1A capable gate drive to provide rapid switching of the power MOSFET.
- Internal soft start
- Pulse skipping at light load

Operating Conditions

Input:

- V_{IN} (DC) = 8.9V to 40V
- V_{IN} (AC) = $24V_{AC}$

Output: $330mW_{OUT}$ = 3.3V ±3%

- I_{OUT} = 0.1A

Simplified Schematic (Block Diagram)

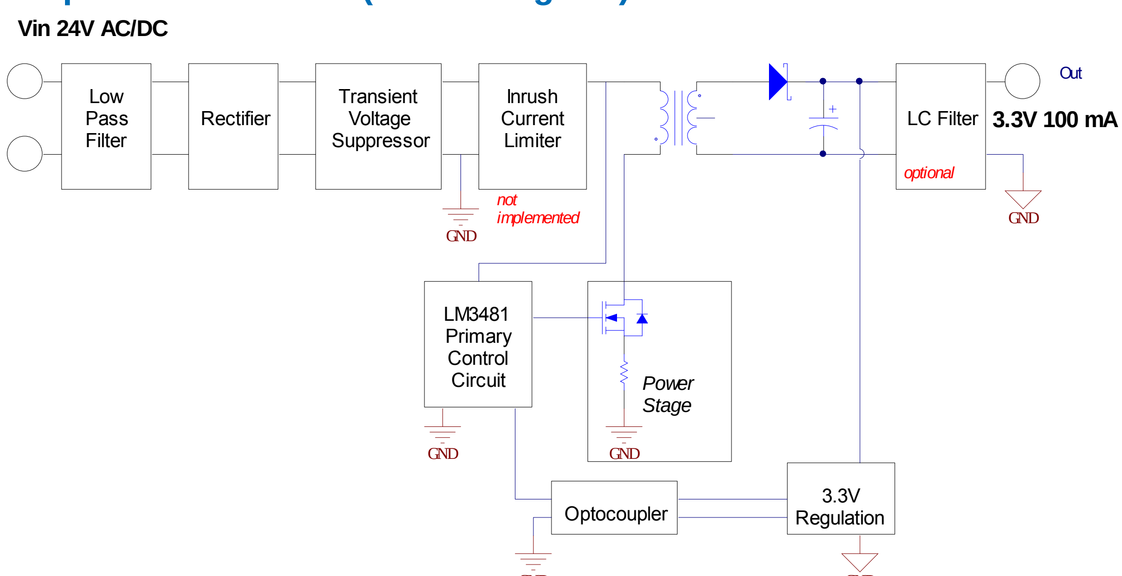


FIGURE 1. Block Diagram

Complete Schematic

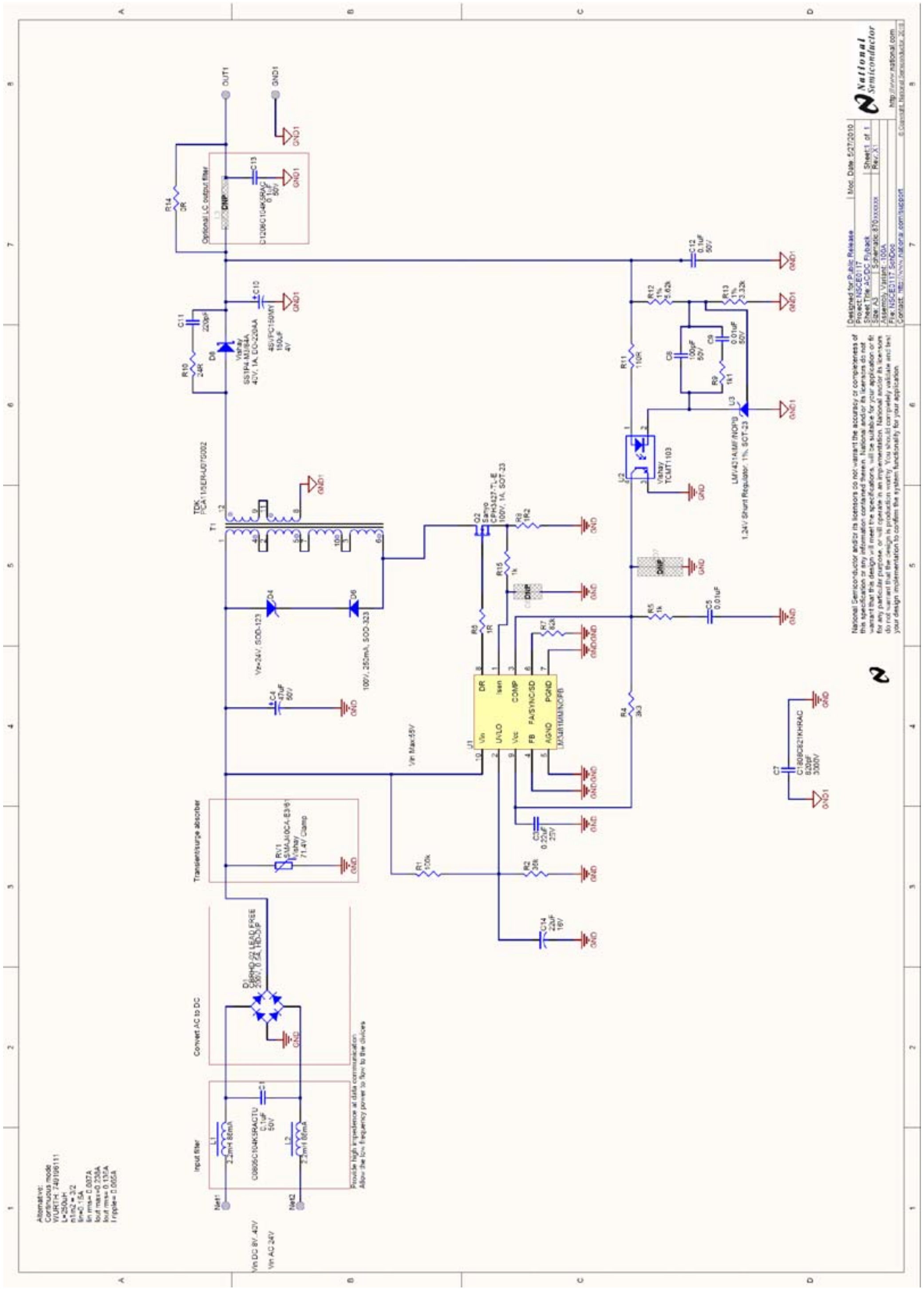


FIGURE 2. Complete Schematic

Bill of Material

Designator	Description	Manufacturer	Part Number	RoHS
C1	CAP, CERM, 0.1uF, 50V, 10%, X7R, 0805	Kemet	C0805C104K5RACTU	Y
C3	CAP, CERM, 0.22uF, 25V, 10%, X7R, 0805	Kemet	C0805C224K3RACTU	Y
C4	CAP, AL, 47uF, 50V, +/-20%, 0.68 ohm, SMD	Panasonic	EEEFK1H470P	Y
C5, C9	CAP, CERM, 0.01uF, 50V, 10%, X7R, 0603	Kemet	C0603C103K5RACTU	Y
C7	CAP, CERM, 820pF, 3000V, 10%, X7R, 1808	Kemet	C1808C821KHRAC	Y
C8	CAP, CERM, 100pF, 50V, 5%, C0G/NP0, 0603	Kemet	C0603C101J5GAC	Y
C10	CAP, Conductive Polymer, 150uF, 4V , 20%, SMD	Sanyo	4SVPC150MY	Y
C11	CAP, CERM, 220pF, 100V, 5%, C0G/NP0, 0805	Kemet	C0805C221J1GAC	Y
C12	CAP, CERM, 0.1uF, 50V, 10%, X7R, 0603	Kemet	C0805C104K5RAC	Y
C13	CAP, CERM, 0.1uF, 50V, 10%, X7R, 1206	Kemet	C1206C104K5RAC	Y
C14	CAP, CERM, 22uF, 16V, 10%, X5R, 1210	Kemet	C1210C226K4PAC	Y
D1	Diode, Switching-Bridge, 200V, 0.5A, HD-DIP	Central Semiconductor	CBRHD-02 LEAD FREE	Y
D4	Diode, Zener, 24V, SOD-123	Central Semiconductor	CMHZ4709 LEAD FREE	Y
D6	Diode, High Speed Switching, 100V, 250mA, SOD-323	Central Semiconductor	CMDD4448 LEAD FREE	Y
D8	Diode, Schottky, 40V, 1A, DO-220AA/SMP	Vishay	SS1P4-M3/84A	Y
L1, L2	Inductor, Shielded Drum Core, Ferrite, 2.2mH, 0.11A, 6.4 ohm, SMD	Coilcraft	LPS6235-225MLB	Y
Q2	MOSFET, N-CH, 100V, 1A, SOT-23	Sanyo	CPH3427-TL-E	Y
R1	RES, 100k, 5%, 0603	Not Specified	Not Specified	Opt
R2	RES, 36k, 5%, 0603	Not Specified	Not Specified	Opt
R4	RES, 3k3, 5%, 0603	Not Specified	Not Specified	Opt
R5, R15	RES, 1k, 5%, 0603	Not Specified	Not Specified	Opt
R6	RES, 1R, 5%, 0603	Not Specified	Not Specified	Opt
R7	RES, 82k, 5%, 0603	Not Specified	Not Specified	Opt
R8	RES, 1R2, 5%, 0805	Not Specified	Not Specified	Opt
R9	RES, 1k1, 5%, 0603	Not Specified	Not Specified	Opt
R10	RES, 24R, 5%, 1206	Not Specified	Not Specified	Opt
R11	RES, 110R, 5%, 0603	Not Specified	Not Specified	Opt
R12	RES, 5.62k, 1%, 0603	Not Specified	Not Specified	Opt
R13	RES, 3.32k, 1%, 0603	Not Specified	Not Specified	Opt
R14	RES, 0R, 5%, 0603	Not Specified	Not Specified	Opt
RV1	Transient Suppressor, 71.4V, SMA	Vishay	SMAJ40CA-E3/61	Y
T1	Transformer	TDK	PCA11/5ER-U07S002	?
U1	High Efficiency Low-Side N-Channel Controller for Switching Regulators	National Semiconductor	LM3481MM/NOPB	Y
U2	Optocoupler, CTR 100% to 200%	Vishay	TCMT1103	Y
U3	1.24V Shunt Regulator, 1%, SOT-23	National Semiconductor	LMV431AIMF/NOPB	Y

TABLE 1. Bill of Material

Theory of Operation

Flyback Converter Theory

The basic flyback converter circuit is shown in FIGURE 3. The power transistor TP operates as a switch, which is alternately closed (i.e. the transistor TP conducts in a saturated state) and opened (i.e. the transistor TP is off). The secondary winding of the transformer is phased so that the diode DS is reverse biased, when the power transistor TP is closed. The Figure shows the theoretical waveforms of current and voltage at various points in the circuit under steady state operating conditions. When the power transistor TP conducts, the input supply VIN is applied across the primary winding of the transformer and the diode DS is non-conducting. Current rises linearly in the primary winding until the transistor is switched off:

$$Vp = Lp\frac{dic}{dt} \quad \text{or} \quad \frac{dic}{dt} = \frac{Vp}{Lp}$$

Where:

- Vp = Voltage across the primary winding
- Lp = Primary inductance of the transformer
- Ic = Collector current of the power transistor

$$Ic = \int_0^{ton} Vp.dt = \frac{Vin}{Lp}.t$$

At the end of the conduction time t on, the collector current reaches the value defined I C given by:

$$W = \frac{Vin}{Lp}ton$$

This results in an energy transfer from the input supply to the primary inductance of the transformer:

$$W = \frac{1}{2}Lp(Ic)^2 \frac{Vin^2 * ton^2}{2Lp}$$

When the transistor TP turns off, the collector current I_C falls rapidly to zero. The energy W stored in the primary inductance of the SMT makes the voltage across the primary and secondary windings reverse in polarity. These reverse voltages increase rapidly until the voltage across the secondary winding exceeds the voltage across the output capacitor CS. The diode DS starts to conduct and to transfer the energy, which were stored in the primary inductance to the output capacitor CS and the load RL.

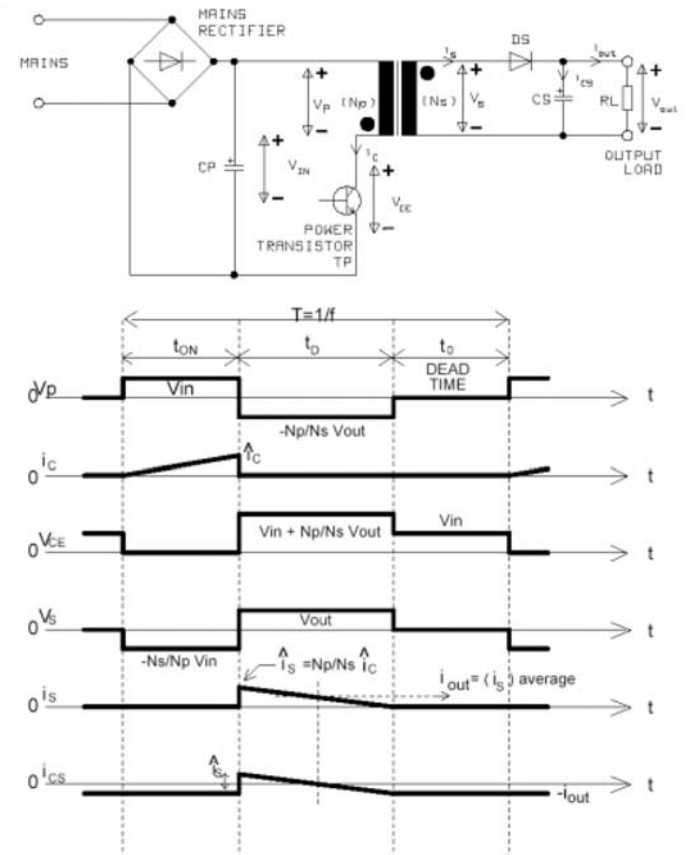


FIGURE 3. Flyback converter theory

When the energy transfer is finished, the voltages V_P and V_s quickly fall to zero and the voltage V_{CE} to V_{IN}. They remain at these respective values for the remainder of the period. The diode DS is off. After a dead time t0, the power transistor TP switches on again and cycle repeats. During the dead time t0 and the conduction period t_{ON} of the power transistor, the load is supplied only by energy stored in the output capacitor CS which holds the output voltage V_{OUT} substantially constant over every cycle.

The term “discontinuous mode” refers to the fact that the current through the primary inductance goes to zero before the start of the next cycle. The power delivered by the input supply is V in to the primary winding is given by:

$$Pin = \frac{W}{T}$$

Where T is the period of operation that is:

$$Pin = \frac{Vin^2 * ton^2}{2LpT}$$

The power delivered to the output load is:

$$Pout = \frac{Vout^2}{Rl}$$

The relationship between Pin and Pout is:

$$Pout = \delta * Pin$$

Where is the efficiency of the power conversion between the input supply Vin and the output load RL. Therefore:

$$\frac{Vout^2}{RL} = \delta \frac{Vin^2 * ton^2}{2LpT} ton$$

$$\triangleright Vout^2 = \delta \frac{Vin^2 * ton^2}{2LpT} ton * RL$$

$$\triangleright Vout = ton * Vin * \sqrt{\frac{\delta RL}{2LpT}}$$

This relationship shows that the output voltage can be stabilized against variations in the input voltage V_{in} or the load RL by varying the on-time of the power transistor (or duty cycle since the period T is supposed to be constant).

Board Photos

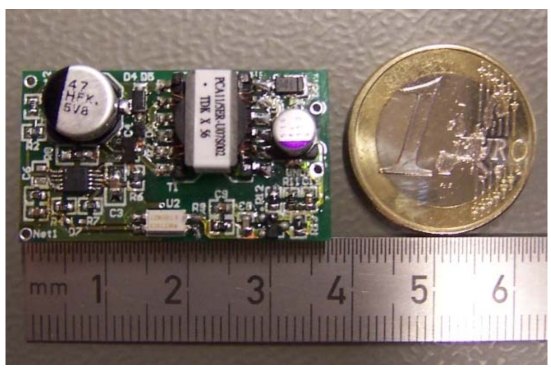


FIGURE 4. Photos of the Board

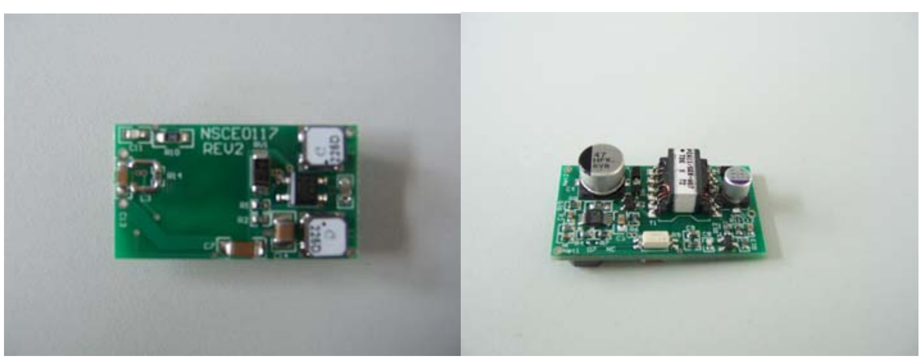


FIGURE 5. Photos of the Board

Specifications

Specification	Model	
	Max output power (W)	**0.3W**
	DC Output	**3.3V**
Input	Voltage (DC)	**8.9V$_{DC}$ to 40V$_{DC}$**
	Voltage (AC)	**24V$_{AC}$**
	Efficiency (%)	**63%**
Switching frequency	(Hz)	**250K**
Output	Voltage (V)	**3.3V +/-3%**
	Current (A)	**0.1A**
	Ripple (mV$_{pp}$)	**32mV**
	Ripple (mV$_{pp}$) (20MHz bandwidth)	**18.8mV**
	start up time (ms)	**50ms (V$_{IN}$=8.5V$_{DC}$, I$_{out}$=100%)**
	Hold up time (input failure)	**128ms @ 100% load**
	Remote sensing	**No**
	Remote on/off	**No**
Isolation	Input/output	**500V$_{DC}$**
Safety	Agency approvals	**None**
EMI	EN55022 Conductive average	**Yes**
Other	cooling method	**None**
	Ambient temperature range	**-40°C to +85°C**

Note 1 Maximum component height is 11mm. The over all size area is 20mm* 36.5mm.

Waveforms

All measurements have been done ensuring the shortest as possible probe connection (Figure 6).

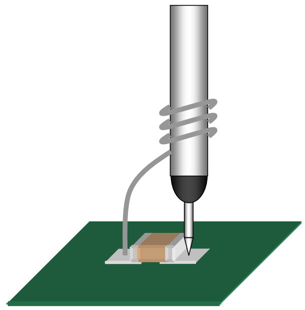


FIGURE 6. Short Probe Connection

Plug in into the supply line

At plug in, the input voltage charges the input capacitor with a low peak current due to the DCR of the input filter.

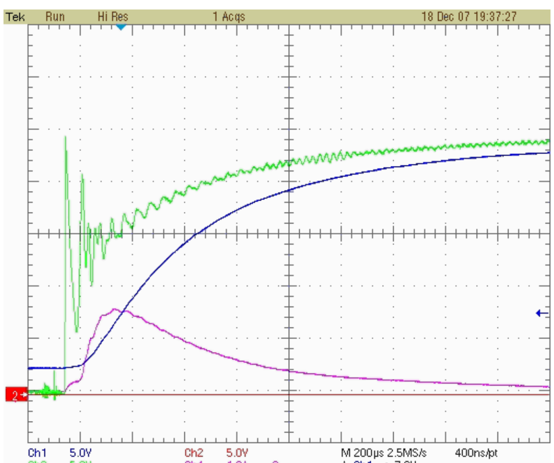


FIGURE 7

CH1: V_{IN} (pin 10)
CH3: input Voltage
CH4: input Current

Vin: 24VDC
Vout: **3.3V@0.1A**
Measurement done at hot plug in
Max peak current: 1.68A

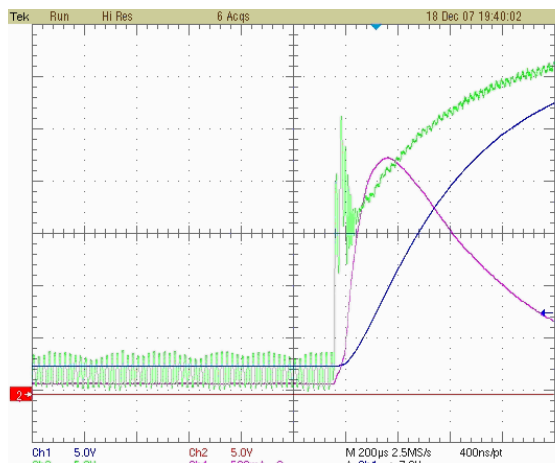


FIGURE 8

CH1: V_{IN} (pin 10)
CH3: input Voltage
CH4: input Current

Vin: 24VAC
Vout: **3.3V@0.1A**
Measurement done at hot plug in
Max peak current: 2.3A

Start-Up Phase

As soon as the voltage on the pin 2 reaches the upper voltage threshold of the UVLO logic, the device turns into active mode and start switching smoothly due to the internal soft start.
The following plot shows the voltage on the Vcc pin of the LM3481 during start up phase. It can be seen from the plots that it takes approx. 3.24ms for the power supply to regulate.

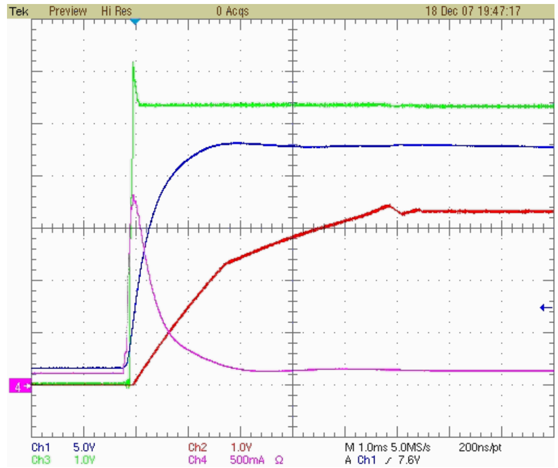


FIGURE 9

CH1:	V_{IN} (pin 10)	**Vin:**	**24V$_{DC}$**
CH2:	V_{OUT}	**Vout:**	**3.3V@0.1A**
CH3:	V_{CC} (pin 9)	Measurement done at plug in	
CH4:	input Current	Start up time: 3.24 ms	

Time delay after plug in

To avoid disturbing the line during plug in the power supply should wait at least this minimum time before starting the DC/DC converters. This is to ensure that all of the input storage capacitors have charged up to the full available source power supply voltage before starting up. This is done by adding a capacitor C14 on the UVLO pin. The following plots show the timing between the plug in and the 3.3V output at full load with Vin min and max.

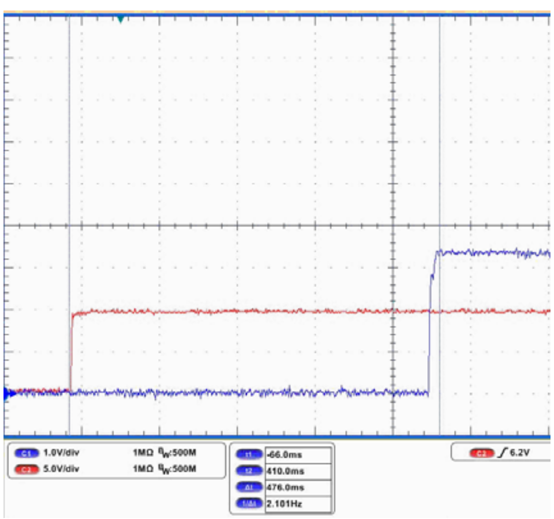


FIGURE 60

CH2:	V_{IN} (pin 10)	**Vin:**	**8.5V$_{DC}$**
CH1:	V_{OUT}	**Vout:**	**3.3V@0.1A**
		Measurement done at plug in	
		Delay time: 476 ms	

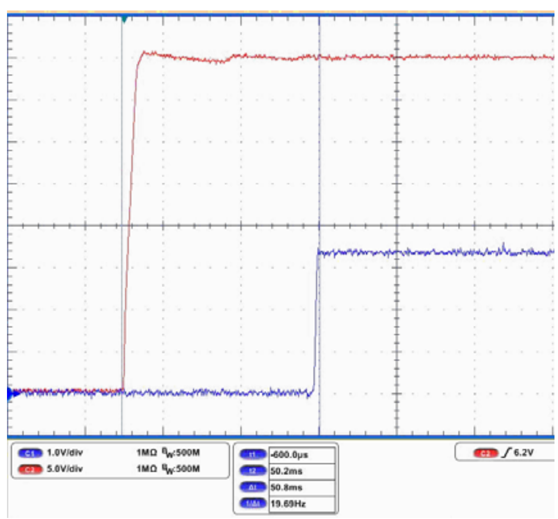


FIGURE 7

CH2:	V_{IN} (pin 10)	**Vin:**	**40V$_{DC}$**
CH1:	V_{OUT}	**Vout:**	**3.3V@0.1A**
		Measurement done at plug in	
		Delay time: 50 ms	

One Complete Cycle

This plot shows in detail the drain-source voltage and drain current of Q2 for one complete cycle in on mode. The cycle can be divided into different phases as shown on the plot of FIGURE 8FIGURE 8:

- (1) Switch on phase
- (2) Conducting phase
- (3) Switch off phase
- (4) Off phase which can be subdivided into
  - (5) Energy transfer phase
  - (6) Dead time

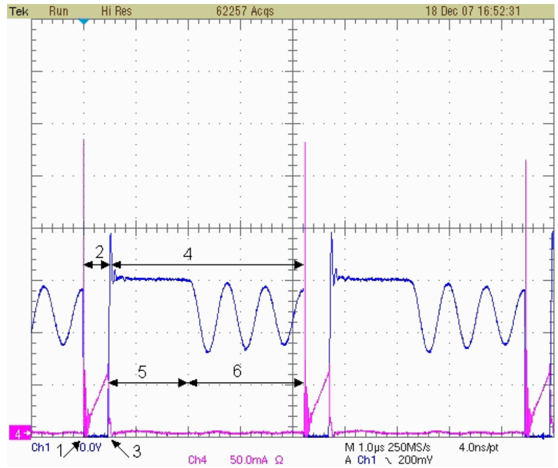


FIGURE 8

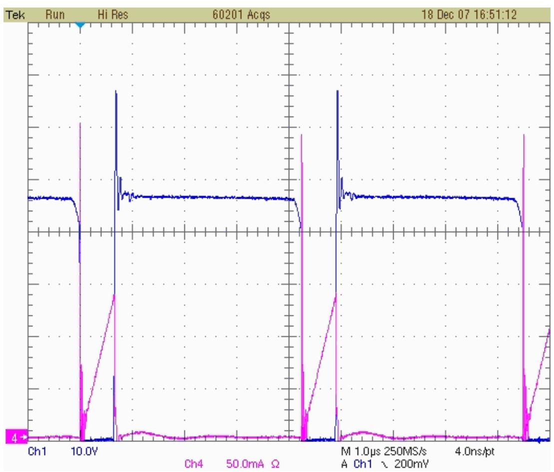


FIGURE 13. One complete cycle: $V_{IN\ max}$ with $I_{OUT\ max}$

CH1:	V_D Q2	**Vin:**	**40V_{DC}**
CH4:	I_D Q2	**Vout:**	**3.3V@0.1A**
		Result: Edge of continuous mode	

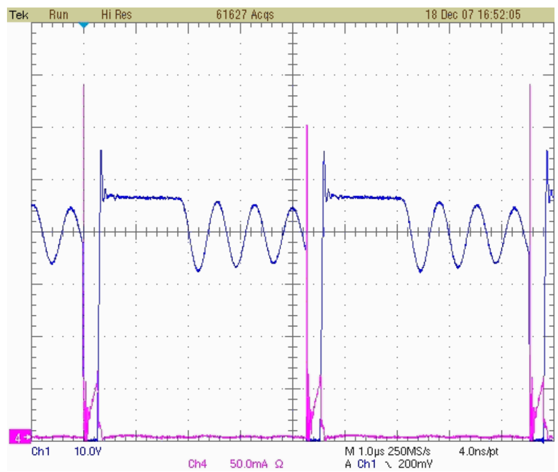


FIGURE 14. One complete cycle: $V_{IN\ max}$ with $I_{OUT\ min}$

CH1:	V_D Q2	**Vin:**	**40V_{DC}**
CH4:	I_D Q2	**Vout:**	**3.3V@15mA**
		Result: Discontinuous mode	

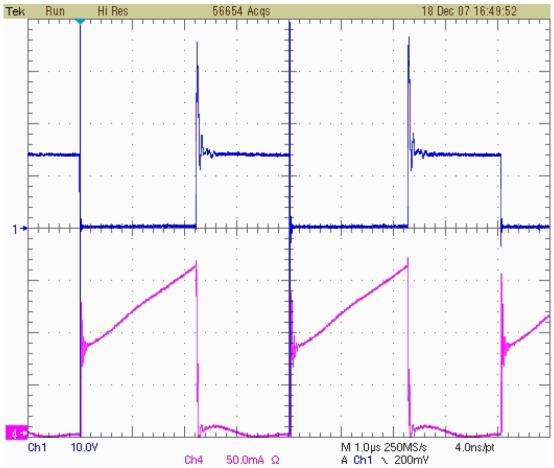


FIGURE 95 One complete cycle: $V_{IN\ min}$ with $I_{OUT\ max}$

CH1: V_D Q2
CH4: I_D Q2
NO INPUT FILTER

Vin: **$8V_{DC}$**
Vout: **3.3V@0.1A**
Result: continuous mode

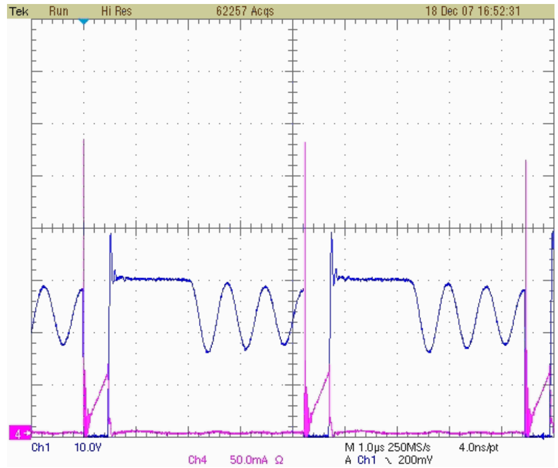


FIGURE 107. Output regulation: Minimum load at $24V_{in\ DC}$

CH1: V_D Q2
CH4: I_D Q2
NO INPUT FILTER

Vin: **$24V_{DC}$**
Vout: **3.3V@15mA**
Result: discontinuous mode

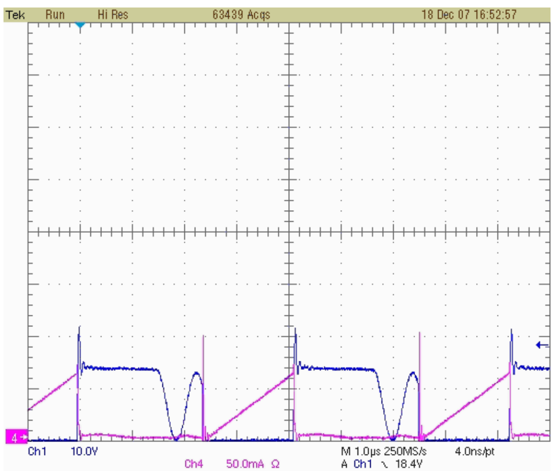


FIGURE 16. One complete cycle: $V_{IN\ min}$ with $I_{OUT\ min}$

CH1: V_D Q2
CH4: I_D Q2
NO INPUT FILTER

Vin: **$8V_{DC}$**
Vout: **3.3V@15mA**
Result: Discontinuous mode

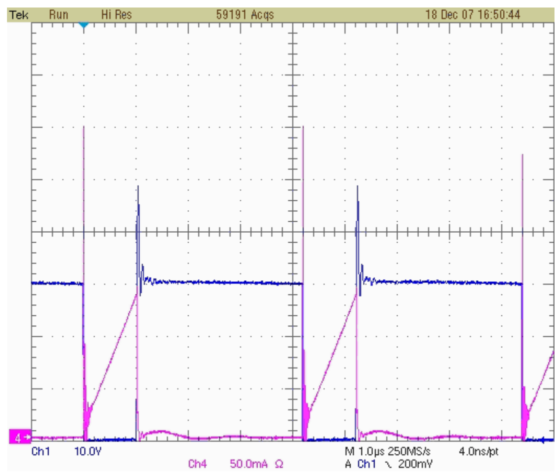


FIGURE 118. Output regulation: Maximum load at $24V_{in\ DC}$

CH1: V_D Q2
CH4: I_D Q2
NO INPUT FILTER

Vin: **$24V_{DC}$**
Vout: **3.3V@0.1A**
Result: continuous mode

Fold back point

The fold back point is where the load on the output of the power supply is increased until the Power supply can no longer regulate and the voltage starts to fall. The reason is that the drain current of Q2 is so large that the current limit threshold is reached. This effectively limits the energy that can be stored in the transformer T1 and hence the energy that can be transferred to the secondary side. The fold back point is effectively a measure of the max output power of the power supply and represents the worst case load on the power supply. The next 2 plots show the output voltage and the switching node under the condition of minimum and maximum input voltage.

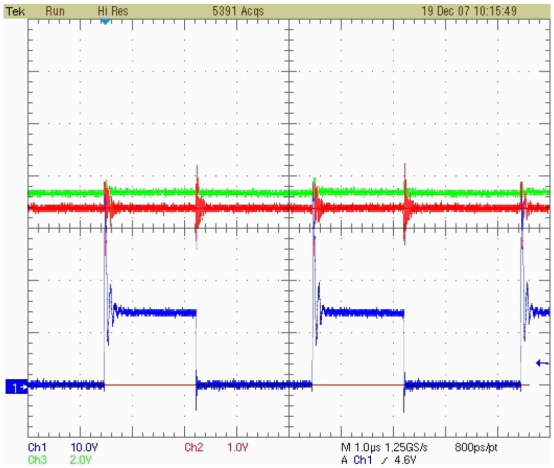


FIGURE 12. Maximum output current at minimum input voltage

CH1: V_D Q2
CH2: V_{OUT}
CH3: V_{IN} pin
Increasing output current

Vin: **8V$_{DC}$**
Vout: **3.3V**
Result: Max output current before the V_{OUT} drops: **115mA**

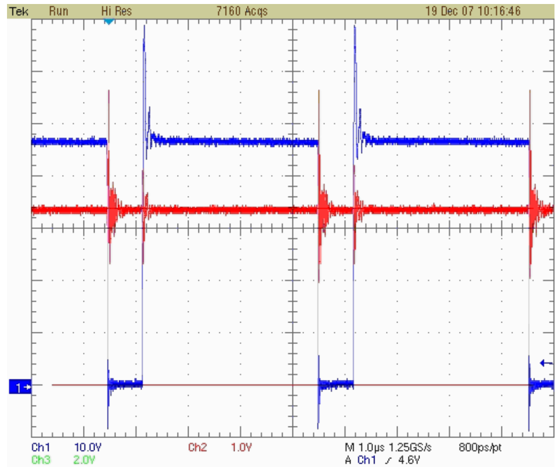


FIGURE 20, Maximum output current at maximum input voltage

CH1: V_D Q2
CH2: V_{OUT}
Increasing output current

Vin: **40V$_{DC}$**
Vout: **3.3V**
Result: Max output current before the V_{OUT} drops: **295mA**

Protection

Primary protection

The primary side inherits a cycle by cycle current limitation, which means that the maximum transferable power is limited and the secondary voltage will drop down if this limit will be reached. The resistors R8 provides a proportional voltage to the drain current and is used for the current sense input pin 1 of the LM3481. If the voltage at R8 becomes high enough the PWM of U1 uses this information to terminate the output switch conduction. The typical I_sense signal is 0.16V.

Secondary protection: short circuit

For safety reasons and to fulfill short circuit requirements, it has been ensured that no component can overheat and burn in case of short circuit. At short circuit the power supply reaches the fold back point and provides a defined maximum current. So the power supply cannot be damaged. As soon as the short circuit is removed from the output, the power supply will go back to the regulated voltage 3.3V.

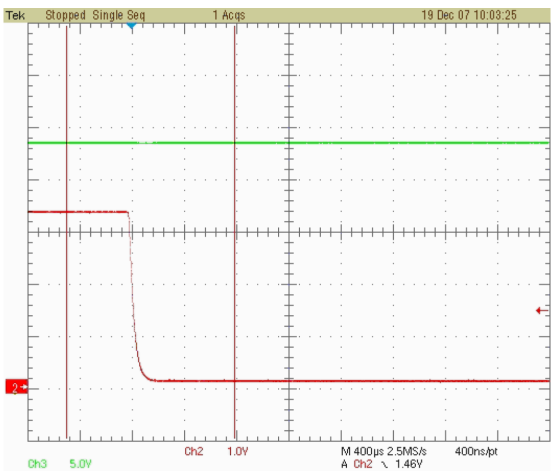


FIGURE 21, Typical protection after short circuit of the 3.3V

CH2: V_{OUT} **Vin:** **$24V_{DC}$**
CH3: V_{IN} pin
Short Circuit

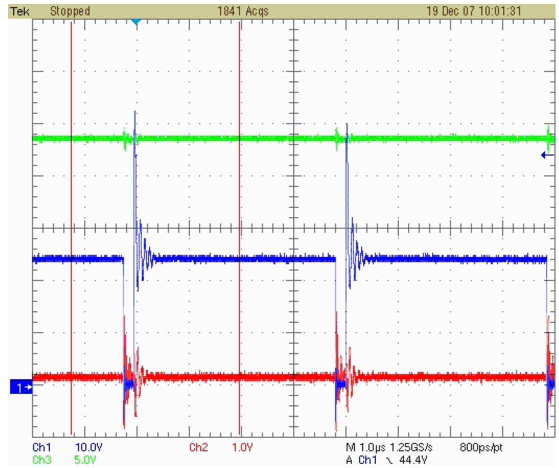


FIGURE 22, Typical protection after short circuit of the 3.3V

CH1: V_D Q2 **Vin:** **$24V_{DC}$**
CH2: V_{OUT}
CH3: V_{IN} pin
Short Circuit

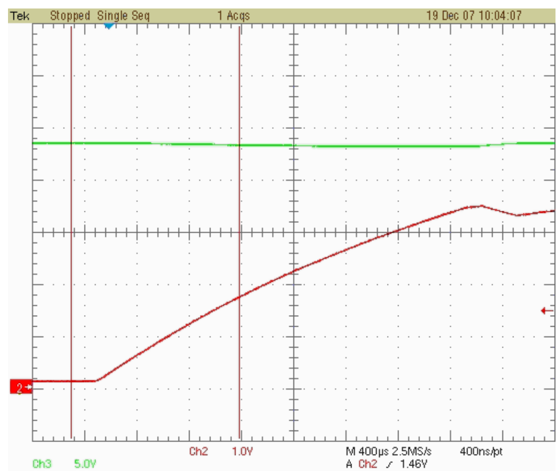


FIGURE 23, Start up phase after that the short circuit is removed

CH2: V_{OUT} **Vin:** **$24V_{DC}$**
CH3: V_{IN} pin
Short Circuit removed

Secondary protection: Over Voltage

If there is an open loop failure of the PWM regulation, the 3.3V output increases and the voltage on the comp pin 3 becomes higher and switches off the Mosfet. As the internal over voltage protection is disabled due to the pin VFB connected to ground, the output voltage will increase. At 100mA output, the output voltage reaches a maximum of 6.3V. To avoid this behavior a 3.9V zener diode 500mW can be connected in parallel to the output.

Efficiency

The following pictures show the efficiency for different input configurations.

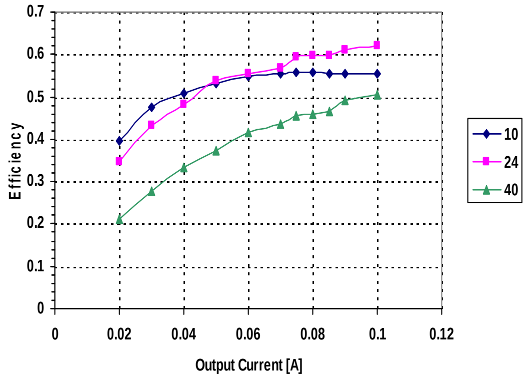


FIGURE 13, Efficiency of the complete board including the input filter at Vin=10V,24V,40V

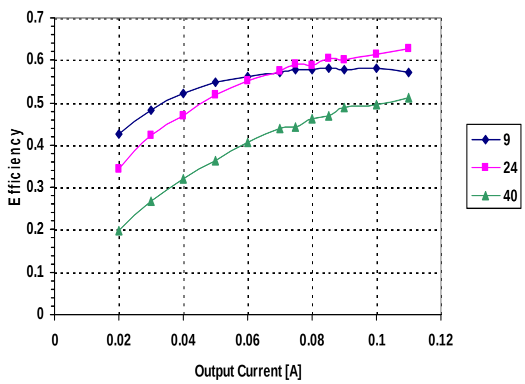


FIGURE 14, Efficiency of the complete board without the input filter at Vin=9V,24V,40V

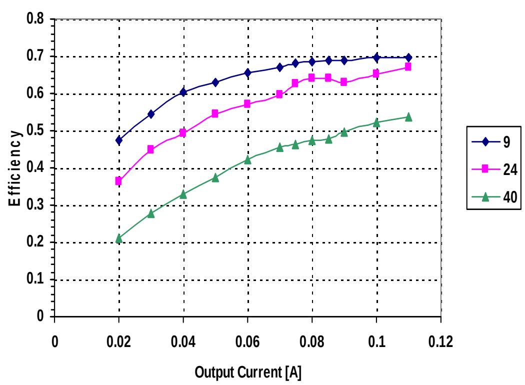


FIGURE 156, Efficiency of the DC/DC part: no input filter and no bridge

Ripple

The optional output LC filter is not needed due to the low output ripple.

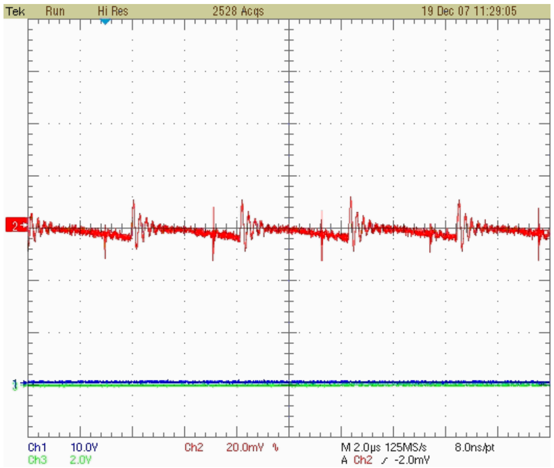


FIGURE 27, Output Ripple

CH2: V_{OUT} (AC)
Vin: 24Vdc

V_{OUT} = 24mVpp
Full bandwidth

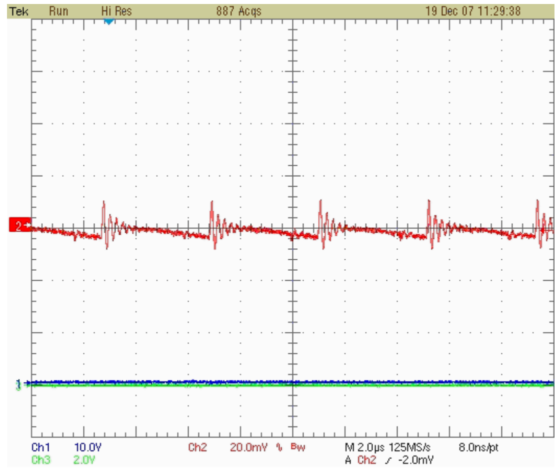


FIGURE 28, Output Ripple

CH2: V_{OUT} (AC)
Vin: 24Vdc

V_{OUT} = 18mVpp
20MHz Bandwidth

Snubber Network

In switched mode power supplies, there is a high dV/dt across the FET when it switches off. This is caused by abruptly cutting off the current through the primary inductance of the transformer. This high dV/dt is undesirable for a number of reasons:

- High switching losses in the FET
- Cause EMI Emission
- High output ripple

This high dV/dt can be reduced by a clamp network. There is a clamp network on the primary side with a zener diode D5 and also a snubber across the secondary diode D8.
The following plots show the voltage on the anode of this diode with and without snubber network.

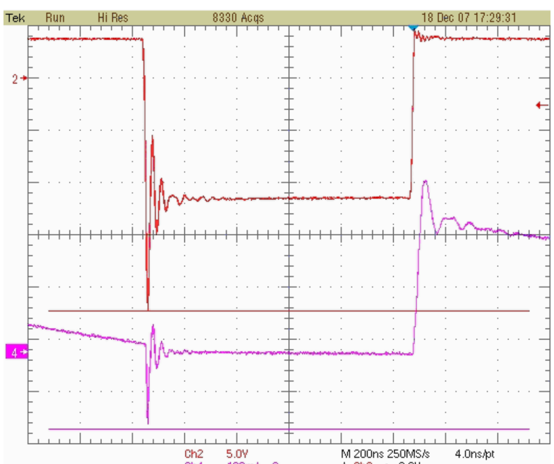


FIGURE 29, Switching Noise

CH2: V_{ANODE} DS
CH4: I_{DS}

V_{in}= 24V
V_{OUT}=3.3V@0.1A
NO Snubber

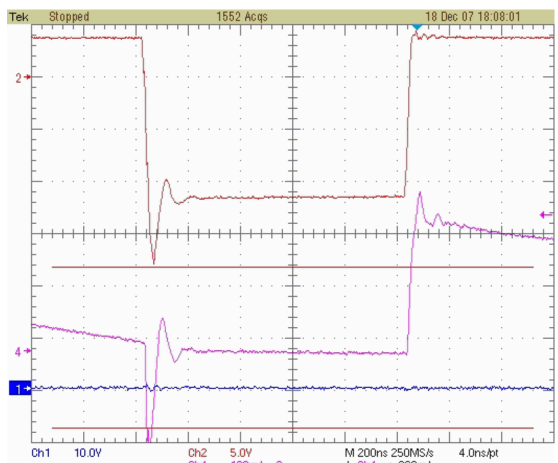


FIGURE 30, Switching Noise

CH2: V_{ANODE} DS
CH4: I_{DS}

V_{in}= 24V
V_{OUT}=3.3V@0.1A
WITH Snubber

Thermal Behavior

Functional tests to ensure full reliability have been done with DC input voltage from 8.9V to 40V with an output current of 100mA over an ambient temperature range from -40°C to +85°C.

Transient Measurement

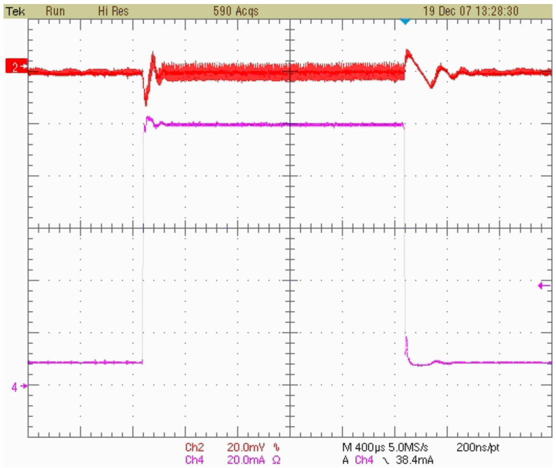


FIGURE 16, Load Transient

The pk to pk voltage on the output 3V3 is 22Mv.

CH2:	V_{OUT} (AC)	**I_{OUT} transition from**
CH4:	I_{OUT}	**10mA to 100mA**

Frequency Domain Analysis (Stability)

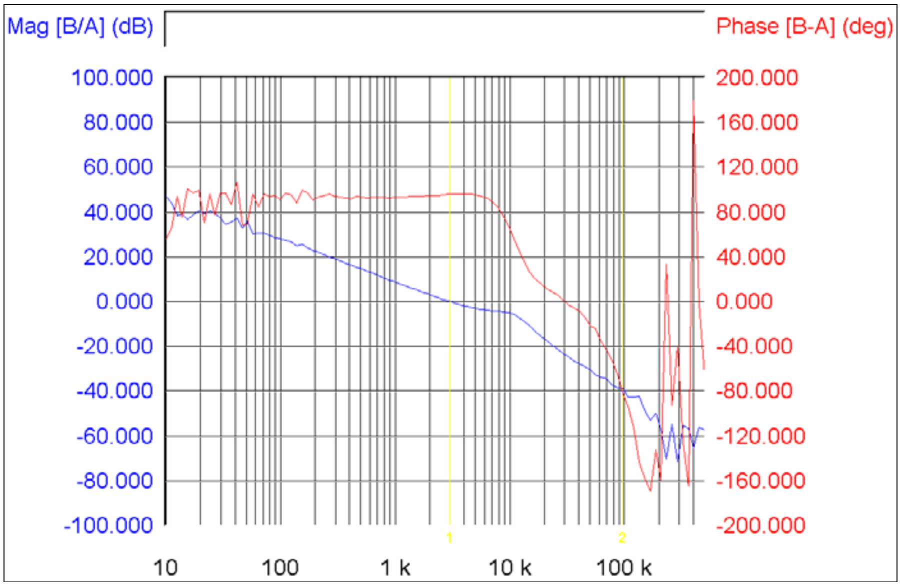


FIGURE 32, Transfer function

Cross-over freq: 2.5kHz
Phase Margin: 90Deg

EN 55022 conductive EMI

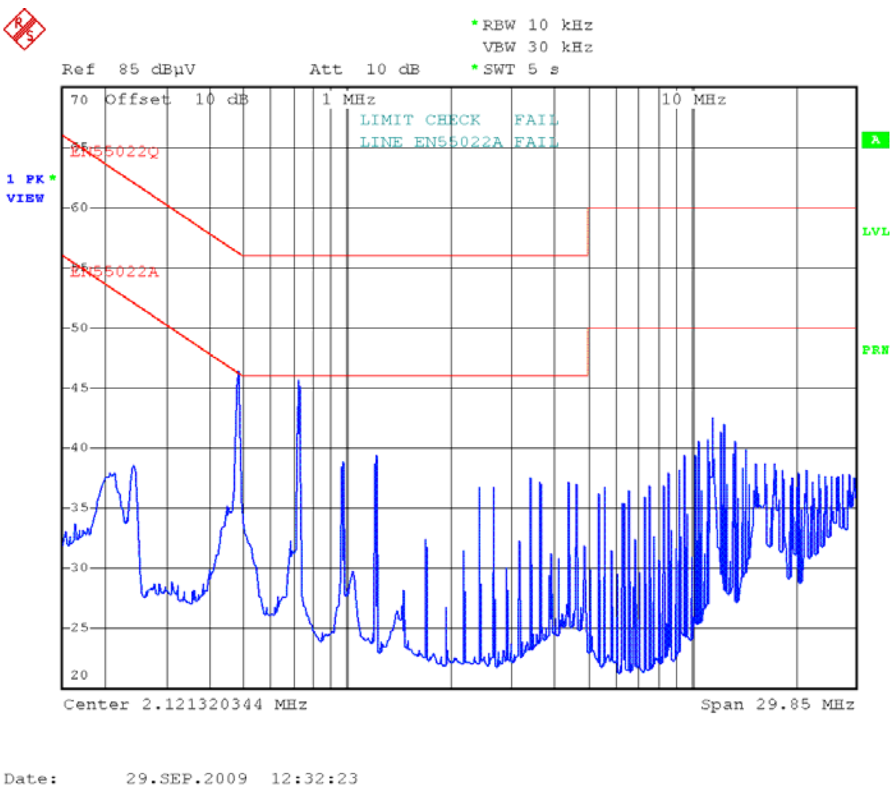
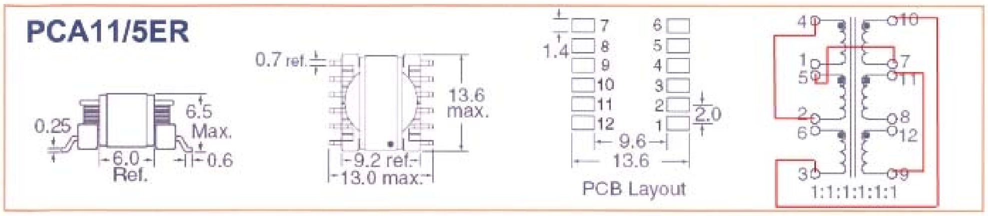


FIGURE 33, Conductive EMI (Average only), Quasi-peak not measured.

Transformer Specifications

SMD Multi Winding Transformer PCA11/5ER Series

TDK



PCA11/5ER Series

Inductance (μH)		IDC (A) (Typ.)		DRC (mΩ) (±15%)		
Parallel	Series	Parallel	Series	Parallel	Series	TDK Part No.
193.0±30%	6.9mH±30%	2.6	0.44	44.4	1607	PCA11/5ER-U01S002
85.8±30%	3.1mH±30%	4.2	0.70	18.4	668	PCA11/5ER-U02S002
27.4±20%	985±20%	2.6	0.44	44.4	1607	PCA11/5ER-U03S002
12.2±20%	438±20%	4.2	0.70	18.4	668	PCA11/5ER-U04S002
14.7±20%	529±20%	2.6	0.44	44.4	1607	PCA11/5ER-U05S002
6.5±20%	235±20%	4.2	0.70	18.4	668	PCA11/5ER-U06S002
10.9±20%	394±20%	2.6	0.44	44.4	1607	PCA11/5ER-U07S002
4.9±20%	175±20%	4.2	0.70	18.4	668	PCA11/5ER-U08S002
8.5±20%	306±20%	2.6	0.44	44.4	1607	PCA11/5ER-U09S002
3.8±20%	136±20%	4.2	0.70	18.4	668	PCA11/5ER-U10S002

NSCE0117 XFMR

Primary Ind.: 173,63uH
Secondary Ind.: 45,48uH
Leakage Ind.: 4,58uH

Measured at 100kHz
Instrument: Wayne Kerr 4270
Automatic LCR Meter

TDK Electronics Europe GmbH - February 2006

 2

FIGURE 17, Transformer Specifications

Layout Design

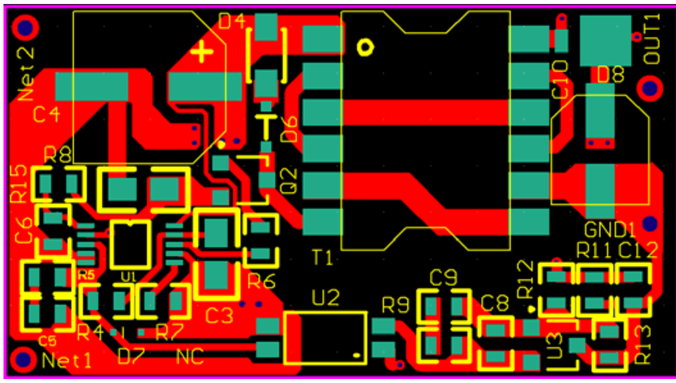


FIGURE 18, TOP Solder

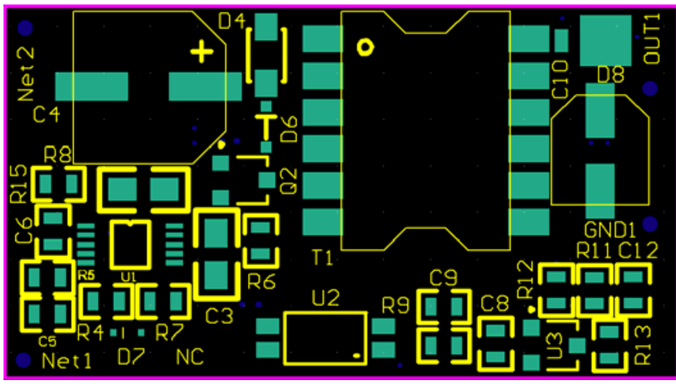


FIGURE 36, TOP Components

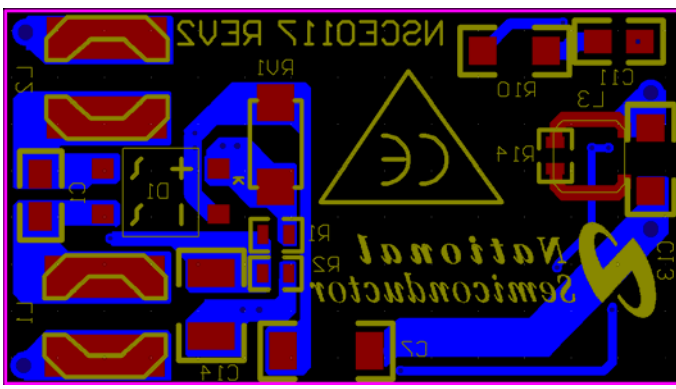


FIGURE 37, Bottom Solder

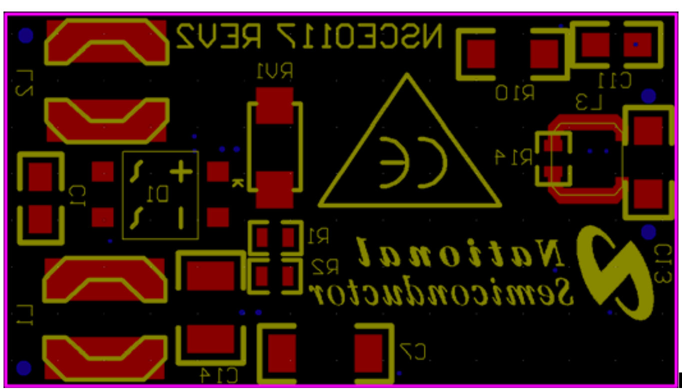


FIGURE 198, BOTTOM Components

Revision History

Version Number	Date	Description of Changes
2.0	2008-05-14	Delay timing and slope compensation added
2.1	2008-11-06	Minor corrections in description
2.2	2008-11-07	Minor corrections in description and units
2.3	2009-02-12	Start up phase and Mosfet Derating
2.4	2009-03-23	CE printed on the PCB
2.5	2009-05-25	Change to new format
2.6	2010-04-21	Change application scope from custom project to generic project. Add conductive EMI measurement result.
2.7	2010-05-28	Minor naming changes. Updated layout pictures, schematic presentation, BOM format.

Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
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Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
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