Application Report
SNVA881–November 2019

Stability Considerations for LP8756x-Q1 and LP8752x-Q1

ABSTRACT

This application report provides an overview of recommended parameters for LP8756x-Q1 and LP8752x-Q1 devices considering stability. Recommendations are based on real measurement data as well as simulations. For more information about LP8756x-Q1 and LP8752x-Q1 devices, refer to the product web pages LP87561-Q1, LP87562-Q1, LP87563-Q1, LP87564-Q1, LP87565-Q1 and LP87523-Q1.

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Trademarks

Keithley 2420 is a trademark of Keithley.
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1 Introduction

The LP8756x-Q1 and LP8752x-Q1 devices are designed to meet the power-management requirements of the latest processors and platforms in various automotive power applications. Both devices contain four stepdown DC/DC converter cores, which are configured as a 4-phase output, 3-phase and 1-phase outputs, 2-phase and 2-phase outputs, one 2-phase and two 1-phase outputs, or four 1-phase outputs. The devices are controlled by an I^2C-compatible serial interface and by enable signals.

The automatic pulse-width-modulation (PWM) to pulsed-frequency-modulation (PFM) operation (AUTO mode) and the automatic phase adding and phase shedding maximizes efficiency over a wide output-current range. The LP8756x-Q1 and LP8752x-Q1 support remote differential-voltage sensing for multiphase outputs, which compensates the IR drop between the regulator output and the point-of-load (POL), improves the accuracy of the output voltage. The switching clock can be forced to the PWM mode and also synchronized to an external clock to minimize the disturbances.

LP8756x-Q1 and LP8752x-Q1 supports the load-current measurement without additional external current sense resistors. The devices also support programmable start-up and shutdown delays and sequences synchronized to enable signals. The sequences can include GPIO signals to control external regulators, load switches, and processor reset. During start-up and voltage change, the devices control the output slew rate to minimize an output voltage overshoot and in-rush current.

This application report can be used as a reference in selecting external components and phase configuration to achieve the wanted phase margin. This application report does not provide information about the electrical characteristics, package, or the functionality of the device. For this information and the full register maps, refer to LP8756x-Q1 16-A Buck Converter With Integrated Switches and LP8752x-Q1 10-A Buck Converter With Integrated Switches datasheets.

2 Stability Target

The loop is stable when the system's feedback is negative and limits the gain. In other words, the loop is unstable if the negative feedback turns into positive feedback, which consequently saturates the output to supply limits. Negative feedback will turn in to positive feedback if the phase changes by 180 degrees and the closed loop gain is positive. The frequency is the point of interest in the measurements where the phase crosses 0 or ±180 degrees and the gain falls below 0 dB (the gain and phase margin is measured from those frequencies). The gain margin defines how much more gain the loop may have until it becomes unstable, and the phase margin defines how much phase shift there may be until the loop becomes unstable.

Generally the loop has sufficient stability margin if it has over 45 degrees of phase margin and over 10 dB of gain margin (these are often the design targets). Even the lower margins and theoretically the loop are stable, if both the gain and phase margins are larger than 0 dB or 0 degrees, but 10 dB gain margin and 45 degree phase margin are considered a standard safety buffer for stability. Higher stability margins are possible at the expense of slower transient response. For the LP8756x-Q1 and LP8752x-Q1 devices, the phase margin of 45 degrees and 10 dB gain margin are a good compromise between stability and transient response. Many different parameters affect both the phase and gain margin, and this application report focuses on systematically iterating through some of the most significant parameters. Layout has an impact on phase margin as well, but iterating through multiple different layouts was not possible. To maximize the phase margin, the PCB parasitic inductance should be minimized and the point of load capacitors should be placed as close to the load as possible. For more information about phase margin and closed loop stability, refer to Switch-mode power converter compensation made easy article.

Please note that the inductor value should be kept at a constant 470 nH, as the internal compensation of the device is configured for previously mentioned inductance. The device verification and validation has been done using 470 nH inductors.

3 Use Cases

General use cases for the LP875x-Q1 devices are listed in Table 1. The total output capacitance is the sum of the C_{LOCAL} capacitance near the switcher and C_{POL} point of load (POL) capacitance. The maximum total output capacitance per phase is 500 µF, if the output voltage slew-rate is less than or equal to 1.9 mV/µs. Higher slew-rates have lower maximum capacitance limits. Refer to LP8756x-Q1 16-A Buck Converter With Integrated Switches or LP8752x-Q1 10-A Buck Converter With Integrated Switches datasheet for more information.

Table 1. Use cases for LP875x devices

V_{IN} (V)	Switching frequency (MHz)	L (nH)	C_{IN} (µF/phase)	V_{OUT} (mV)	C_{LOCAL} (µF/phase)	I_{OUT} (A)	C_{POL} (µF/phase)
3.3	2	470	10	860	22	3.0	22
							44
							91
5.0							22
							44
							91
3.3				1000			22
							44
							91
5.0							22
							44
							91
3.3				1800			22
							44
							91
5.0							22
							44
							91
5.0				3300			22
							44
							91

In addition to the 21 use cases listed in Table 1, the phase configuration has an effect on stability. Every use case is measured and simulated for every phase configuration from 1 to 4 phases, totaling 84 measurements and simulations.

4 Measurements

Measurements are done on the LP8756xQ1EVM evaluation module, which demonstrates the integrated circuit LP8756x-Q1 and LP8752x-Q1 from Texas Instruments. The evaluation module is controlled through the EVM's software graphical user interface (GUI). The software communicates with the EVM through an available USB port.

Table 2. Main components used in measurements

Description	Manufacturer	Part number
CAP, CERM, 10 µF, 10 V, X7R, 10%, 0805	MuRata	GCM21BR71A106KE22
CAP, CERM, 22 µF, 10 V, X7R, 10%, 1206	MuRata	GCM31CR71A226KE02
CAP, CERM, 47 µF, 10 V, X5R, 20%, 0805	MuRata	GRM21BR61A476ME15
Inductor, Shielded, 470 nH, 4.7 A, 0.021 ohm, 1008 (2520)	MuRata	DFE252012PD-R47M

For more information about the used evaluation module and evaluation software, please refer to the The LP8756xQ1EVM (SV601325) Evaluation Module user's guide.

4.1 Measurement Setup

Measurements were done using Clarke Hess 2505 gain phase analyzer which was controlled through an automated LabVIEW sequence. Measurements are done up to 2.4 MHz, which limits some of the gain margin measurement data, since the phase may not cross 0 degrees below 2.4 MHz. The EVM was powered with theQL355TP™ power supply and outputs were loaded withKeithley 2420™. All measurement results are an average of three consequent measurements. The used measurement setup is illustrated in Figure 1.

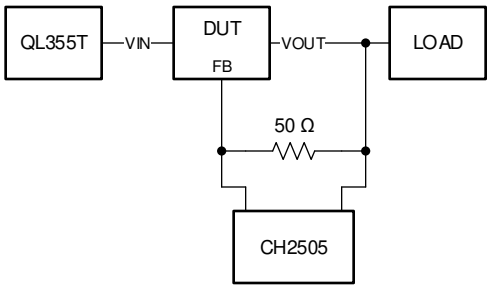

Figure 1. Measurement setup

4.2 Measurement Results

Typical Bode diagrams for every phase configuration are shown in Figure 2, Figure 3, Figure 4 and Figure 5. Each configuration has 1000 mV output voltage and 44 µF POL capacitance.

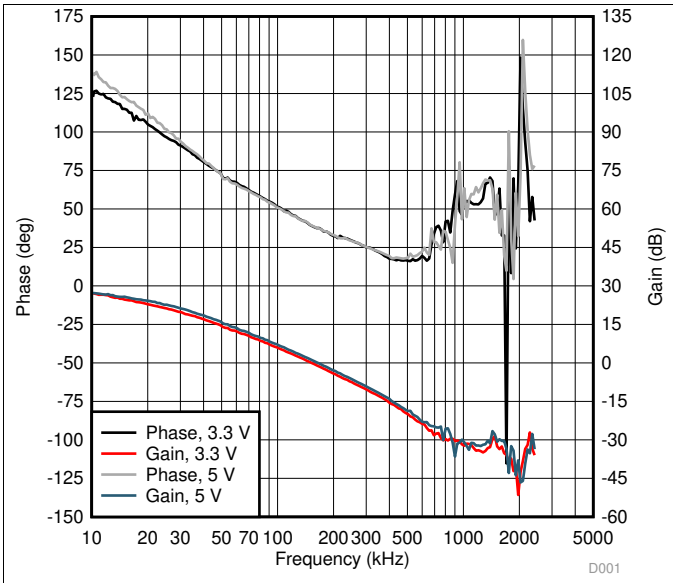

Figure 2. V_{OUT}=1000 mV, C_{POL}=44 µF/phase, 1-phase configuration

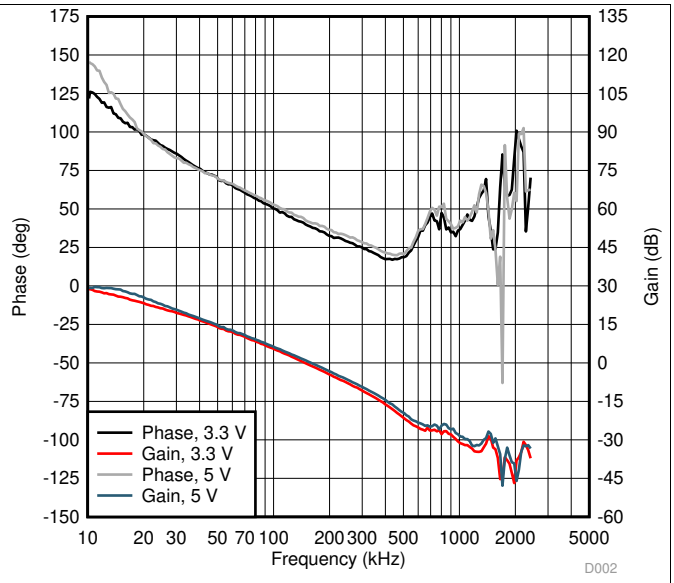

Figure 3. V_{OUT}=1000 mV, C_{POL}=44 µF/phase, 2-phase configuration

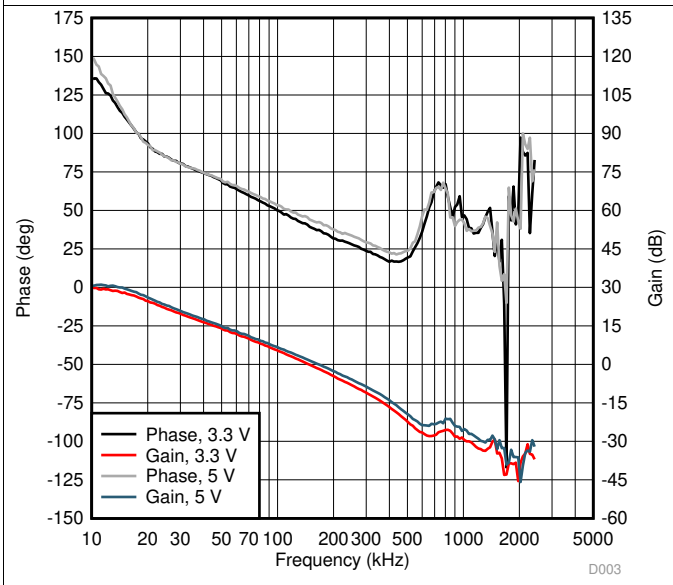

Figure 4. V_{OUT}=1000 mV, C_{POL}=44 µF/phase, 3-phase configuration

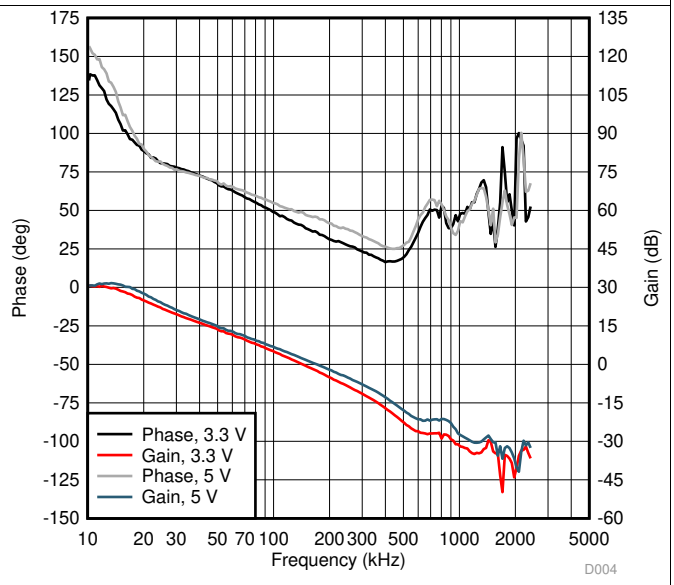

Figure 5. V_{OUT}=1000 mV, C_{POL}=44 µF/phase, 4-phase configuration

All measurement results are listed in Table 3, Table 4, Table 5 and Table 6 for each phase configuration. Results marked with N/A were not possible to measure due to the limitations in the measurement hardware as mentioned in Section 4.1. These results can be used when selecting point of load capacitance to fulfill phase margin requirements on specific V_{IN} and V_{OUT}.

Table 3. Measured gain and phase margins for 1-phase configuration

V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Gain margin (dB)	Phase margin (deg)
3.3	860	22	193.2	18.3	30.3
		44	147.7	31.1	36.9
		91	101.7	38.5	48.5
	1000	22	201.2	17.8	32.0
		44	152.4	35.3	39.1
		91	104.4	N/A	50.4
	1800	22	224.5	17.3	38.8
		44	167.4	29.2	46.0
		91	116.2	36.1	55.3
5.0	860	22	229.6	19.6	34.0
		44	172.0	N/A	41.0
		91	114.6	N/A	52.0
	1000	22	219.0	19.9	30.8
		44	164.7	N/A	37.5
		91	112.1	N/A	48.4
	1800	22	245.7	17.7	39.2
		44	181.4	30.9	45.4
		91	124.9	39.4	55.4
	3300	22	296.9	13.8	45.4
		44	207.5	26.9	51.9
		91	152.5	26.2	58.1

Table 4. Measured gain and phase margins for 2-phase configuration

V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Gain margin (dB)	Phase margin (deg)
3.3	860	22	188.2	19.0	31.9
		44	143.9	35.4	39.1
		91	95.2	N/A	50.4
	1000	22	193.6	18.7	33.2
		44	147.5	N/A	40.3
		91	99.6	N/A	50.7
	1800	22	209.8	18.6	36.3
		44	158.8	N/A	43.3
		91	110.7	N/A	52.3
5.0	860	22	223.4	22.0	35.9
		44	168.1	34.5	43.7
		91	108.3	N/A	54.0
	1000	22	210.7	21.7	34.6
		44	159.4	38.4	41.0
		91	105.7	N/A	52.2
	1800	22	236.3	20.6	39.9
		44	174.0	N/A	46.9
		91	119.4	N/A	55.0
	3300	22	273.3	16.3	44.8
		44	194.2	26.8	50.3
		91	137.0	27.8	56.5

Table 5. Measured gain and phase margins for 3-phase configuration

V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Gain margin (dB)	Phase margin (deg)
3.3	860	22	186.7	21.3	31.2
		44	144.2	36.7	38.8
		91	100.5	N/A	48.3
	1000	22	193.7	19.9	32.7
		44	147.4	41.5	39.8
		91	102.6	N/A	49.8
	1800	22	209.2	19.4	36.3
		44	157.0	37.7	42.6
		91	111.4	N/A	51.5
5.0	860	22	246.4	21.2	36.1
		44	183.1	32.9	45.6
		91	122.2	N/A	55.5
	1000	22	223.9	20.7	35.0
		44	166.2	35.6	42.4
		91	112.5	N/A	51.5
	1800	22	241.3	19.8	39.2
		44	175.8	29.5	46.2
		91	123.0	N/A	53.7
	3300	22	287.8	15.9	42.4
		44	204.6	25.8	50.1
		91	146.5	27.1	55.1

Table 6. Measured gain and phase margins for 4-phase configuration

V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Gain margin (dB)	Phase margin (deg)
3.3	860	22	180.7	20.6	31.6
		44	136.9	N/A	38.3
		91	95.3	N/A	48.6
	1000	22	189.7	20.3	32.8
		44	143.3	N/A	40.0
		91	99.5	N/A	49.4
	1800	22	207.6	23.4	36.5
		44	153.7	N/A	42.8
		91	109.7	N/A	50.8
5.0	860	22	261.0	N/A	38.0
		44	194.7	N/A	48.9
		91	129.5	N/A	59.8
	1000	22	240.6	N/A	38.1
		44	170.7	N/A	45.7
		91	113.4	N/A	54.0
	1800	22	231.4	31.7	39.8
		44	169.0	N/A	47.4
		91	118.4	N/A	54.2
	3300	22	263.7	28.2	44.9
		44	197.2	28.1	50.1
		91	137.4	N/A	55.0

5 Simulations

All of the use cases listed in Table 1 and all phase configurations were simulated using SIMPLIS.

5.1 Simulation Model

Simulations were completed using the simulation model schematic in Figure 6. The simulation model is available here. The model includes parameters for phase configuration, input and output voltage, switching frequency, local capacitance, and point of load capacitance. The model also has some of the parasitics parametrized, including the equivalent series inductances and resistances of capacitors, DC resistances of inductors, and PCB parasitics. To change these parameters press F11 to open the command window where the parameters are listed in a text format. Parameters and their descriptions are in Table 7.

Table 7. Simulation parameters

Parameter	Description
Vin	Input voltage
Vout	Target output voltage
stepLow	Initial current in transient analysis
stepHigh	Pulse current in transient analysis
riseTime	Rise time of the pulse current
fallTime	Fall time of the pulse current
swFreq	Switching frequency
NofPhases	Phase count
Cout_local	Local capacitance per phase
Cout_local_ESR	Equivalent series resistance (ESR) of a local capacitor
Cout_local_ESL	Equivalent series inductance (ESL) of a local capacitor
Cout_local_shunt	Shunt resistance of local capacitor's ESL
Cout_POL	Point of load (POL) capacitance per phase
Cout_POL_ESR	Equivalent series resistance (ESR) of a POL capacitor
Cout_POL_ESL	Equivalent series inductance (ESL) of a POL capacitor
Cout_POL_quantity	POL capacitor quantity per phase
Cout_POL_shunt	Shunt resistance of POL capacitor's ESL
L	Inductor per phase
L_DCR	Inductor's DC resistance
rPCB	Parasitic resistance from PCB
lPCB	Parasitic inductance from PCB
rPCB_GND	Parasitic resistance from PCB ground plane
lPCB_GND	Parasitic inductance from PCB ground plane

The capacitor parameters should be chosen according to the capacitance needed per phase. The simulation model provides Bode plot and step load transient simulation results when using the default simulation configuration. The step load parameters can be configured by double clicking the LOAD current waveform generator. The default configuration is step load of 1 A - 3 A - 1 A.

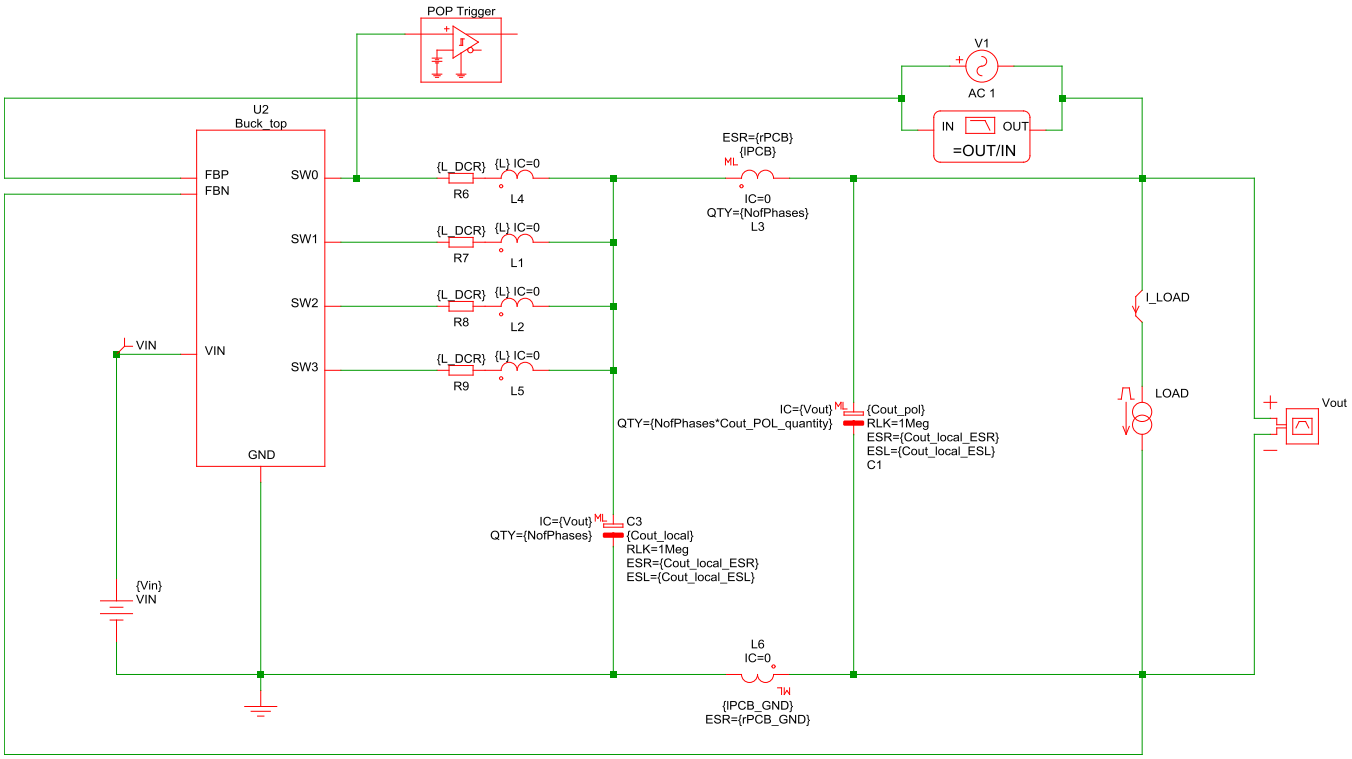

Figure 6. Simulation schematic

5.2 Simulation Results

Same configurations that were measured and plotted in Figure 2, Figure 3, Figure 4 and Figure 5 were simulated and plotted in Figure 7, Figure 8, Figure 9 and Figure 10. Configurations had 44 µF of point of load capacitance per phase in every phase configuration.

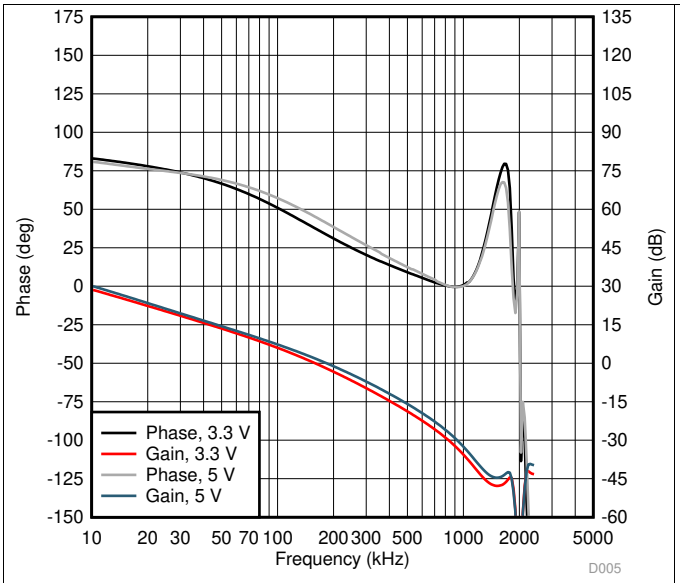

Figure 7. V_{OUT}=1000 mV, C_{POL}=44 µF/phase, 1-phase configuration

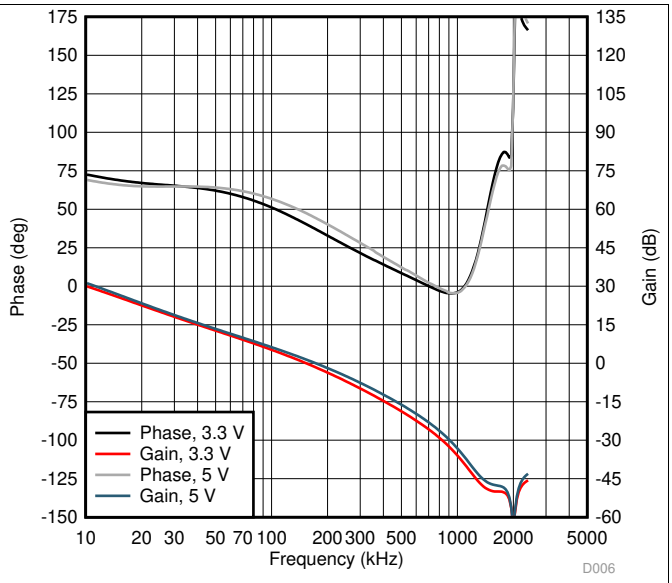

Figure 8. V_{OUT}=1000 mV, C_{POL}=44 µF/phase, 2-phase configuration

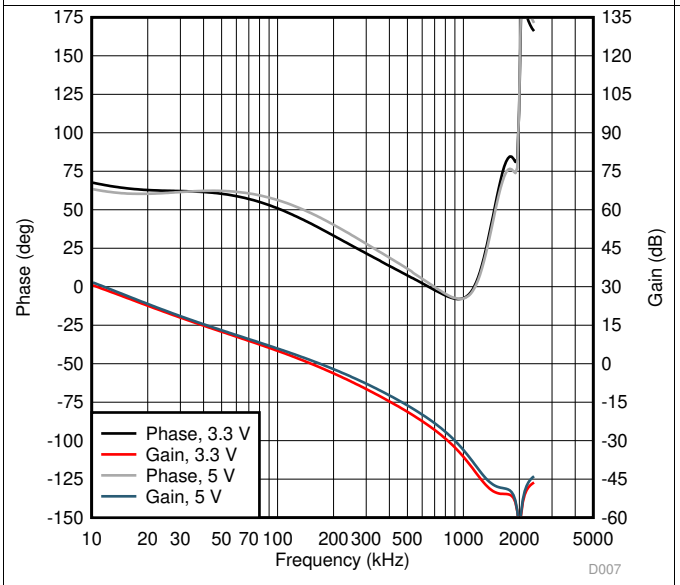

Figure 9. V_{OUT}=1000 mV, C_{POL}=44 µF/phase, 3-phase configuration

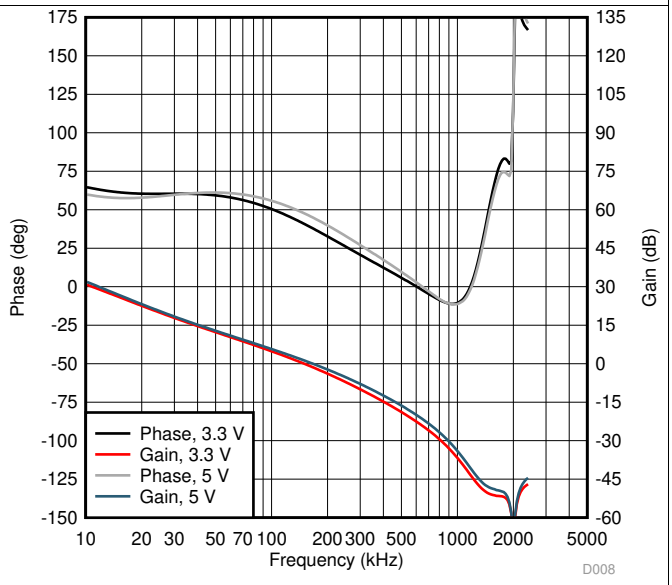

Figure 10. V_{OUT}=1000 mV, C_{POL}=44 µF/phase, 4-phase configuration

All simulation results are listed in Table 8, Table 9, Table 10 and Table 11.

Table 8. Simulated gain and phase margins for 1-phase configuration

V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Gain margin (dB)	Phase margin (deg)
3.3	860	22	202.1	43.5	34.1
		44	158.3	28.7	37.9
		91	109.7	64.0	45.1
	1000	22	203.5	43.4	33.7
		44	159.1	30.1	37.6
		91	110.1	65.0	45.0
	1800	22	211.6	42.8	33.8
		44	164.2	29.0	38.2
		91	112.2	85.9	46.1
5.0	860	22	235.5	40.6	36.9
		44	182.4	27.3	41.3
		91	124.0	58.7	49.4
	1000	22	236.3	40.3	36.4
		44	183.4	27.3	41.0
		91	124.5	57.4	49.2
	1800	22	243.9	39.6	36.1
		44	188.1	28.1	41.2
		91	126.6	57.9	49.8
	3300	22	263.9	38.7	38.9
		44	199.8	46.6	44.3
		91	131.5	85.2	53.0

Table 9. Simulated gain and phase margins for 2-phase configuration

V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Gain margin (dB)	Phase margin (deg)
3.3	860	22	197.9	69.1	35.7
		44	152.4	25.6	40.2
		91	102.9	68.0	47.8
	1000	22	199.6	68.6	35.7
		44	153.4	25.8	40.4
		91	103.3	67.6	48.0
	1800	22	207.4	68.1	37.0
		44	158.1	25.9	42.0
		91	105.1	67.4	49.8
5.0	860	22	225.7	68.8	39.2
		44	171.6	24.8	44.3
		91	113.3	74.0	52.3
	1000	22	227.4	68.8	39.2
		44	172.6	25.2	44.4
		91	113.8	74.4	52.4
	1800	22	235.8	67.7	40.3
		44	177.4	24.9	45.7
		91	115.7	73.1	53.7
	3300	22	252.1	68.5	43.7
		44	186.9	24.0	49.4
		91	119.2	75.1	57.1

Table 10. Simulated gain and phase margins for 3-phase configuration

V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Gain margin (dB)	Phase margin (deg)
3.3	860	22	196.8	27.5	35.9
		44	150.6	24.2	40.7
		91	100.7	32.8	48.3
	1000	22	198.4	28.1	36.0
		44	151.5	24.1	40.9
		91	101.0	33.9	48.6
	1800	22	205.8	52.7	37.7
		44	155.9	24.2	42.9
		91	102.6	52.1	50.6
5.0	860	22	222.3	26.3	39.5
		44	168.0	23.2	44.8
		91	110.0	52.0	52.7
	1000	22	223.9	26.8	39.6
		44	168.9	23.1	45.0
		91	110.3	52.1	52.9
	1800	22	231.9	26.5	41.0
		44	173.5	22.9	46.5
		91	112.1	52.7	54.4
	3300	22	248.9	53.3	45.0
		44	183.0	22.5	50.7
		91	115.6	53.8	58.0

Table 11. Simulated gain and phase margins for 4-phase configuration

V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Gain margin (dB)	Phase margin (deg)
3.3	860	22	195.4	23.8	35.6
		44	149.2	22.6	40.6
		91	99.4	29.2	48.3
	1000	22	196.4	24.3	35.8
		44	149.8	22.7	40.8
		91	99.6	29.5	48.6
	1800	22	204.2	23.6	37.8
		44	154.3	22.8	43.1
		91	101.2	30.2	50.8
5.0	860	22	221.1	22.8	39.4
		44	166.4	22.0	44.8
		91	108.4	29.6	52.7
	1000	22	221.8	22.5	39.6
		44	166.7	21.5	44.9
		91	108.5	28.9	52.8
	1800	22	230.0	22.8	41.1
		44	171.5	21.6	46.7
		91	110.4	30.0	54.5
	3300	22	246.4	22.3	45.2
		44	180.4	21.5	50.9
		91	113.5	60.7	58.2

6 Summary

Figure 11, Figure 12, Figure 13, and Figure 14 summarize the measured phase margins for every phase configuration. The figures include all the measured combinations and are divided into different figures based on the phase configuration. These figures can be used when selecting point of load capacitors for the systems using the LP8756x-Q1 or LP8752x-Q1 PMICs.

To select the required point of load capacitor value which achieves a sufficient phase margin, do the following:

1. Take a look at the figure corresponding to the phase configuration.
2. Select the curve that matches the desired V_{OUT} and V_{IN} parameters the closest.
3. Find the point on which the curve crosses the desired phase margin value and read the horizontal C_{POL} value on that point.

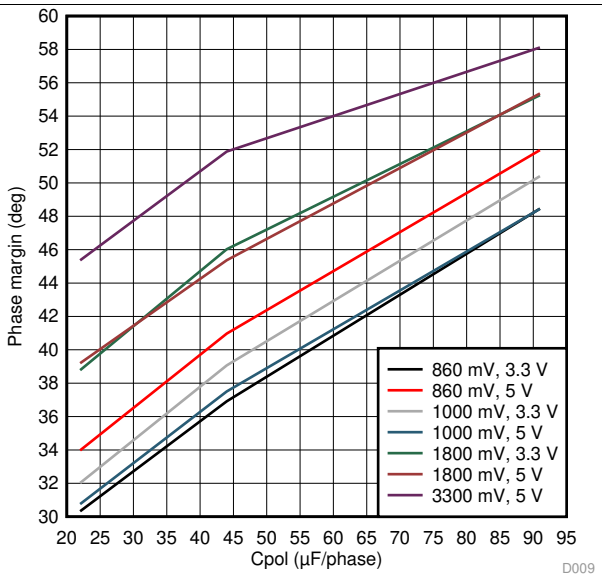

Figure 11. Phase margins for 1-phase configurations

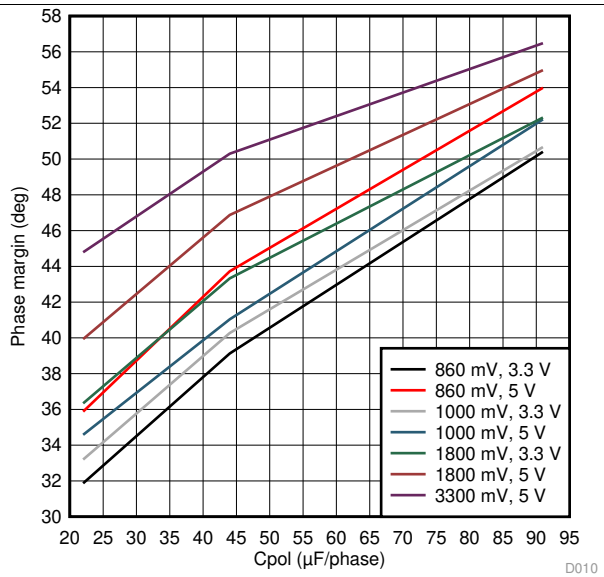

Figure 12. Phase margins for 2-phase configurations

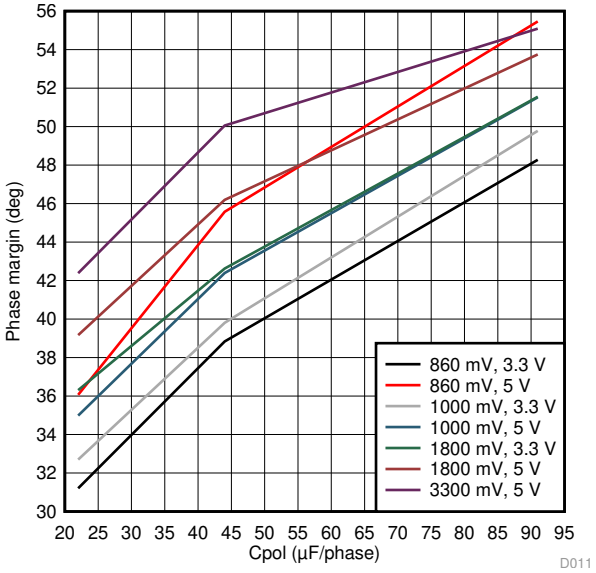

Figure 13. Phase margins for 3-phase configurations

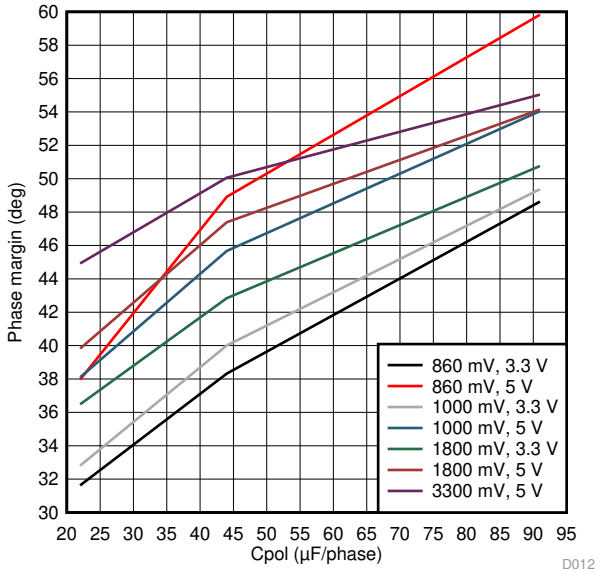

Figure 14. Phase margins for 4-phase configurations

The minimum capacitor configurations that fulfilled the 45 degree phase margin requirement are listed in Table 12

Table 12. Minimum C_{POL} required for 45 degree phase margin

Phases	V_{IN} (V)	V_{OUT} (mV)	C_{POL} (µF/phase)	Bandwidth (kHz)	Phase margin (deg)
1 (LP875x4/3/2-Q1)	3.3	860	91	101.7	48.5
		1000	91	104.4	50.4
		1800	44	167.4	46.0
	5	860	91	114.6	52.0
		1000	91	112.1	48.4
		1800	44	181.4	45.4
		3300	22	296.9	45.4
2 (LP875x3/5-Q1)	3.3	860	91	95.2	50.4
		1000	91	99.6	50.7
		1800	91	110.7	52.3
	5	860	91	108.3	54.0
		1000	91	105.7	52.2
		1800	44	174.0	46.9
		3300	44	194.2	50.3
3 (LP875x2-Q1)	3.3	860	91	100.5	48.3
		1000	91	102.6	49.8
		1800	91	111.4	51.5
	5	860	44	183.1	45.6
		1000	91	112.5	51.5
		1800	44	175.8	46.2
		3300	44	204.6	50.1
4 (LP875x1-Q1)	3.3	860	91	95.3	48.6
		1000	91	99.5	49.4
		1800	91	109.7	50.8
	5	860	44	194.7	48.9
		1000	44	170.7	45.7
		1800	44	169.0	47.4
		3300	44	197.2	50.1

7 References

See these references for additional information:

1. Texas Instruments, LP8756x-Q1 16-A Buck Converter with Integrated Switches Datasheet.
2. Texas Instruments, LP8752x-Q1 10-A Buck Converter with Integrated Switches Datasheet.
3. Robert Sheehan, Louis Diana, Texas Instruments, Switch-mode Power Converter Compensation Made Easy.
4. Texas Instruments, LP8756xQ1EVM (SV601325) Evaluation Module User's Guide.

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