User's Guide
SNVA852–December 2018

Power Supply Design for Mobileye EyeQ4 Using LP875701-Q1

This document details the design considerations of a power management unit solution for the Mobileye EyeQ4 Mid SoC (system-on-chip) core rail using the LP875701-Q1 power management IC. This power solution assumes an input voltage of 3.3 V or 5 V (+/-5%). If the system input voltage is higher, for example a car battery, a buck converter as a pre-regulator should be used to generate a supply voltage of 3.3 V or 5 V

The LP878701A-Q1 has 4 buck converters configured to work as single 1 V output multiphase converter. LP875701 operates in PWM mode with all 4 phases switching in interleaved mode when output is activated.

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1 Design Parameters

Design target parameters for the EyeQ4 Mid core rail power is show in Table 1 and typical measurement data is seen in Section 6.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
VIN	3.3 V / 5 V (+/-5%)
V_{OUT}	1 V
I_{OUT}	7.5 A max (LP875701A-Q1 supports up to 10 A load current)
V_{OUT} tolerance	+/-3% in all conditions including DC accuracy and load transient
Load transient	6 A/µs, 1.5 A to 7.5 A to 1.5 A
C_{IN}(nom)	At least 10µF capacitor per phase
C_{OUT}(nom)	144µF total capacitance per phase, including point of load capacitors
C_{OUT}(min)	100µF total capacitance per phase, including point of load capacitors
C_{OUT}(max)	1500µF total, all phases combined, including point of load capacitors
L (nom)	330 nH, at least 3.5 A saturation current
Phase margin	>45°
Gain margin	>10 dB

2 Power Solution

Figure 1 shows an example block diagram of LP875701-Q1 device powering the EyeQ4 Mid core rail, and LP87563x PMIC powering the other required rails. PMIC from the LP87563x family could be configured to power the other rails depending on use case.

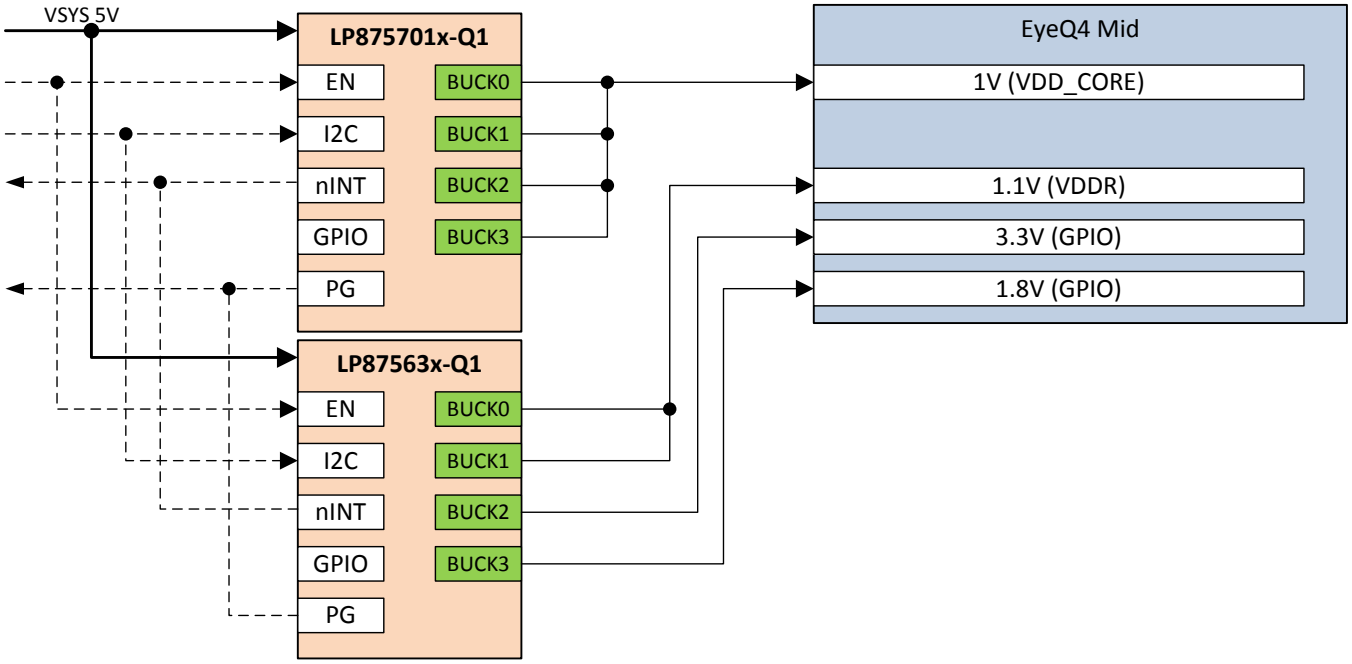


Figure 1. EyeQ4 Mid Power Solution Block Diagram

After the devices are powered, the microcontroller can set the EN pin high to enable the PMIC. Startup delay of the LP875701ARNFRQ1 has been set to 0 ms. Full OTP register settings of LP875701ARNFRQ1 can be found in *LP875701A-Q1 Technical Reference Manual*. I^2C can be used to read status registers and reset interrupts.

3 Schematic

LP875701 schematic with critical components is shown in Figure 2. Input EMI filters are optional. Snubbers are needed when input voltage of the system is >4 V, otherwise they are optional.

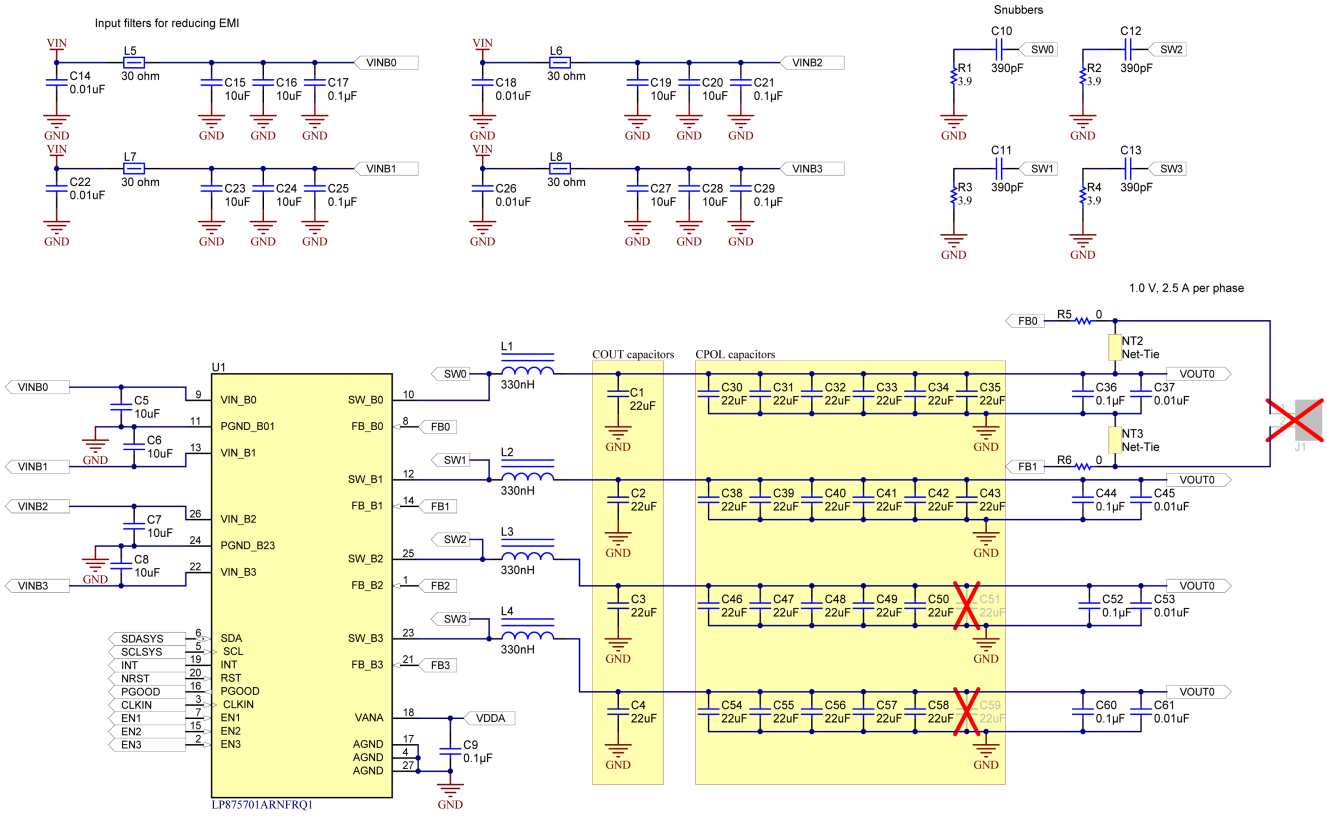


Figure 2. EyeQ4 Mid Core Rail Schematic

4 Layout

4.1 Layout Considerations

The high frequency and large switching currents of the LP875701-Q1 make the choice of layout important. Good power supply results only occur when care is given to correct design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to 10 A and over, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to make sure the device is stable and keeps correct voltage and current regulation across its intended operating voltage and current range.

- Place each CIN as close as possible to the VIN_Bx pin and the PGND_Bxx pin. In the example layout input capacitors are placed on the bottom side of the board to help with the layout routing. Use multiple vias with high enough current rating and route the VIN trace wide and thick to avoid IR drops. The trace between the positive node of the input capacitor and the VIN_Bx pin(s) of LP875701-Q1, as well as the trace between the negative node of the input capacitor and power PGND_Bxx pin(s), must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor — parasitic inductance on these traces must be kept as small as possible for correct device operation. The parasitic inductance can be decreased by using a ground plane as close as possible to top/bottom layer by using thin dielectric layer between top/bottom layer and ground plane.
- The output filter, consisting of COUT and L, converts the switching signal at SW_Bx to the noiseless output voltage. It must be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the LP875701-Q1 output capacitors and the load direct and wide to avoid losses due to the IR drop.

- Input for analog blocks (VANA and AGND) must be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.
- If the processor load supports remote voltage sensing, connect the feedback pins FB_Bx of the LP875701-Q1 device to the respective sense pins on the processor. In any case connect feedback pin FB_B0 to supply terminal of the point-of-load, and feedback pin FB_B1 to the GND of the point-of-load. This allows compensating for the IR drop from the buck output to the point of load and also on the GND. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND_Bxx, VIN_Bx, and SW_Bx, as well as high bandwidth signals such as the I^2C. Avoid both capacitive and inductive coupling by keeping the sense lines short, direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. Running the signal as a differential pair is recommended for multiphase outputs.
- PGND_Bxx, VIN_Bx and SW_Bx must be routed on thick layers. They must not surround inner signal layers, which are cannot withstand interference from noisy PGND_Bxx, VIN_Bx and SW_Bx.
- If the input voltage is above 4 V, place snubber components (capacitor and resistor) between SW_Bx and ground on all four phases. The components can be also placed to the other side of the board if there are area limitations and the routing traces can be kept short.
- Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent parameters such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Correct PCB layout, focusing on thermal performance, results in lower die temperatures. Wide and thick power traces can sink dissipated heat. This can be improved further on multilayer PCB designs with vias to different planes. This results in decreased junction-to-ambient ($R_{\theta JA}$) and junction to- board ($R_{\theta JB}$) thermal resistances and thereby decreases the device junction temperature, T_J. TI strongly recommends doing a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process, by using a thermal modeling analysis software.

4.2 Example Layout

LP875701 Layout from LP875701Q1EVM with critical components is shown in this section. See LP875701Q1EVM User Guide for more details.

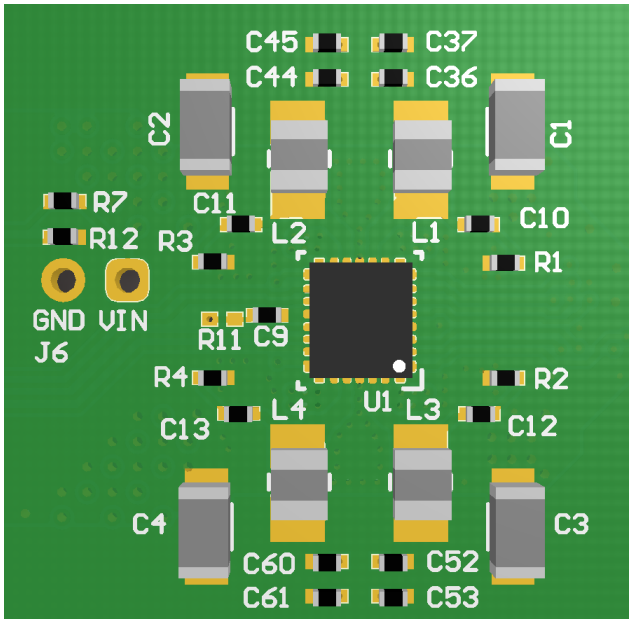


Figure 3. LP875701-Q1 Top Component Placement

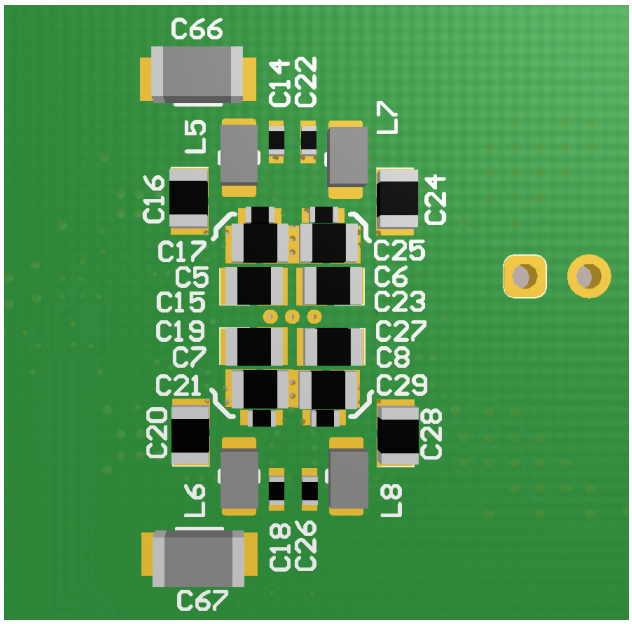


Figure 4. LP875701-Q1 Bottom Component Placement

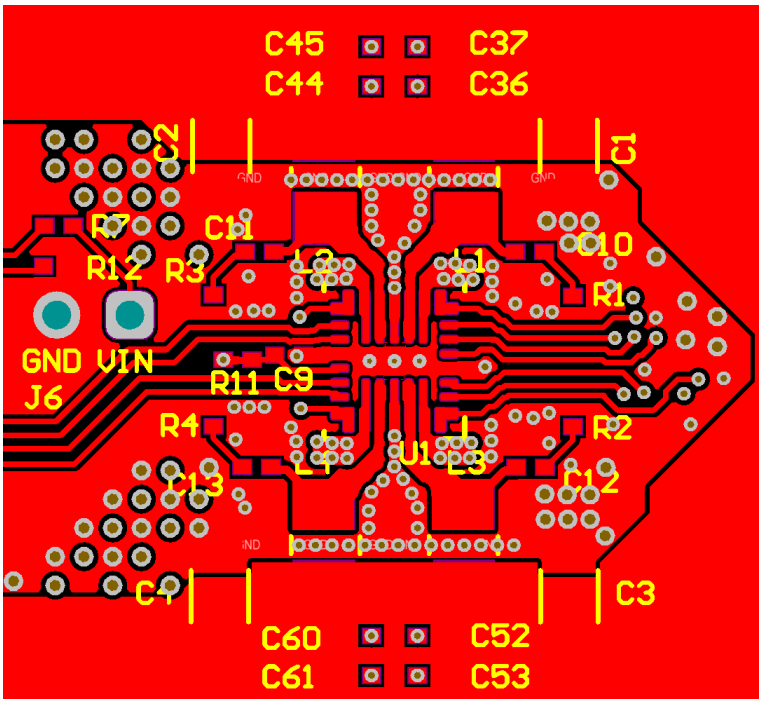


Figure 5. LP875701-Q1 Layout, Layer 1

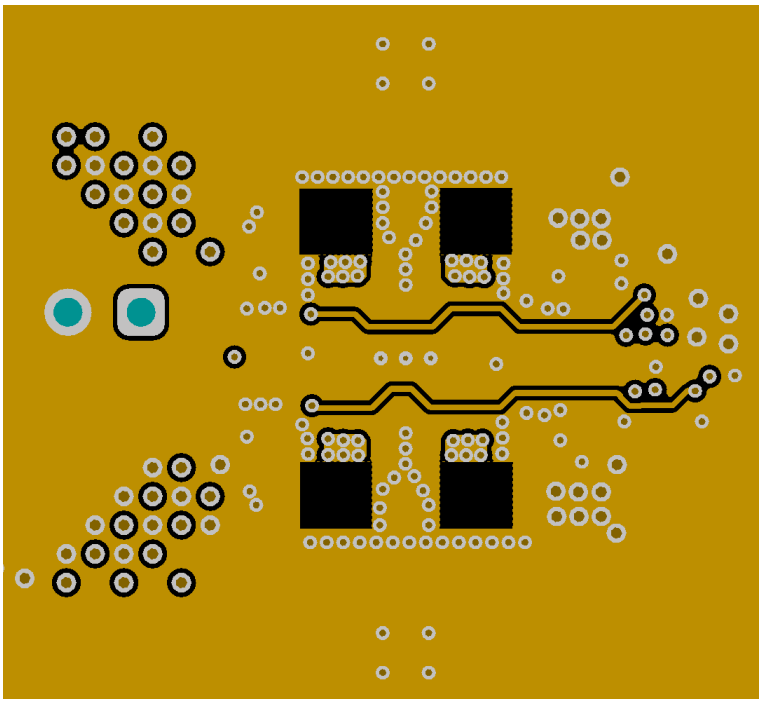


Figure 6. LP875701-Q1 Layout, Layer 2

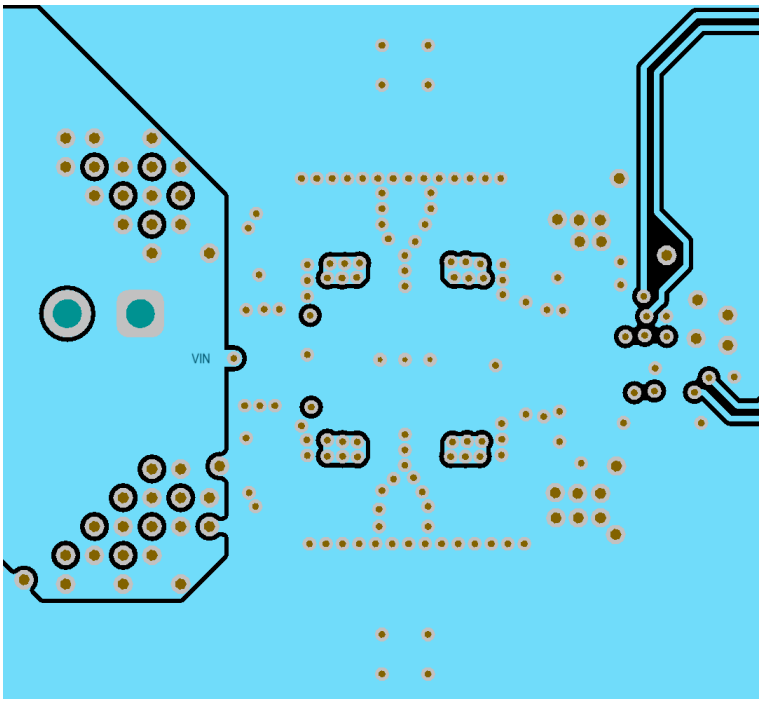


Figure 7. LP875701-Q1 Layout, Layer 3

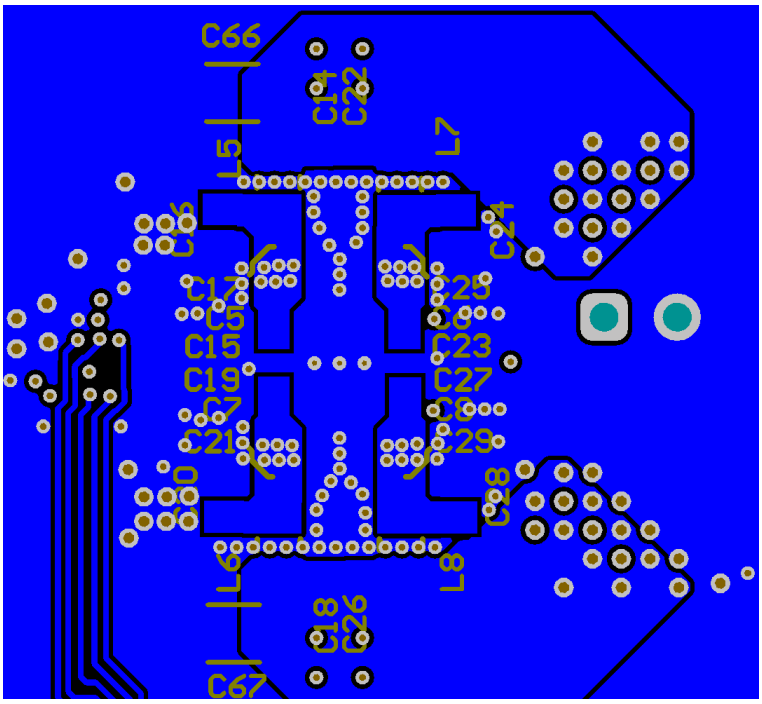


Figure 8. LP875701-Q1 Layout, Layer 4, Bottom

5 Recommended External Components

See Table 2 for the recommended external components to use in this solution with the LP875701-Q1. It also shows the total solution size including the PMIC device and the external components.

Table 2. Bill of Materials

SYSTEM COMPONENT	COUNT	VALUE	SIZE	PART NUMBER	MANUFACTURER	BOARD SIZE(1)
PMIC	1	-	4.5 x 4 mm	LP875701ARNFRQ1	TI	27.5 mm^2
Buck input capacitor	4	10 µF	0805	GCM21BR71A106KE22L	Murata	27 mm^2
Buck output inductor	4	0.33 µH	1008	DFE252012PD-R33M	Murata	42 mm^2
Buck output capacitor	26	22 µF	1206	GCM31CR71A226KE02	Murata	283.9 mm^2
Buck output capacitor	4	100 nF	0402	GCM155R71C104JA55D	Murata	12 mm^2
Buck output capacitor	4	10 nF	0402	GCM155R71H103KA55D	Murata	12 mm^2
VANA supply capacitor	1	100 nF	0402	GCM155R71C104JA55D	Murata	3 mm^2
Snubber resistor	4	3.9 ohm	0402	CRCW04023R90JNED	Vishay-Dale	12 mm^2
Snubber capacitor	4	390 pF	0402	CGA2B2C0G1H391J050BA	TDK	12 mm^2
TOTAL	52	-	-	-	-	431.4 mm^2

(1) Assuming 1 mm keep-out around each component, and multiplying by component count

6 Measurements

Test data can be found in the Application Curves section of the *LP875701-Q1 Four-Phase 3-MHz 1-V 10-A DC/DC Buck Converter With Integrated Switches Datasheet*.

Additional bench test data for load transient response, efficiency, and phase margin can be seen in this section at different input voltages.

Measurements were taken on LP875701Q1EVM with default components. For load transient a special high speed amplifier controlled current sink was used to realize 1.5A to 7.5A to 1.5A transient with 1µs slew rate (6A/µs).

Control loop response (Bode plot) was measured with Keysight MSOX6004A oscilloscope.

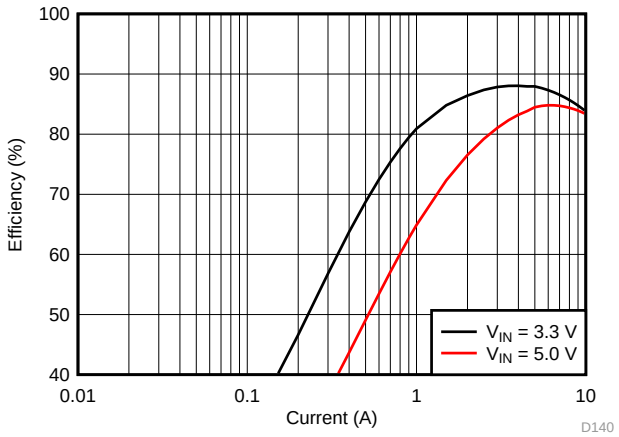


Figure 9. LP875701-Q1 Efficiency at Vin = 5 V and Vin = 3.3 V

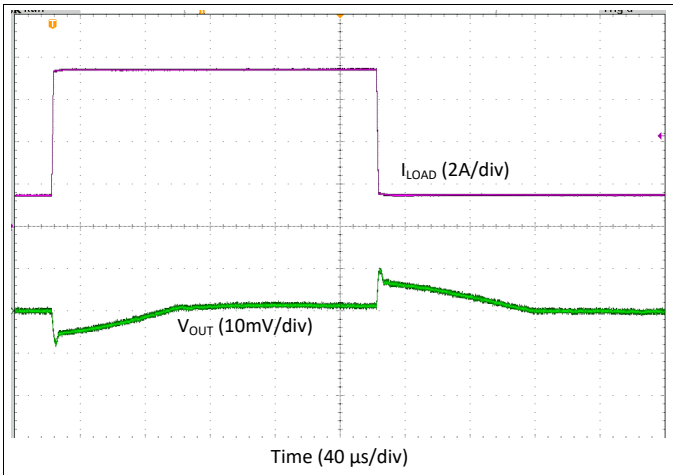


Figure 10. LP875701-Q1 Load Transient Response at Vin = 5 V, 25°C. -8.4 mV / +9.8 mV

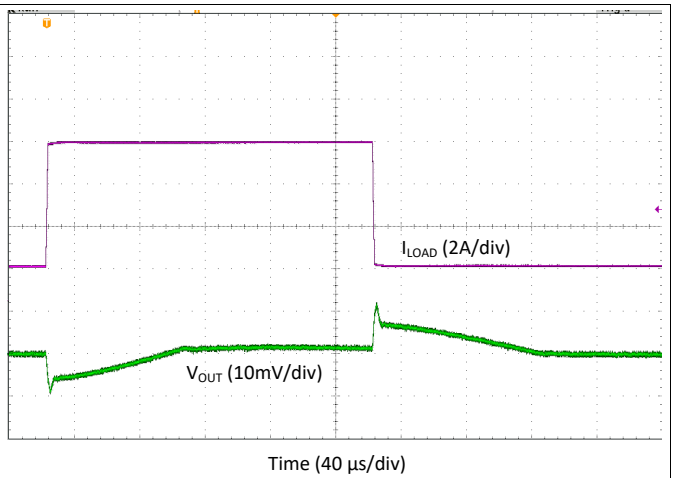


Figure 11. LP875701-Q1 Load Transient Response at Vin = 5 V, 125°C. -9.3 mV / +12.2 mV

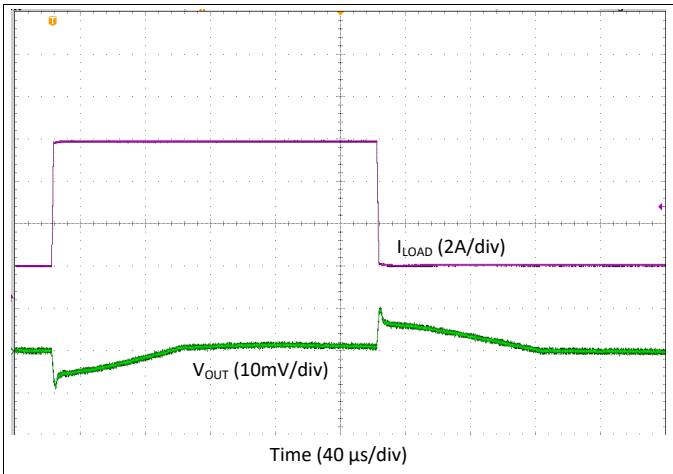


Figure 12. LP875701-Q1 Load Transient Response at Vin = 5 V, -40°C. -8.6 mV / +10.3 mV

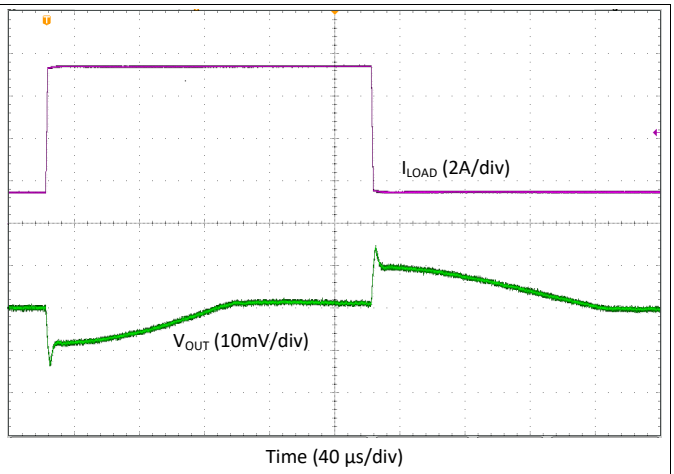


Figure 13. LP875701-Q1 Load Transient Response at Vin = 3.3 V, 25°C. -13.7 mV / +14.6 mV

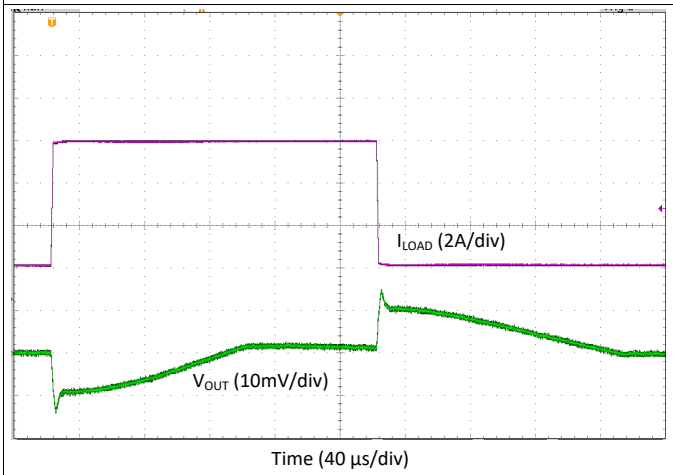


Figure 14. LP875701-Q1 Load Transient Response at Vin = 3.3 V, 125°C. -13.6 mV / +14.7 mV

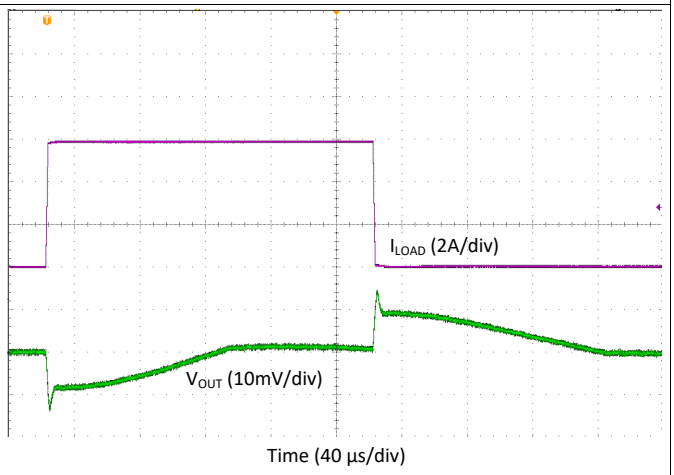


Figure 15. LP875701-Q1 Load Transient Response at Vin = 3.3 V, -40°C. -13.6 mV / +14.7 mV.

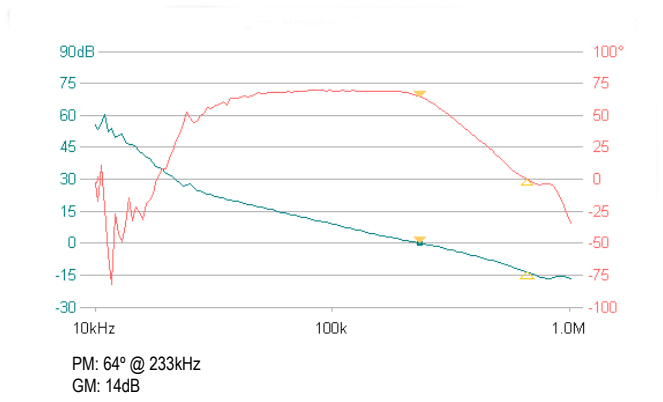


Figure 16. LP875701-Q1 Phase Margin / Bode Plot at Vin = 5 V, 25°C

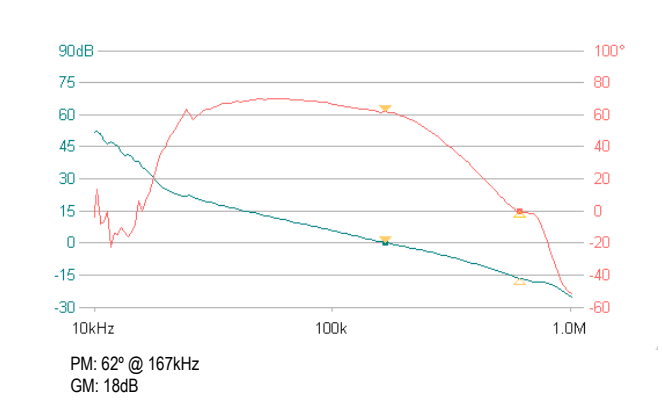
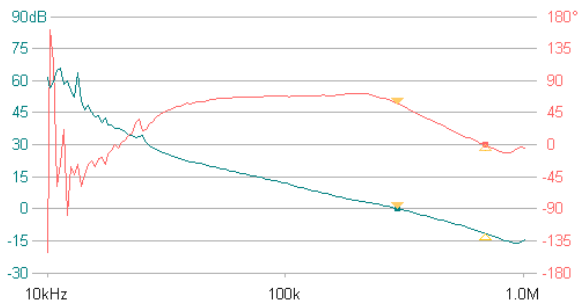
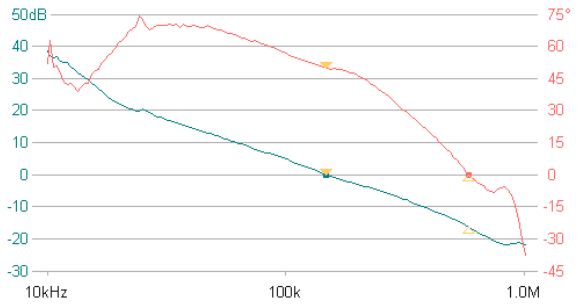


Figure 17. LP875701-Q1 Phase Margin / Bode Plot at Vin = 5 V, 125°C



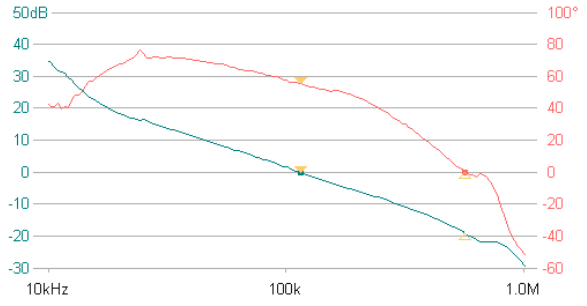
PM: 57° @ 294kHz
GM: 13dB

Figure 18. LP875701-Q1 Phase Margin / Bode Plot at Vin = 5 V, -40°C



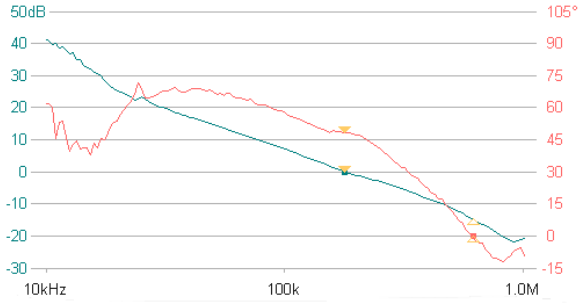
PM: 50° @ 147kHz
GM: 16dB

Figure 19. LP875701-Q1 Phase Margin / Bode Plot at Vin = 3.3 V, 25°C



PM: 55° @ 115kHz
GM: 19dB

Figure 20. LP875701-Q1 Phase Margin / Bode Plot at Vin = 3.3 V, 125°C



PM: 48° @ 178kHz
GM: 15dB

Figure 21. LP875701-Q1 Phase Margin / Bode Plot at Vin = 3.3 V, -40°C

7 Conclusion

With this presented solution with LP875701-Q1 the output voltage accuracy requirement is met for EyeQ4 Mid application processor while maintaining good efficiency. Phase margin is over 50° in all measured conditions which shows good stability of the control loop. Table 3 shows combined data for the critical parameters.

Table 3. Results

Parameter	Result	Comment
DC output voltage accuracy, includes voltage reference, DC load and line regulations, process, and temperature effect	Within +/-15 mV	+/-1.5% with 1 V output voltage
Transient load step response 1.5 A to 7.5 A to 1.5 A. 6 A/µs	Within +/-15 mV	+/-1.5% with 1 V output voltage
Total accuracy including DC + transient	Within +/-30 mV	+/-3% with 1 V output voltage
Efficiency	88% at 4 A load, VIN = 3.3 V	
Phase margin	50...64° depending on condition	>45° is considered good design target
Gain margin	13...19 dB depending on condition	>10 dB is considered as good design target
Bandwidth	114...294 kHz depending on condition	

8 References

See these references for additional information:

1. Texas Instruments, *LP875701-Q1 Four-Phase 3-MHz 1-V 10-A DC/DC Buck Converter With Integrated Switches Datasheet* data sheet
2. Texas Instruments, *LP875701A-Q1 Technical Reference Manual*
3. Texas Instruments, *The LP875701Q1EVM (BMC043) Evaluation Module*

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