Application Report
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PCB Layout Guideline for Automotive LED Drivers

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ABSTRACT

PCB layout design for automotive applications requires stricter standards than industrial and personal electronics applications for such as EMC regulation, operating temperatures, and transient conditions. The considerations for these requirements at PCB design stage improves system performance and save the effort and cost of development at later stages. The purpose of this application note is to help users with basic ideas about PCB design for LED drivers with DC-DC converters. This document uses the LP8863-Q1 device and EVM design as examples and also shows generic rules and examples for better PCB design which can be applied across application areas. This document does not provide detailed theories and backgrounds of all guidelines described here.

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1 Typical Application Circuit of LP8863-Q1

The LP8863-Q1 application circuit in Figure 1 shows a common LED driver circuit for automotive applications with power-line FET, current sense resistors, inductor, boost input/output capacitors, switching FET, diode, capacitors for internal charge pump, and host interface. Additionally, an EMI filter was used on the LP8863-Q1 EVM to suppress common mode noise of the system.

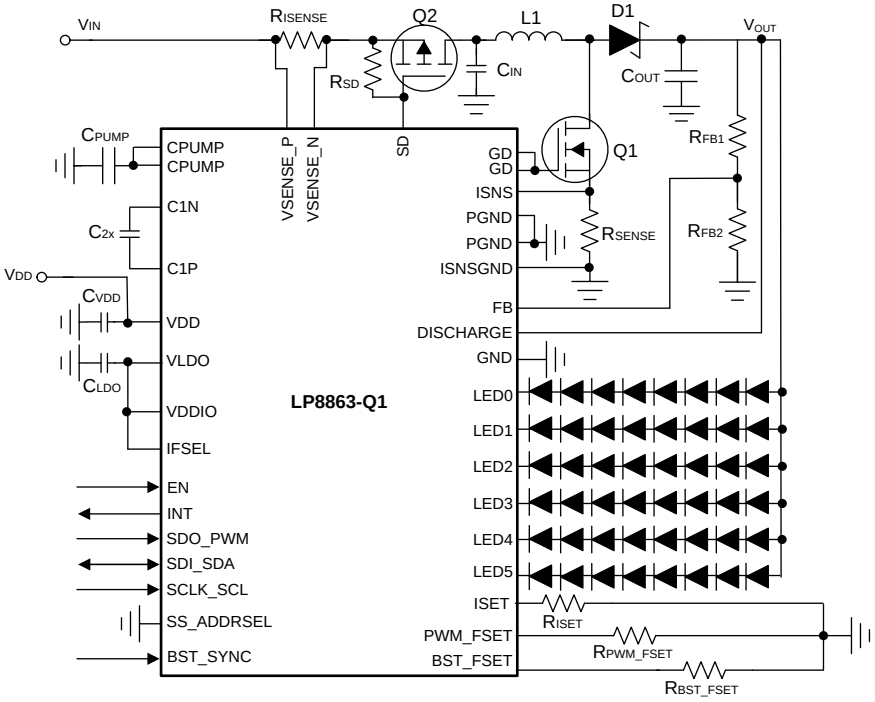


Figure 1. Simplified Schematic of LP8863-Q1

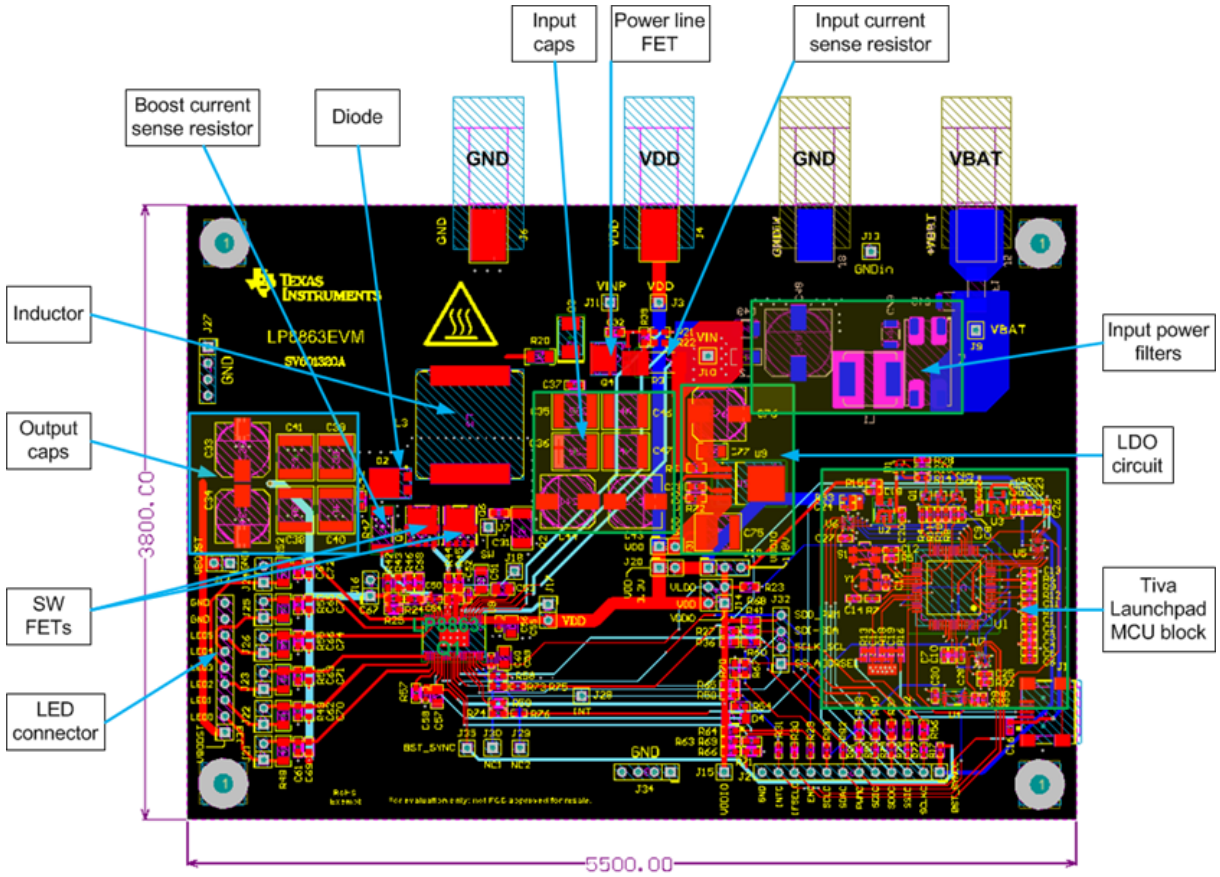


Figure 2. PCB Layout of LP8863-Q1 EVM

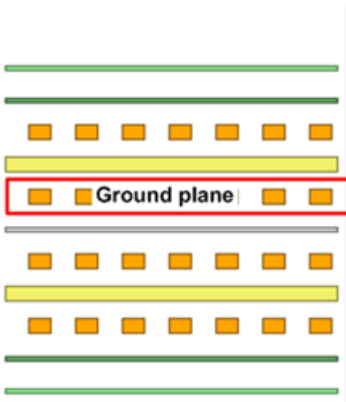
Figure 3. Top View of LP88663-Q1 EVM

2 Consideration of Critical Factors

The guidelines in this document are described starting from those with the most impact first for most of the application cases.

2.1 Layers of PCB

TI recommends 4 or more layers of PCB, if possible, to isolate noisy nodes from/to other parts of system PCB and to shorten GND path of each signal/power rail. Use one of the internal layers as a GND plane for this purpose. If only 2 layers are used, noise isolation may not be effective, and the GND path can be unnecessarily longer than 4 layers. 2-layer design must be prioritized between cost and performance. The LP8863-Q1 EVM uses 4 layer PCB — see stack information in Figure 4:



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)
Top Overlay	Overlay					
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Top Layer	Signal	Copper	1.4			
Dielectric1	Dielectric	Core	40	FR-4	4.8	
Signal Layer 1	Signal	Copper	1.4			
Dielectric 2	Dielectric	Prepreg	5		4.2	
Signal Layer 2	Signal	Copper	1.4			
Dielectric 3	Dielectric	Core	10		4.2	
Bottom Layer	Signal	Copper	1.4			
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Bottom Overlay	Overlay					

Figure 4. PCB Layer Stack of LP8863-Q1 EVM

- 1st layer (top) : signals/powers/GND mixed. All areas except for signals and power rails are covered with copper connected to GND to isolate the traces on it.
- 2nd layer (signal layer 1) : GND plane for both digital and power ground.
- 3rd layer (signal layer 2) : signals/GND mixed. All areas except for signals are covered with copper connected to GND to isolate the traces on it.
- 4th layer(Bottom) : signals/powers/GND mixed. All areas except for signals and power rails are covered with copper connected to GND to isolate the traces on it.

2.2 Current Loops

There are 2 main loops of boost current flow. Current loops generate a magnetic field which can interfere other circuitry of system. The strength of magnetic field is proportional to loop size; minimize loop size minimized, if possible. Figure 5 and Figure 6 show 1st and 2nd current loop. The first loop current flows from inductor, SW FET and to power ground. The second loop current flows from inductor, diode, output capacitor and to power ground. Each component must be placed as close as possible around boost controller(LED driver) and share same ground plane to reduce loop sizes.

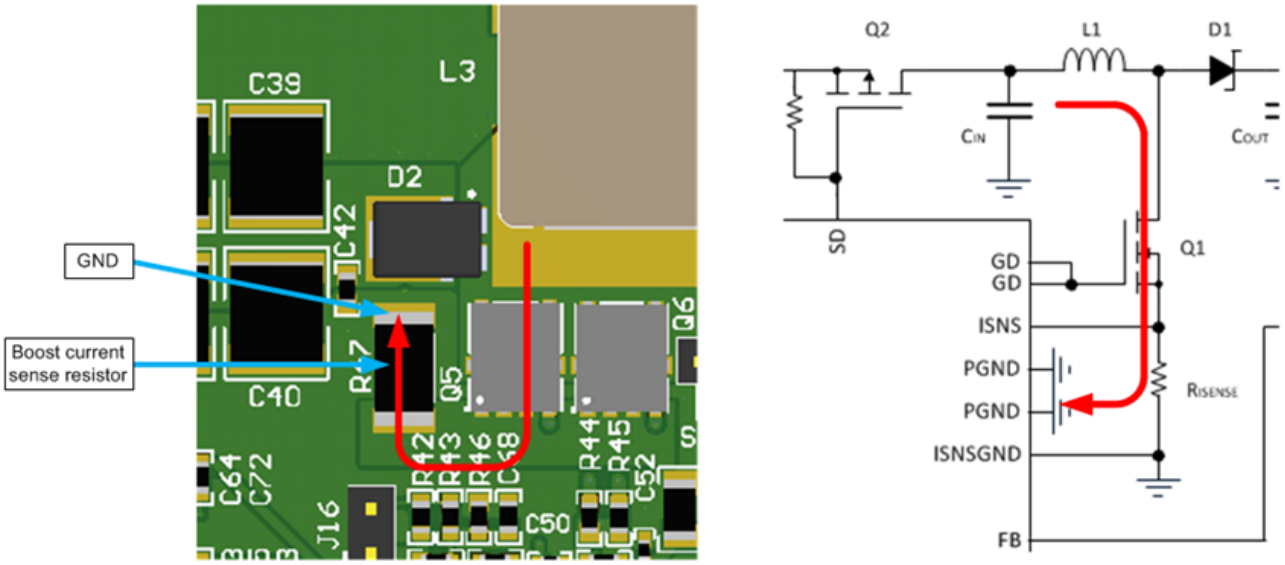


Figure 5. Switching Current Loop 1

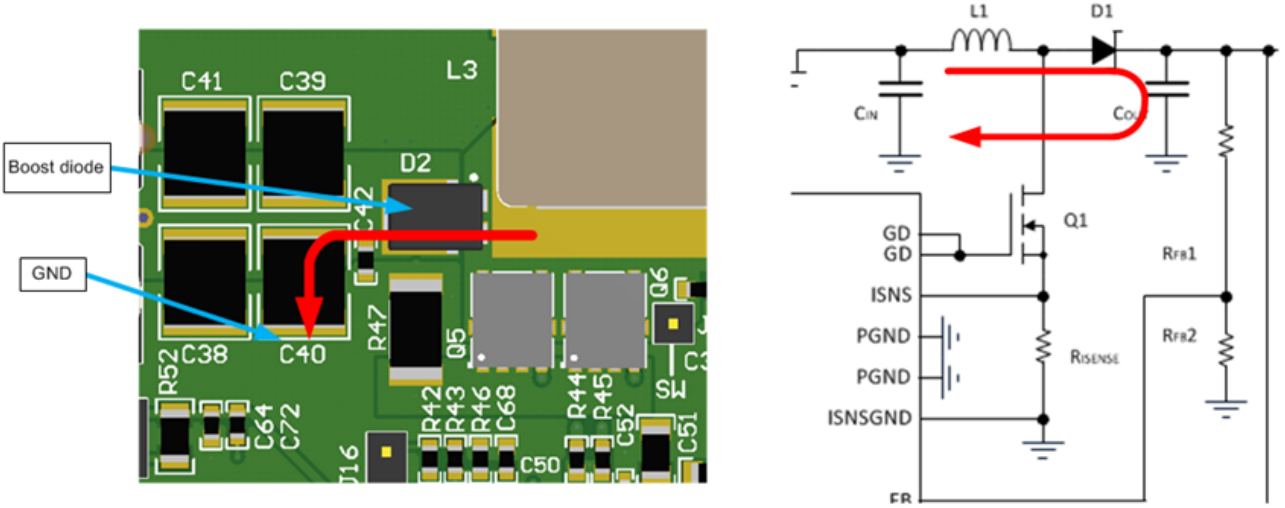


Figure 6. Switching Current Loop 2

Figure 7 shows main current flows and component placements. Power ground of input, switch, and boost output are all centered and each component has enough vias to connect to ground plane with shortest path.

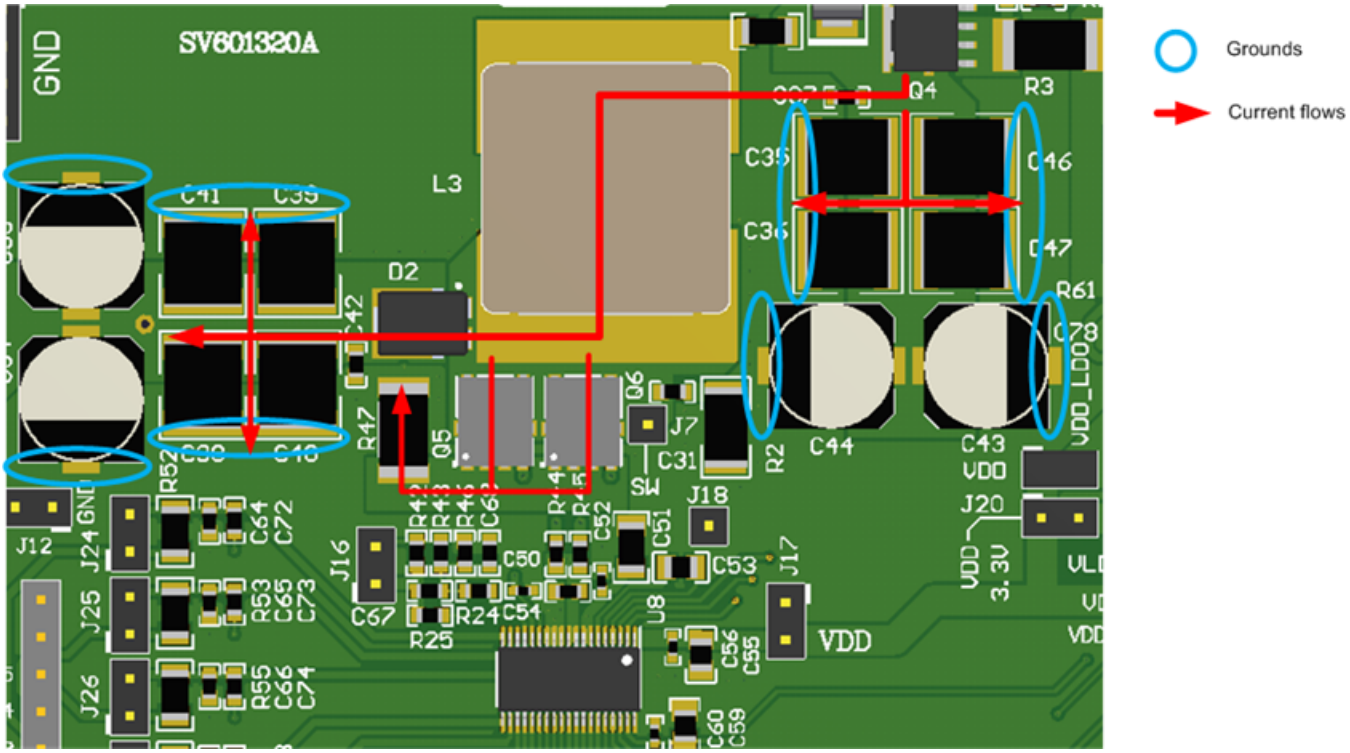


Figure 7. Current Flows of LP8863-Q1 EVM

3 Switching FET

3.1 Thermal Consideration

The switching FET has DC and AC power losses on it. DC loss is caused by the turnon resistance of the FET, which is proportional to switching current. This can be minimized by selecting a big enough FET with low R_{DSON} value. AC loss is caused by switching operation of the DC-DC converter and proportional to swing voltage, frequency and rise/fall time of switching. AC loss can be a critical factor of power loss especially at high switching frequencies, and there may be a limitation on selecting big enough or fast enough FET to reduce the loss with given operating conditions due to the limitation of FET performances.

Because of the limited FET capability and nature of DC-DC converter, thermal accumulation on switching FET is inevitable. Therefore, consideration for good thermal dissipation is required for PCB design. Figure 8 shows the switch node of the LP8863-Q1 EVM. Two switching FETs were used to dissipate the power loss of each one.

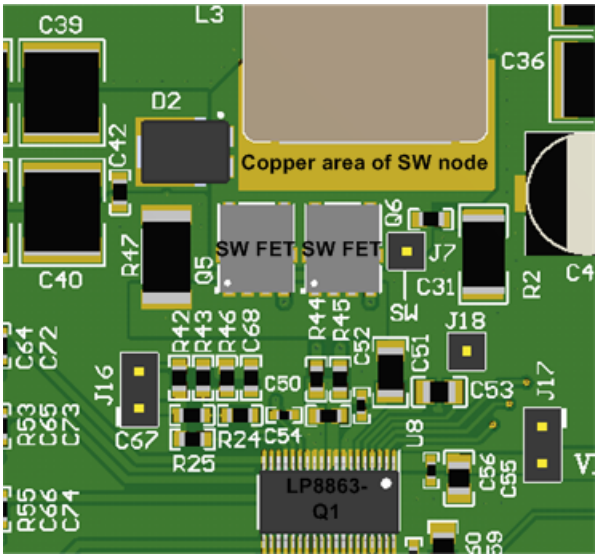


Figure 8. Copper Area of SW Node for Thermal Dissipation

Increasing switch node area must be done carefully as it may cause a couple of side effects.

1. Due to big copper area, parasitic capacitance of switch node is increased, thus increasing switching time, which results in higher switching power loss.
2. Large copper area can act like an antenna, which may affect EMC characteristics.

Therefore, there should be some trade-off for increasing copper area of switch node. In most cases, TI recommends an area a few times larger than switching the FET footprint for high switching frequency. For low switching frequency, such as a few hundred kHz, the switch-node area is not as critical to AC loss and thermal dissipation.

3.2 Consideration of Current Flow

3.2.1 Vias to Connect Switch Current Sense Resistor to Ground Plane

Switch current flows from switch FET to current sense resistor and to ground plane through vias. The path must be large enough for this current flow. Trace width can be calculated as explained in *Section 11*. Via count can be also calculated by current capacity of each via (see Equation 1):

$$\text{Current capacity(Aamp)} = k \times \text{Temp\_rise(°C)}^{b} \times \text{Area(mils2)}^{c} \quad (1)$$

where

- Area = pi × (inner_diameter+plating_thickness) × plating_thickness for IPC-2221 external layers: k = 0.048, b = 0.44, c = 0.725, plating_thickness(min) = 1 mil

A via of 8 mil(diameter) was used on the LP8863-Q1 EVM to connect sense resistor to ground plane. A reasonable estimate of the current capacity of this via is approximately 1.49 A for a 10°C increase. A total of 12 vias were used on the sense resistor ground of the LP8863-Q1 device, which support up to 17.88 A — large enough for a maximum switching current limit (approximately 10 A). Equation 1 can be used for any other high current paths requiring via connections.

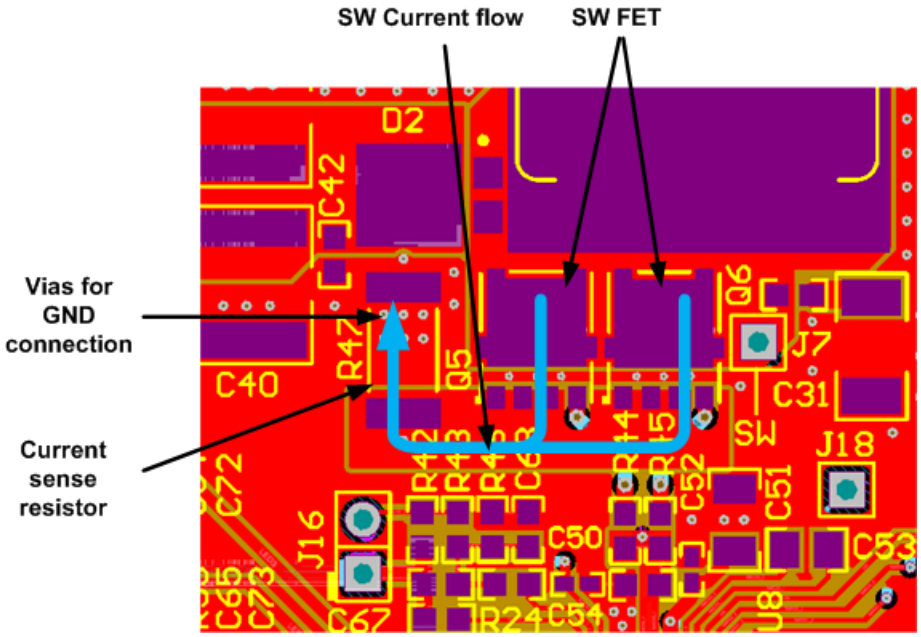


Figure 9. Vias for Ground Plane Connection

4 Isolation of Noisy (Switch) Node

Effective isolation of noisy node improves EMC characteristics of the system. Switch node of DC-DC converter can act as an antenna emitting high-frequency EMI. Surrounding this node with short ground paths effectively isolates the noise by removing coupling to other circuits and localize it forming smaller loops. Figure 10 shows that switching node is surrounded by polygon connected to ground layers with vias for short connection.

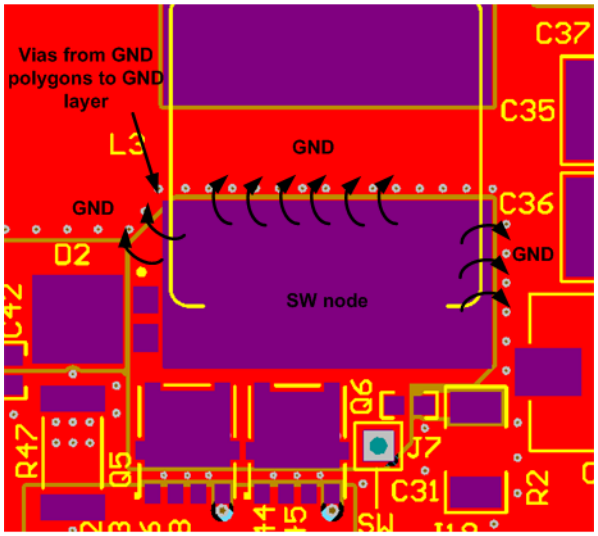


Figure 10. Isolation of Noisy (SW) Node for EMC Improvement

Figure 11. Localizing Noise Source to Form Smaller Current Loops

5 Trace of Gate-Drive Signal

The trace of gate drive signal for switching FET must be short and wide to reduce inductance and resistance to avoid ringing and slow rise/fall time. This is one of the most critical traces for boost control.

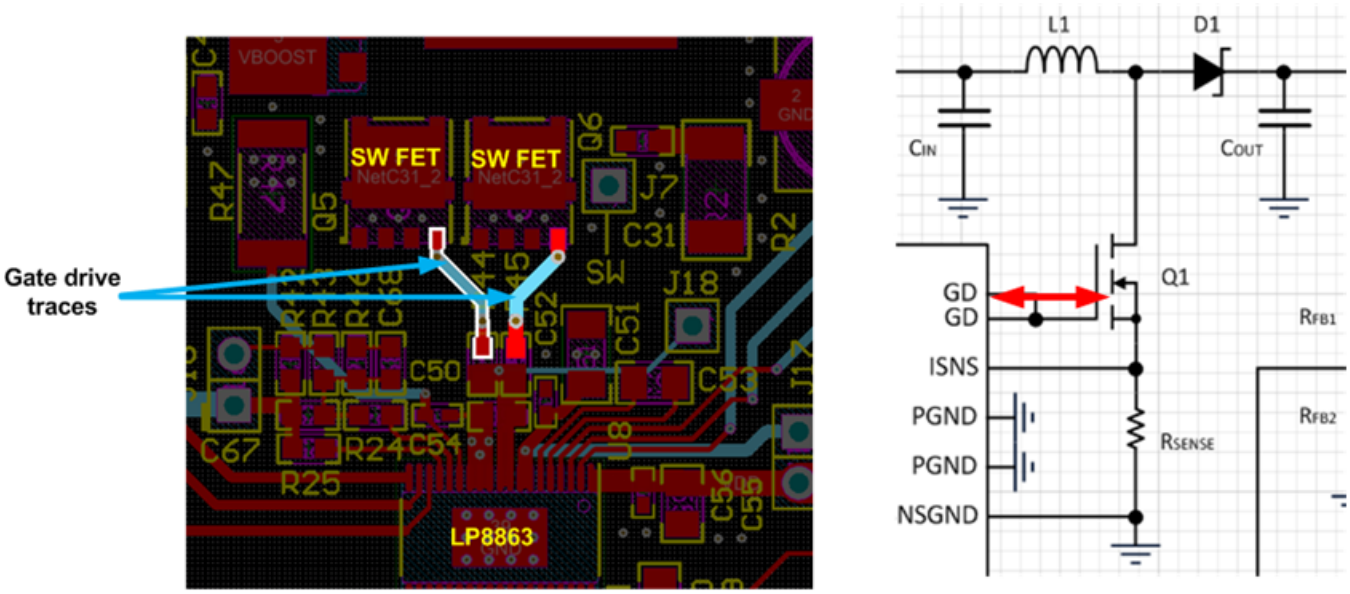


Figure 12. Gate-Drive Signal From LP8863-Q1 to SW FET

6 LED Driver (LP8863-Q1)

LED driver itself can have power loss by headroom voltage of LED string. If there are high voltage mismatches of total V_f of each LED string, the LED driver inputs with high headroom voltage (that is, the LED string with lowest total V_f) has high power loss. In order to avoid excessive thermal accumulation on the LED driver, its die-attach pad (DAP) must connected to GND plane with many vias and/or wide traces. The LP8863-Q1 EVM uses 12 20-mil (outer diameter) vias to connect DAP of the device to ground plane.

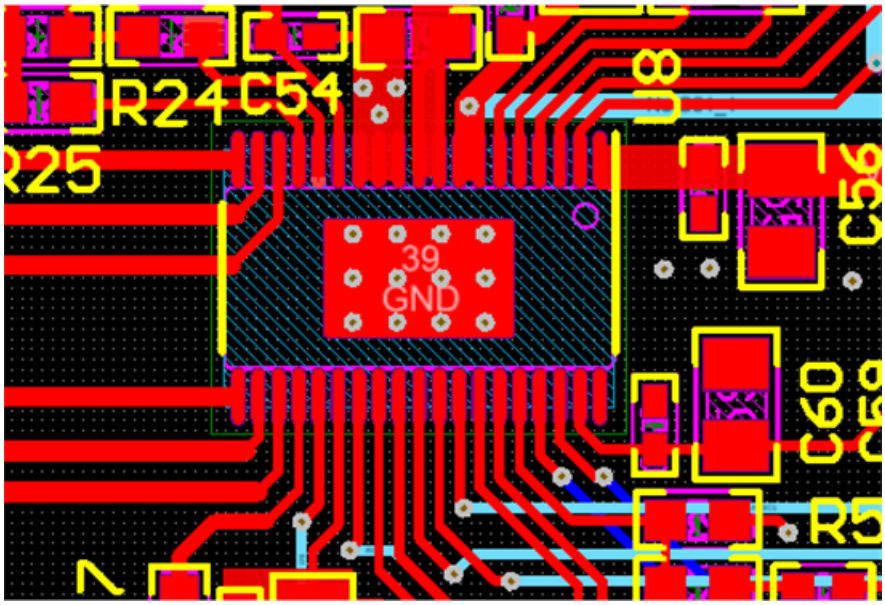


Figure 13. Vias from DAP of LP8863-Q1 to Ground Layer for Thermal Dissipation

Adding vias on the DAP helps reduce die temperature and makes enough current path for LED driver (DAP of LP8863-Q1 is LED ground). Thermal impedance of each via used on LP8863-Q1 EVB is estimated as approximately 26°C/W (see Equation 2), so use as many vias as required for expected power dissipation on LED driver and temperature requirement.

$$\theta_{cu\text{-}via} = L / (K \times \pi \times (D_0^2 - D_1^2) / 4 \quad (2)$$

where

- L = length of via
- K = thermal conductivity of copper(9W/in°C)
- D_0 = outer diameter of via(20 mil)
- D_1 = Inner diameter of via(8 mil)

7 Logic Power Input

The logic power input of LED driver may contain noises or ripples, which can disturb digital (or even analog) operation of LED drivers. Filter out noises or ripples before logic power is inputted to LED driver. Typically a few µF (for example, 0.1 µF) of capacitance is used as a low-pass filter, and these capacitors must be placed at nearest point to the input pin.

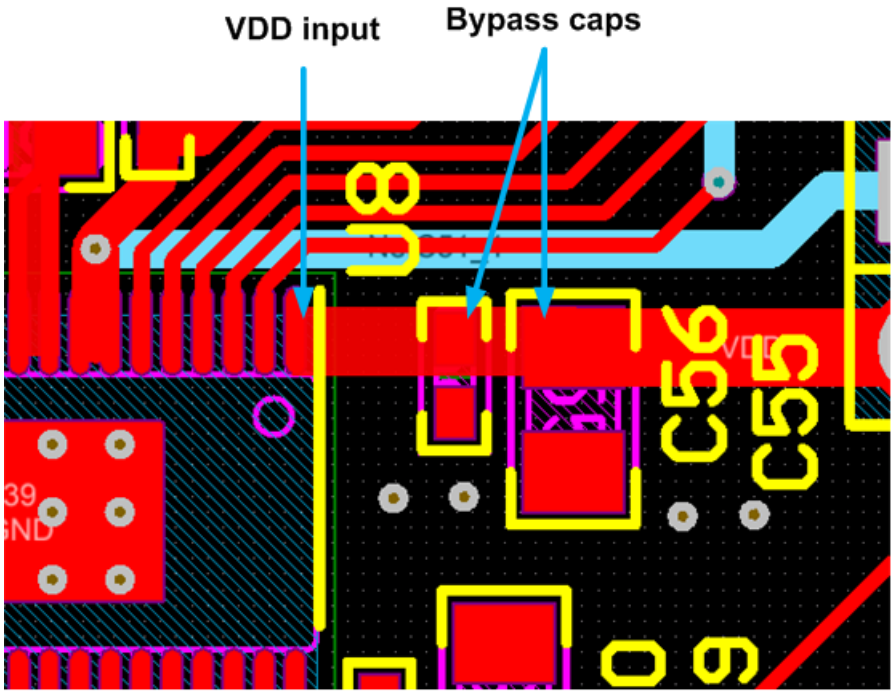


Figure 14. Bypass Capacitors of Logic Power Input

8 Trace of Boost Feedback Signal

The feedback signal of boost output is returned to LED driver (LP8863-Q1) for boost control loop. This connection must be isolated or not affected from external noise or crosstalk from neighboring signals so that the stable boost control is not disturbed. As shown in Figure 15, feedback trace is isolated from boost-switch node by ground polygon and vias (to ground layer) on the top layer and buried in the inner layer where ground layer is in between.

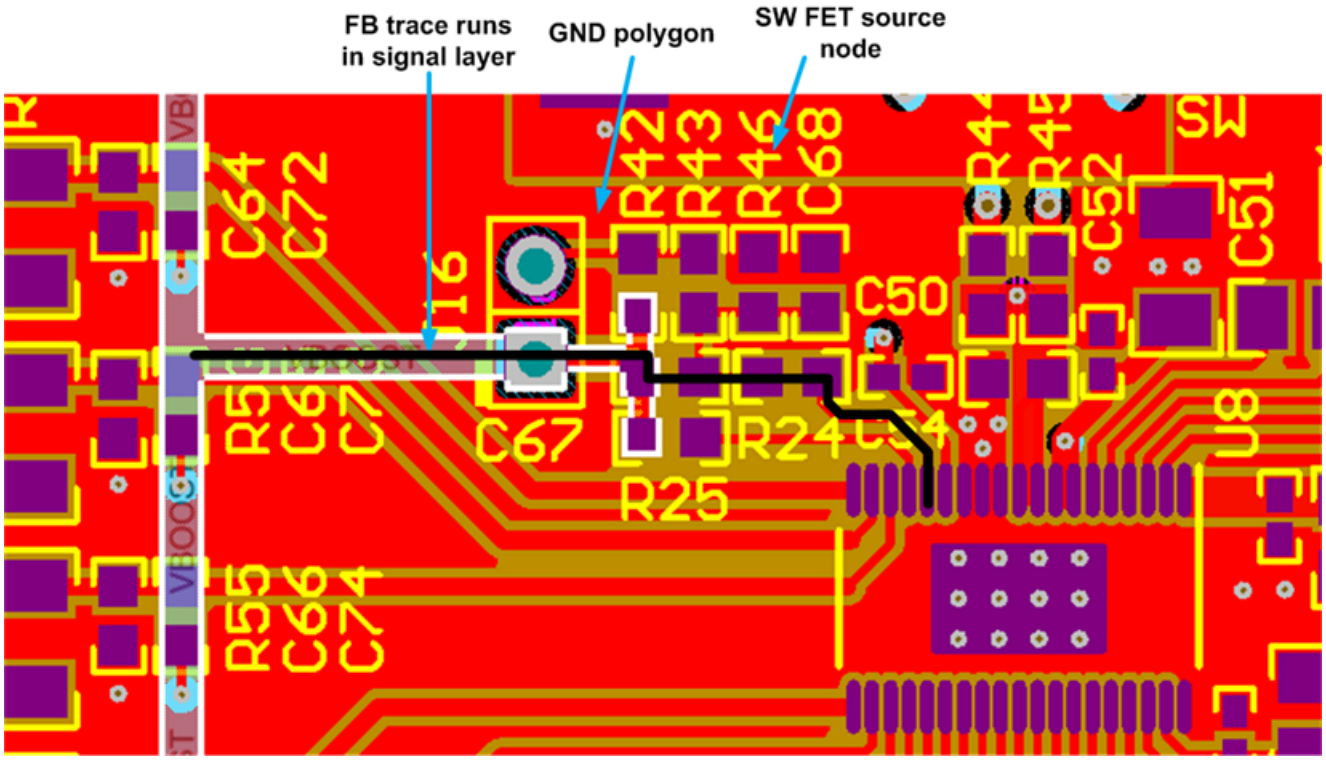


Figure 15. Trace for Boost Feedback

9 Charge Pump

The LP8863-Q1 has an internal charge pump to double the gate-drive voltage of switch FET from external low voltage power input. There must be at least 2 capacitors for charge pump. One is flying capacitor for charge pump switching, and another one is output capacitor. Place both at the nearest location from the charge-pump controller (LP8863-Q1) to avoid unnecessary noise and ringing by parasitics. The trace width of flying capacitor and output capacitor must be able to handle maximum driving current of charge pump not causing excessive voltage drop and heat. Refer to *Section 11* for trace width calculation for thermal control.

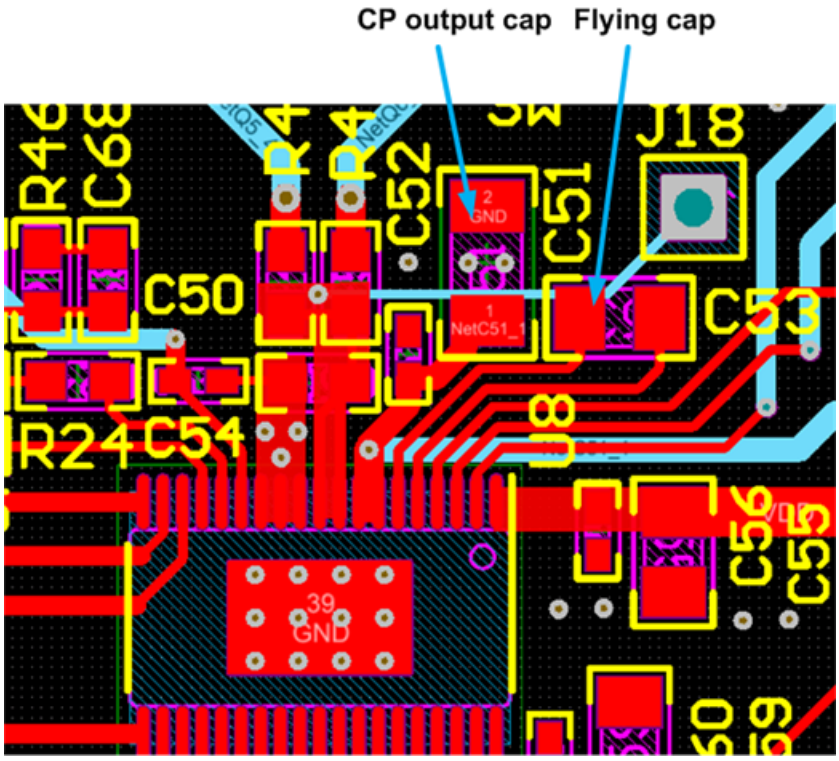


Figure 16. Capacitor Locations of Charge Pump

10 Power-Line FET

A power-line FET may or may not be used for LP8863-Q1 applications. If this FET is not used, trace width must calculated to be wide enough to flow the current without excessive temperature increase, which is discussed *Section 11*. If a power-line FET is used, a trace much wider than the FET width must be used is required to dissipate heat from power loss on power-line FET. Power dissipation on this FET can be simply calculated by $P = I_{IN}^2 \times R_{DSON}$. Table 1 shows the thermal parameters of power-line FET used on LP8863-Q1 EVM. Junction temperature = $R_{\theta JA} \times P$ + ambient temperature when there is one-inch 2 of PCB area as specified in the datasheet of FET. If die temperature is expected higher than maximum junction temperature supported by the FET, the copper area of the power-line FET (thermal pad side or drain) must be increased.

Table 1. Thermal Resistance Ratings

SYMBOL	PARAMETER	LIMIT	UNIT
$R_{\theta JA}$	Junction-to-Ambient	65	°C/W
$R_{\theta JC}$	Junction-to-Case (drain)	1.8	°C/W

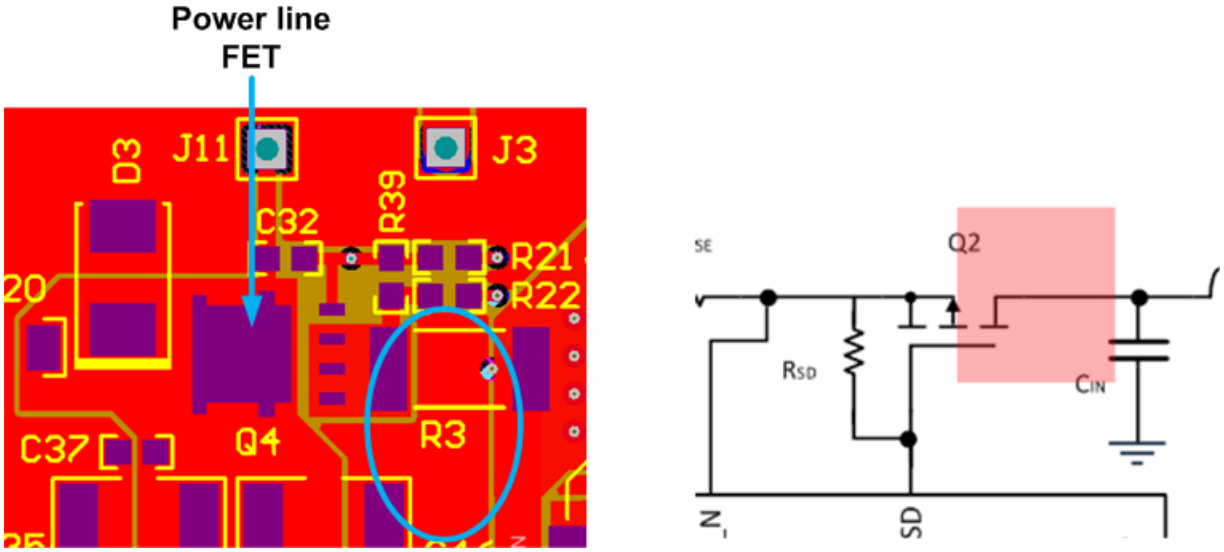


Figure 17. Recommended PCB Pad for Power-Line FET

11 Trace of Boost-Power Input

Input trace of boost power must be wide enough to keep temperature low enough or down to given limits. The minimum required trace width required can be calculated by Equation 3.

$$\text{Width} = (\text{Current[Amps]} / (k \times (\text{Temp\_Rise[°C]})^{b}))^{(1/c)} / \text{Thickness , in mils} \quad (3)$$

where

- For IPC-2221 internal layers: k = 0.024, b = 0.44, c = 0.725
- For IPC-2221 external layers: k = 0.048, b = 0.44, c = 0.725

Maximum input current of LP8863-Q1 is 11.5 A, thickness of this power trace is 1.4 mil, and width is approximately 260 mil. Therefore, expected temperature increase at maximum input current is approximately 15°C. This temperature increase must not be higher than expected temperature increase of each boost component.

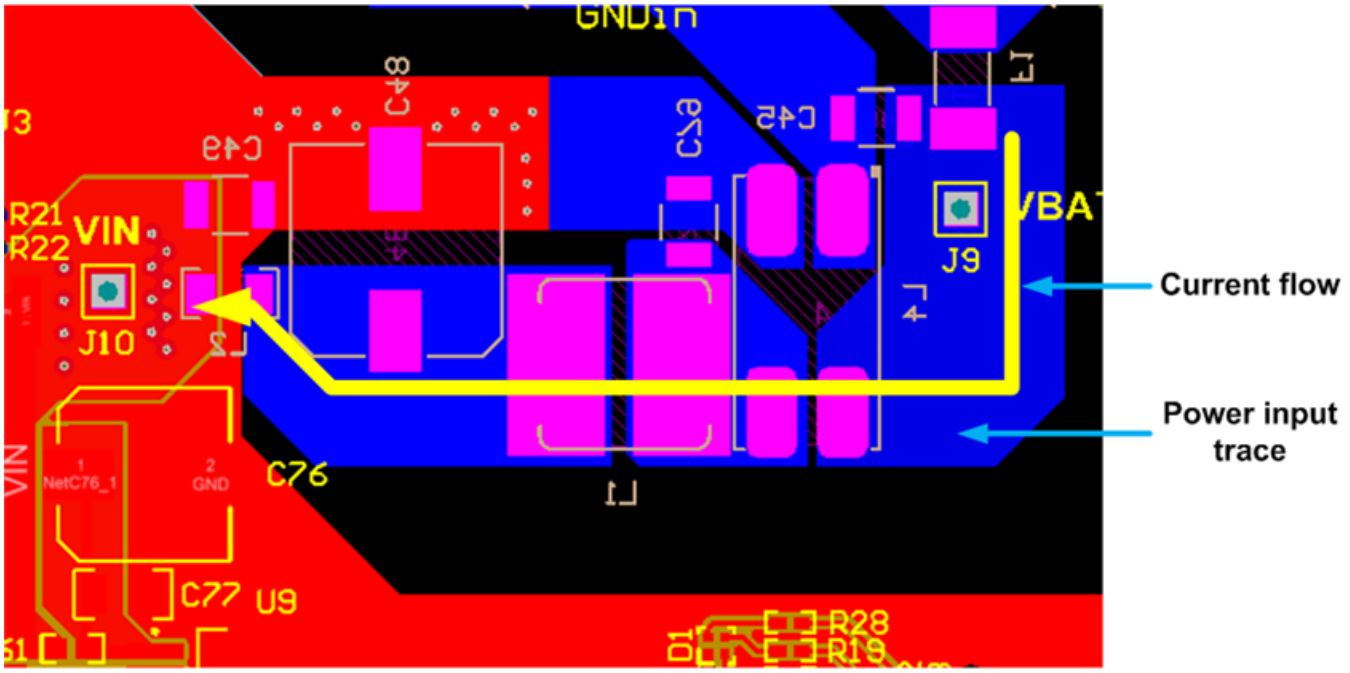


Figure 18. Boost Input Power (V_{IN}) Trace

Apply the same consideration to calculate the trace width from switch FET to ground (via current sense resistor).

12 Placement of Capacitors

Noise from switch-node propagates through diode and output traces, and high-frequency noise tends to generate EMI easily at short antenna length. This high frequency noise is made from ringing or transient condition of switching and frequency of it can be hundreds of MHz to a few GHz. A few inches of output traces may make a good antenna condition for this frequency, so filtering out this frequency range first is more effective for EMI reduction. For this purpose, TI recommends placing smaller-value capacitors to larger-value capacitors from switching node as shown in Figure 19.

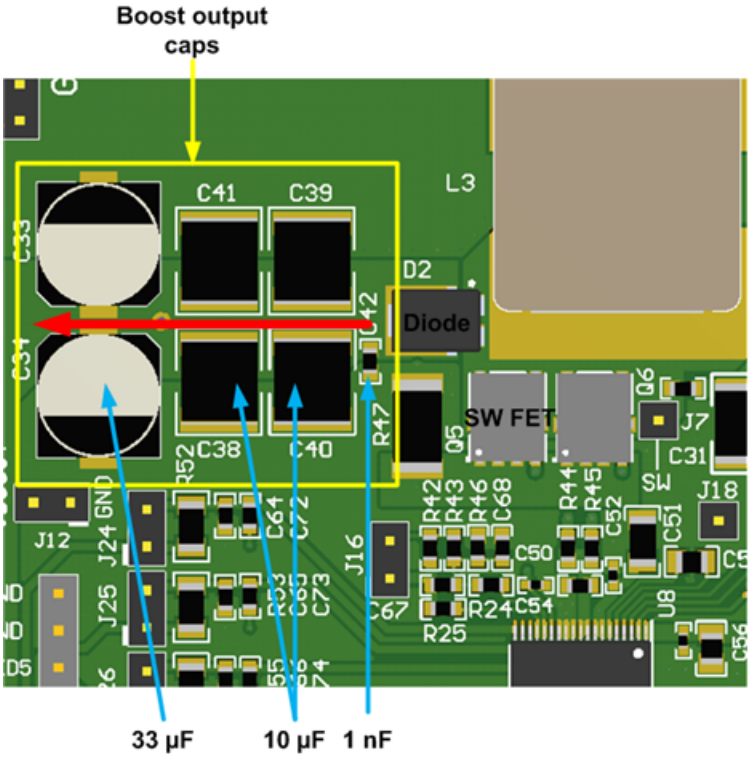


Figure 19. Recommended Placement of Boost Output Capacitors

13 Trace of Digital Control Signals

In most of cases, special routing for digital control signals of LED drivers is not required as digital-control frequencies are fairly low (maximum tens of MHz); however, sudden impedance change by acute angles of traces or thickness change at single point may cause antenna conditions for high frequency factors such as ringing or ripples. Figure 20 shows recommended routing of the traces.

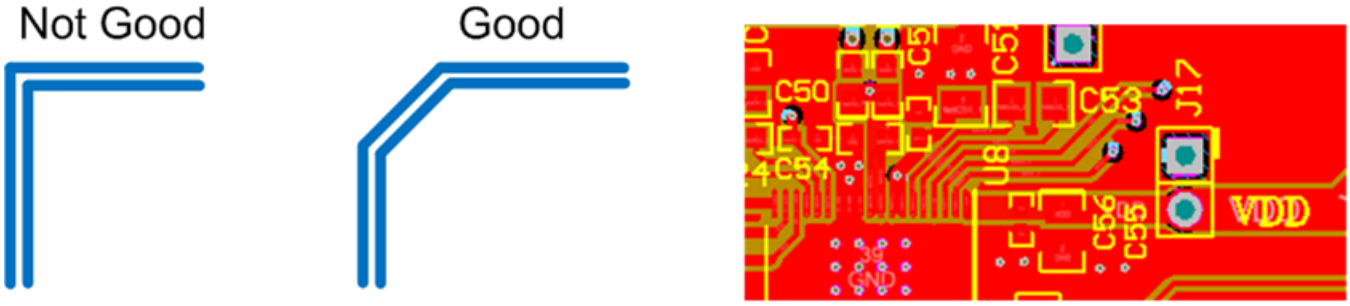


Figure 20. Recommended Trace Routing of Digital Signals

14 Summary

PCB design of high-power LED drivers is becoming more critical due to the the requirements of high-switching frequency and high DC-DC current. All requirements may not be satisfied or supported by the limitation of the components and application condition themselves, but careful consideration of PCB layout widens the range of supported applications and improves stability of the system. Following the generic rules introduced in this document such as smaller current loop, largest trace widths possible, proper thermal dissipation area, isolation of noisy node, and proper placement of components will contribute a better PCB design and an easier system development.

15 References

- Thermal Considerations for Surface Mount Layouts, Charles Mauney, Texas Instruments
- *PCB Design Guidelines for Reduced EMI*, Novemeber 1999
- Reference designer calculators, http://www.referencedesigner.com/cal/cal_06.php
- PCB via calculator, http://circuitcalculator.com/wordpress/2006/03/12/pcb-via-calculator/

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