AN-1723 LM5067 Evaluation Board

1 Introduction

The LM5067EVAL evaluation board provides the design engineer with a fully functional hot swap controller board designed for negative voltage systems. This board contains an LM5067-2, the auto restart version of this IC. This document describes the various functions of the board, how to test and evaluate it, and how to change the components for a specific application. The LM5067 data sheet is available from www.ti.com.

The board's specifications are:

- Input voltage range: -9V to -78V maximum, limited by the transient suppressor (Z1)
- Current limit: 5 Amps, ±12%
- Q1 Power limit: 40W
- UVLO Thresholds: 34.5V, ±5% and 32.4V, ±2%
- OVLO Thresholds: 77.7V, ±3% and 75.6V, ±5%
- Insertion delay: 1470 ms
- Fault timeout period: 104 ms
- Restart time: 21 seconds
- Size: 4.0" x 1.4"

2 Board Configuration

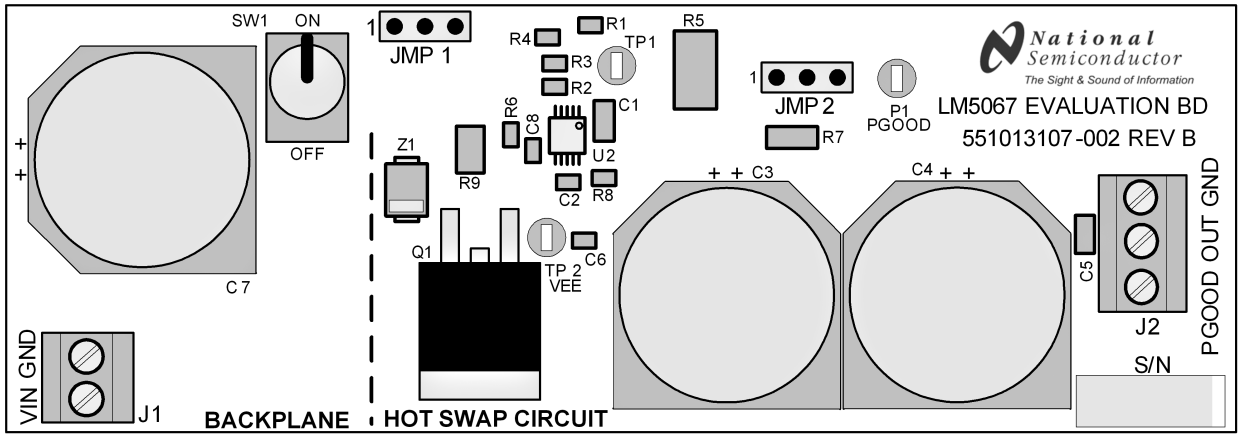


Figure 1. Evaluation Board - Top Side

The LM5067 evaluation board is shown in Figure 1, and the schematic is shown in Figure 2. The "BACKPLANE" section, at the left end of the board, represents the backplane voltage source. The vertical dashed line is the boundary between the backplane voltage source and the hot swap circuit input. In other words, it represents the edge connector in a card cage system. The toggle switch (SW1) provides a means to "connect" and "disconnect" the hot swap circuit from the backplane voltage source.

The circuitry to the right of the vertical dashed line is the hot swap circuit. The system voltage is to be connected to the input terminal block (J1). The external load is to be connected to the output terminal block (J2). Capacitors C3 and C4 represent capacitance, which is typically present on the input of the load circuit, and are present on this evaluation board so the turn-on characteristics of the LM5067 can be tested without having to connect a load.

For a hot swap circuit to function reliably, capacitance is needed on the supply side of the system connector (C7). Its purpose is to minimize voltage transients that occur whenever the load current changes or is shut off. If the capacitance is not present, wiring inductance in the supply lines generate a voltage transient at shutoff, which can exceed the absolute maximum rating of the LM5067, resulting in its destruction.

The LM5067EVB is supplied with pins 2-3 jumpered on JMP1, and pins 1-2 jumpered on JMP2.

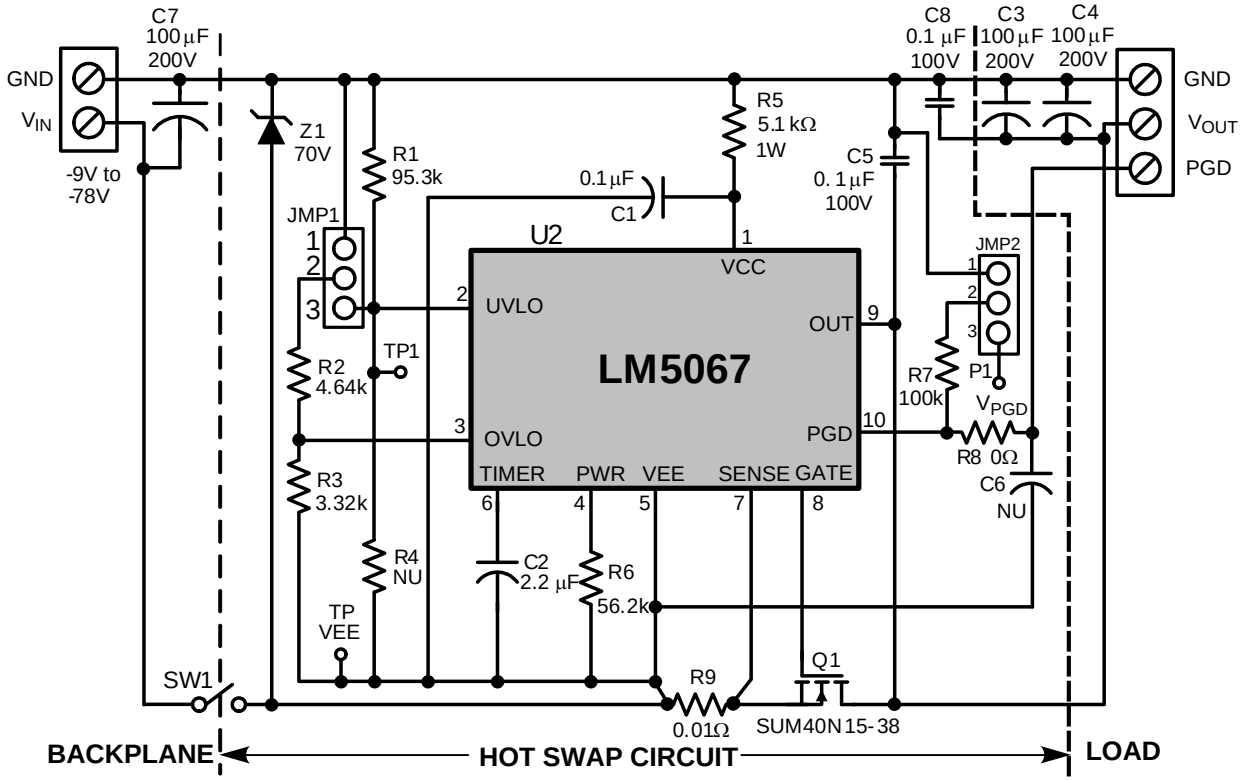


Figure 2. Evaluation Board Schematic

3 Theory of Operation

The LM5067 provides intelligent control of the power supply connections of a load that is to be connected to a live power source. The two primary functions of a hot swap circuit are in-rush current limiting during turn-on, and monitoring of the load current for faults during normal operation. Additional functions include under-voltage lock-out (UVLO) and over-voltage lock-out (OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a defined range, power limiting in the series pass FET (Q1) during turn-on, and a power good logic output (PGD) to indicate the circuit status.

Upon applying the input voltage to the LM5067 (for example, SW1 is switched on), Q1 is initially held off for the insertion delay (≅1470 ms) to allow ringing and transients at the input to subside. At the end of the insertion delay, if the input voltage at VIN is between the UVLO and OVLO thresholds, Q1 is turned on in a controlled manner to limit the in-rush current. If the in-rush current were not limited during turn-on, the current would be high (very high!) as the load capacitors (C3, C4) charge up, limited only by the surge current capability of the voltage source, C7's characteristics, and the wiring resistance (a few milliohms). That very high current could damage the edge connector, PC board traces, and possibly the load capacitors receiving the high current. Additionally, the dV/dt at the load's input is controlled to reduce possible EMI problems.

The LM5067 limits in-rush current to a safe level using a two step process. In the first portion of the turn-on cycle, when the voltage differential across Q1 is highest, Q1's power dissipation is limited to a peak of 40W by monitoring its drain current (the voltage across R9) and its drain-to-source voltage. Their product is maintained constant by controlling the drain current as the drain-to-source voltage decreases (as the output voltage increases). This is shown in the constant power portion of Figure 3 where the drain current is increasing to I_{LIM}. When the drain current reaches the current limit threshold (5 Amps), it is then maintained constant as the output voltage continues to increase. When the output voltage reaches the input voltage (V_{DS} decreases to near zero), the drain current then reduces to a value determined by the load. Q1's gate-to-source voltage then increases to ≅13V above VEE. The circuit is now in normal operation mode.

Monitoring of the load current for faults during normal operation is accomplished using the current limit circuit described above. If the load current increases to 5 Amps (50 mV across R9), Q1's gate is controlled to prevent the current from increasing further. When current limiting takes effect, the fault timer limits the duration of the fault. At the end of the fault timeout period (≅104 ms) Q1 is shut off, denying current to the load. The LM5067-2 then initiates a restart every 21 seconds. The restart consists of turning on Q1 and monitoring the load current to determine if the fault is still present. After the fault is removed, the circuit powers up to normal operation at the next restart.

In a sudden overload condition (the output is shorted to ground), it is possible the current could increase faster than the response time of the current limit circuit. In this case, the circuit breaker sensor shuts off Q1's gate rapidly when the voltage across R9 reaches ≅100 mV. When the current reduces to the current limit threshold, the current limit circuitry then takes over.

The PGD logic level output is low during turn-on, and switches high when the output voltage at OUT has increased to within 1.23V of the input voltage, signifying the turn-on procedure is essentially complete. If the OUT voltage magnitude decreases more than 2.5V with respect to V_{IN} due to a fault, PGD switches low. The high level voltage at PGD can be any appropriate voltage up to 80V above V_{EE}, and can be higher or lower than system ground.

The UVLO and OVLO thresholds are set by resistors R1-R3. The UVLO and OVLO thresholds are reached when the voltage at the UVLO and OVLO pins each reach 2.5V, respectively. The internal 22 µA current sources provide hysteresis for each of the thresholds.

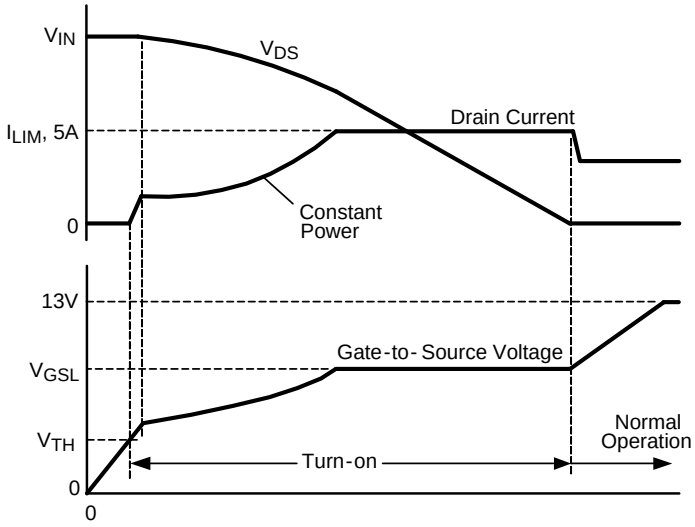


Figure 3. Power Up Using Power Limit and Current Limit

4 Board Layout and Probing Cautions

Figure 1 shows the placement of the circuit components. The following should be kept in mind when the board is powered:

- High voltage, equal to VIN, is present on C3, C4, C7, R9, Q1, and various points within the circuit. Use CAUTION when probing the circuit to prevent injury, as well as possible damage to the circuit.
- At maximum load current (5A), the wire size and length used to connect the power source and the load become important. The wires connecting this evaluation board to the power source SHOULD BE TWISTED TOGETHER to minimize inductance in those leads. The same applies for the wires connecting this board to the load. This recommendation is made in order to minimize high voltage transients from occurring when the load current is shut off.

5 Board Connections/Startup

The input voltage source is connected to the J1 connector (ground to GND, negative supply voltage to VIN). The load is connected to the J2 connector at the GND and OUT terminals. USE TWISTED WIRE. A voltmeter should be connected to the input terminals, and one to the output terminals. The input current can be monitored with an ammeter or current probe. To monitor the status of the PGD output, connect a voltmeter from PGOOD to GND, or from PGOOD to the VEE test point (near Q1).

Put the toggle switch to the ON position. Increase the input voltage gradually. When the UVLO threshold is reached (≅-34.5V) Q1 is switched on and the output voltage increases. If the input current is viewed on an oscilloscope, the waveform will be similar to that shown in Figure 3, and will settle at the value determined by the load and the input voltage. The turn-on timing depends on the input voltage, power limit setting, current limit setting, load capacitance, and the final load current, and is between ≅3 ms with no load current, and ≅16 ms with a 4A load current with Vin = -36V, see Figure 8 and Figure 9.

6 Circuit Parameter Changes

6.1 Current Limit

The current limit threshold is set by R9 according to Equation 1:

$$I_{LIM} = 50 \text{ mV}/R9 \quad (1)$$

If the load current increases such that the voltage across R9 reaches 50 mV, the LM5067 then modulates Q1's gate to limit the current to that level. This evaluation board is supplied with a 10 mΩ resistor for R9, resulting in a current limit of 5A. To change the current limit threshold replace R9 with a resistor of the required value and power capability.

6.2 Power Limit

The maximum power dissipated in Q1 during turn-on, or due to a fault, is limited by R9 and R6 according to Equation 2:

$$P_{FET(LIM)} = \frac{R6}{1.42 \times 10^5 \times R9} \quad (2)$$

With the components supplied on the evaluation board, $P_{FET(LIM)}$ = 40W. During turn-on, when the voltage across Q1 is high, its gate is modulated to limit its drain current so the power dissipated in Q1 does not exceed 40W. As the drain-to-source voltage decreases, the drain current increases, maintaining the power dissipation constant. When the drain current reaches the current limit threshold set by R9 (5A), the current is then maintained constant until the output voltage reaches its final value. The current then decreases to a value determined by the load, see Figure 3, Figure 8, and Figure 9.

Each time Q1 is subjected to the maximum power limit conditions it is internally stressed for a few milliseconds. For this reason, the power limit threshold must be set lower than the limit indicated by the FET's SOA chart. In this evaluation board, the power limit threshold is set at 40W, compared to ≅150W limit indicated in the Vishay SUM40N15-38 data sheet. The FET manufacturer should be contacted for more information on this subject.

6.3 Insertion Time

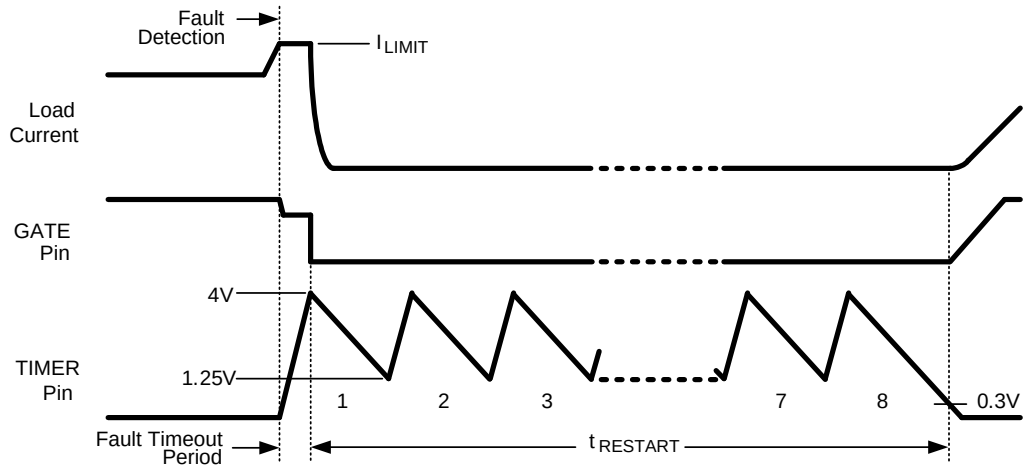
The insertion time starts when the voltage across the LM5067 (VCC - VEE) reaches 7.7V, and its duration is equal to:

$$t_{INSERTION} = C2 \times 6.67 \times 10^5 \quad (3)$$

During the insertion time, Q1 is held off regardless of the voltage at VIN. This delay allows ringing and transients at VIN to subside before the input voltage is applied to the load via Q1. The insertion time on this evaluation board is ≅1470 ms, see Figure 7.

7 Fault Detection and Restart

If the load current increases to the fault level (the current limit threshold, 5A), an internal current source charges the timing capacitor at the TIMER pin. When the voltage at the TIMER pin reaches 4.0V above VEE, the fault timeout period is complete, and the LM5067 shuts off Q1. The restart sequence then begins, consisting of seven cycles at the TIMER pin between 4.0V and 1.25V, as shown in Figure 4. When the voltage at the TIMER pin reaches 0.3V during the eighth high-to-low ramp, Q1 is turned on. If the fault is still present, the fault timeout period and the restart sequence repeat.



NOTE: Voltages are with respect to VEE

Figure 4. Fault Timeout and Restart Sequence

The fault timeout period and the restart timing are determined by the TIMER capacitor according to Equation 4 and Equation 5:

$$t_{FAULT} = C2 \times 4.7 \times 10^4 \quad (4)$$

$$t_{RESTART} = C2 \times 9.4 \times 10^6 \quad (5)$$

The waveform at the TIMER pin can be monitored at the test pad located at the lower left corner of C2, above TP2. In this evaluation board, the fault timeout period is ≅104 ms, and the restart time is ≅21 seconds, see Figure 10 and Figure 11.

8 UVLO/OVLO Input Voltage Thresholds

As supplied, the input voltage UVLO thresholds on this evaluation board are approximately 34.5V increasing, and 32.4V decreasing. The OVLO thresholds are approximately 77.7V increasing, and 75.6V decreasing. The four thresholds are determined by resistors R1-R4. The threshold voltage at each pin is 2.50V, and internal 22 µA current sources provide hysteresis for each threshold. For more details, see the device-specific data sheet.

8.1 Option A

This evaluation board is supplied with the jumper at JMP1 on pins 2-3, resulting in the configuration shown in Figure 5.

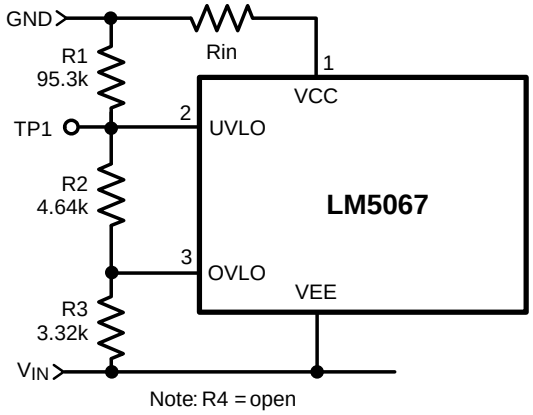


Figure 5. UVLO, OVLO Inputs (Option A)

To change the thresholds in this configuration, resistors R1-R3 are calculated using the following procedure:

- Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL}).
- Choose the upper OVLO threshold (V_{OVH})
- The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If V_{OVL} must be accurately defined in addition to the other three thresholds, see Section 8.2.

The resistors are calculated as follows:

$$R1 = \frac{V_{UVH} - V_{UVL}}{22\ \mu A} \quad (6)$$

$$R3 = \frac{2.5V \times R1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 2.5V)} \quad (7)$$

$$R2 = \frac{2.5V \times R1}{(V_{UVL} - 2.5V)} - R3 \quad (8)$$

The lower OVLO threshold is calculated from Equation 9:

$$V_{OVL} = [(R1 + R2) \times (\frac{(2.5V)}{R3} - 22\ \mu A)] + 2.5V \quad (9)$$

8.2 Option B

If all four thresholds must be determined accurately, move the jumper at JMP1 to pins 1-2, and add R4, resulting in the configuration shown in Figure 6, see the caution below.

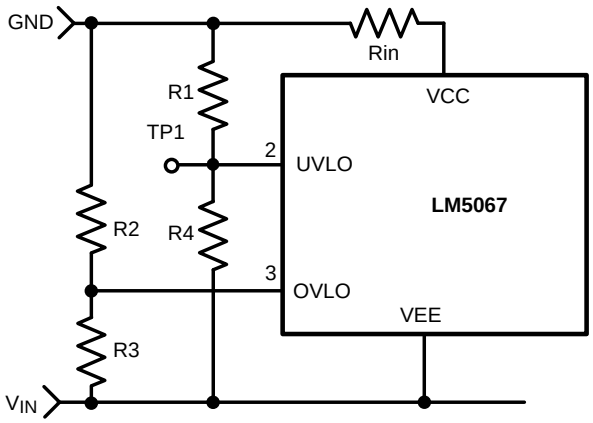


Figure 6. UVLO, OVLO Inputs (Option B)

The four resistor values are calculated as follows:

- Choose the upper and lower UVLO thresholds (V_{UVH}) and (V_{UVL}).

$$R1 = \frac{V_{UVH} - V_{UVL}}{22\ \mu A} \quad (10)$$

$$R4 = \frac{2.5V \times R1}{(V_{UVL} - 2.5V)} \quad (11)$$

- Choose the upper and lower OVLO threshold (V_{OVH}) and (V_{OVL}).

$$R2 = \frac{V_{OVH} - V_{OVL}}{22\ \mu A} \quad (12)$$

$$R3 = \frac{2.5V \times R2}{(V_{OVH} - 2.5V)} \quad (13)$$

CAUTION

Before moving the jumper at JMP1 to pins 1-2 for Section 8.2, the resistor values must be recalculated to avoid damaging the LM5067. The Absolute Maximum Rating for the OVLO and UVLO pins is 17V above VEE. If R4 is not installed, the maximum rating for the UVLO pin will be reached when Vin = -17V. With the supplied values for R2 and R3, the maximum rating for the OVLO pin will be reached when Vin = -40V.

8.3 Option C

The OVLO function can be disabled by removing the jumper from JMP1. The UVLO thresholds are set by R1 and R4 using the procedure in Section 8.2.

9 Shutdown

With the circuit in normal operation, the LM5067 can be shutdown by connecting the UVLO pin to VEE. On this evaluation board, test point TP1 can be connected to the VEE test point for this purpose.

10 Power Good Output

The PGOOD logic output provides an indication of the circuit's condition. This output is high when the circuit is in normal operation - the OUT voltage is within 1.25V of V_{IN}. PGOOD is low when the circuit is shutdown, either intentionally or due to a fault. PGOOD is also high when VIN is less than 2.

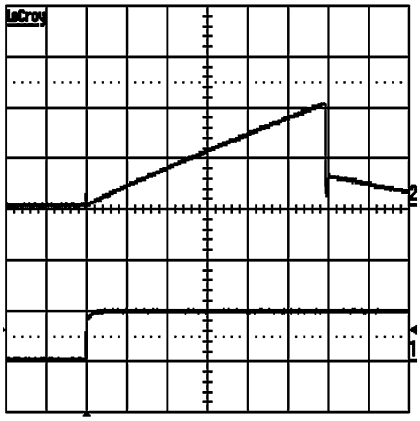
This EVB is supplied with pins 1-2 jumpered on JMP2, powering the PGD pin from ground through a 100 kΩ pull-up resistor. To change the high level PGOOD voltage, move the jumper on JMP2 to pins 2-3, and supply the appropriate pull-up voltage wit respect to VEEto terminal P1 (located next to JMP2). If the UVLO pin is taken low to disable the LM5067, PGOOD switches low within 10 µs without waiting for the OUT voltage to change.

If a delay at the PGOOD output is desired, a resistor and capacitor can be added at positions R8 and C6.

11 LM5067-1 Latch Version

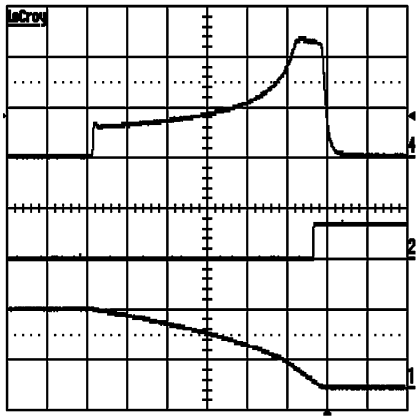
The LM5067-2 supplied on this evaluation board provides a restart attempt after a fault detection, as described above. The companion Hot-Swap IC, the LM5067-1, latches off after a fault detection, with external control required for restart. Restart is accomplished by momentarily taking the UVLO pin within 2.5V of VEE, or by removing and re-applying the input voltage at VIN. Contact the nearest Texas Instruments sales office to obtain samples of the LM5067-1.

12 Performance Characteristics



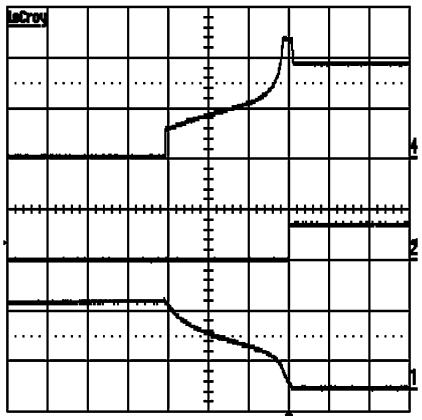
Horizontal Resolution: 200 ms/div
Trace 2: TIMER Pin, 2V/div
Trace 1: Vin, 50V/div (shown inverted 0 to -48V)
Ct = 2.2 µF
Voltages are respect to VEE

Figure 7. Insertion Time Delay



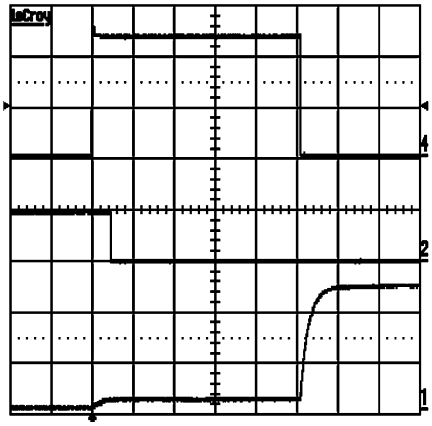
Horizontal Resolution: 0.5 ms/div
Trace 4: Input Current, 2A/div
Trace 2: PGD Pin, 50V/div
Trace 1: Vout, 20V/div
Vin = -36V
Voltages are respect to VEE

Figure 8. Turn-On Sequence With Zero Load Current



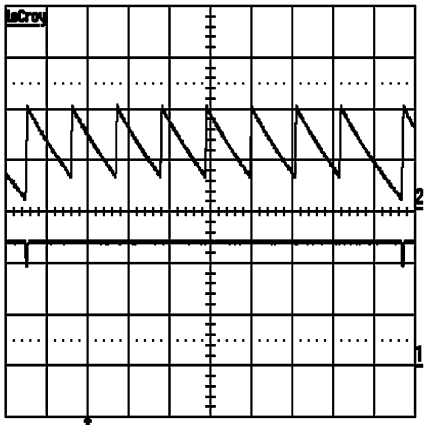
Horizontal Resolution: 5 ms/div
Trace 4: Input Current, 2A/div
Trace 2: PGD Pin, 50V/div
Trace 1: Vout, 20V/div
Vin = -36V
Voltages are respect to VEE

Figure 9. Turn-On Sequence With 4A Load Current



Horizontal Resolution: 20 ms/div
Trace 4: Load Current 0 to 5A, 2A/div
Trace 2: PGD Pin, 50V/div
Trace 1: Vout, 20V/div
Vin = -48V, Ct = 2.2 µF
Voltages are respect to VEE

Figure 10. Fault Timeout



Horizontal Resolution: 2sec/div
Trace 2: TIMER Pin, 2V/div
Trace 1 Vout, 20V/div
Vin = -48V, Ct = 2.2 µF
Voltages are respect to VEE

Figure 11. Restart Timing

13 Bill of Materials (BOM)

Table 1. Bill of Materials

Item	Description	Mfg, Part No.	Package	Value
C1, C5	Ceramic Capacitor	TDK C3216X7R2A104M	1206	0.1 µF, 100V
C3, 4, 7	Alum. Electrolytic Capacitor	Panasonic EEV-EB2D101M	Surf. Mount	100 µF, 200V
C8	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 µF, 100V
C6	Unpopulated			
C2	Ceramic Capacitor	TDK C2012X7R1C225K	0805	2.2 µF, 16V or higher
Q1	N-Channel MOSFET	Vishay SUM40N15-38	TO-263	150V, 40A
R1	Resistor	Vishay CRCW12069532F	1206	95.3k, 1/4 W
R2	Resistor	Vishay CRCW08054641F	0805	4.64k
R3	Resistor	Vishay CRCW08053321F	0805	3.32k
R4	Unpopulated			
R5	Resistor	Vishay CRCW25125101	2512	5.1k, 1W
R6	Resistor	Vishay CRCW08055622F	0805	56.2k
R7	Resistor	Vishay CRCW12061003F	1206	100k, 1/4 W
R8	Resistor	Vishay CRCW08050000Z	0805	Zero Ωs
R9	Resistor	Vishay WSL2010R0100F	2010	10 mΩ, 1/2 W
U2	Hot Swap IC	Texas Instruments LM5067	VSSOP-10	
Z1	Trans. Suppressor	Diodes Inc. SMBJ70A	SMB	70V

14 PC Board Layout

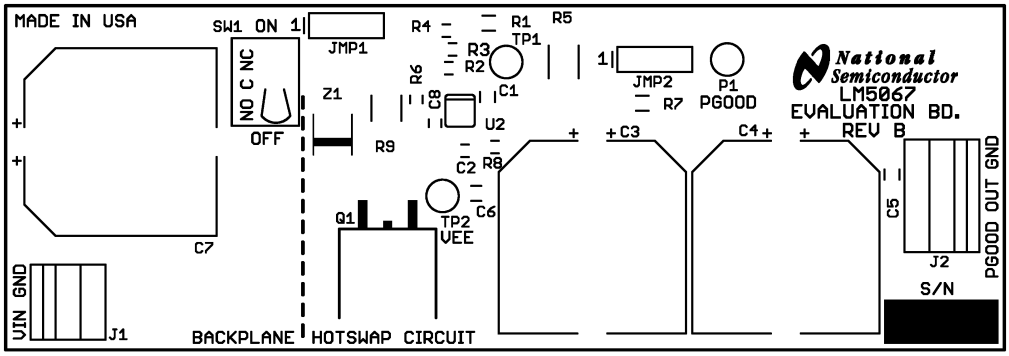


Figure 12. Board Silkscreen

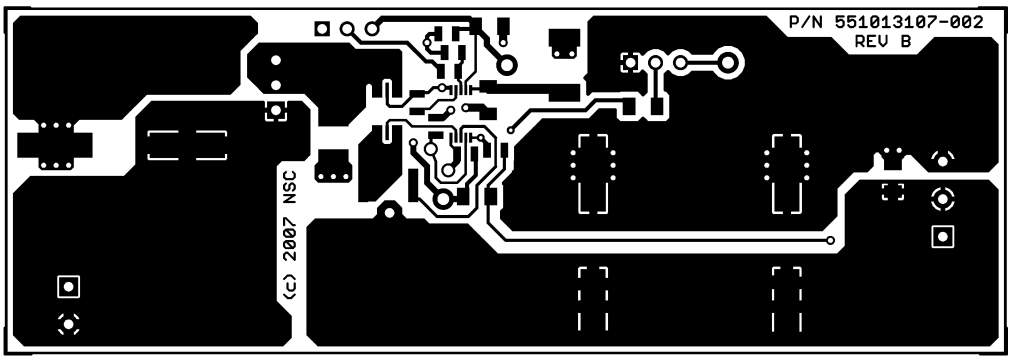


Figure 13. Board Top Layer

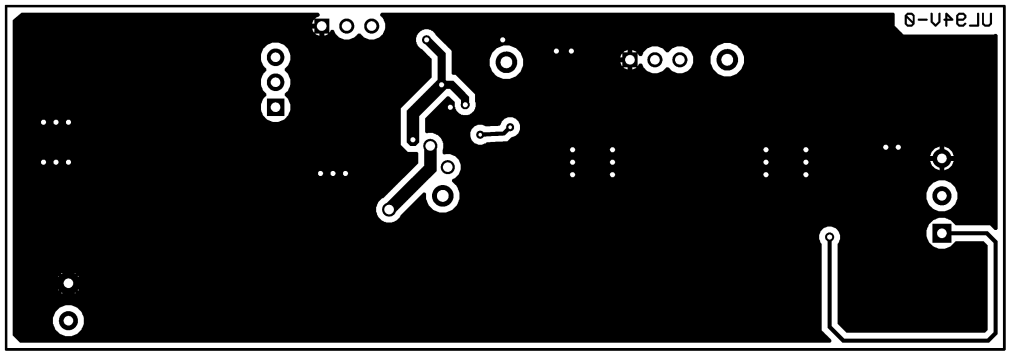


Figure 14. Board Bottom Layer (viewed from top)

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