Application Report
SNVA167A–May 2006–Revised April 2013

AN-1482 LDO Regulator Stability Using Ceramic Output Capacitors

ABSTRACT

Ultra-low ESR capacitors such as ceramics are highly desirable because they can support fast-changing load transients and also bypass very high frequency noise coming from switching converter power sources, which a linear regulator can not reject. However, using ultra-low ESR capacitors on the output of an LDO regulator requires that specific design changes be implemented to ensure loop stability.

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1 Introduction

This application report outlines the fundamentals of LDO loop compensation with respect to how the output capacitor's characteristics affect stability, also detailing the internal design techniques used to make LDO's that are stable when using ceramic output capacitors.

For more information on linear regulator compensation theory, see *AN-1148 Linear Regulators: Theory of Operation and Compensation* (SNVA020).

2 LDO Regulator Basic Operation

The low dropout (LDO) linear voltage regulator is unique because it can regulate the output voltage with an input voltage, which may be within a few hundred millivolts of the output voltage. It can do this because the pass transistor is a single PNP (or P-FET) device, which can be driven fully into saturation. This means the dropout voltage (the minimum required voltage difference from input to output) is the lowest of any linear regulator type (see Figure 1).

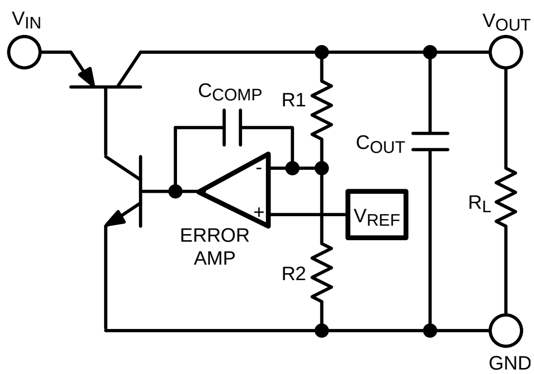

Figure 1. Typical PNP LDO Regulator

The LDO regulates it's output voltage by using an error amplifier to increase or decrease current drive to the PNP pass transistor as required by the load. Resistors R1 and R2 provide the voltage feedback from the output to the error amplifier, which compares this voltage to a fixed reference voltage. Negative feedback within the loop always forces the voltages at both inputs of the error amplifier to be equal. The output voltage is set by the ratio of the two resistors:

$$V_{OUT} = V_{REF} (1 + R1/R2) \quad (1)$$

3 LDO Loop Compensation

The P-type pass transistor of the LDO regulator drives the load off the collector (or drain), a configuration that has inherently high output impedance. Because of this, the capacitor connected to the output forms a pole with the load resistor whose frequency is given by:

$$P_{LOAD} = 1 / (2 \times \pi \times {}^*R_{OUT} \times C_{OUT}) \quad (2)$$

$^*R_{OUT}$ is here defined as the effective impedance from the output node to ground: this is actually the parallel combination of:

- The load resistance R_L
- The sum of R1 + R2
- The output impedance of the pass transistor

However, in most cases, the load resistance is orders of magnitude less than the other two elements, so R_{OUT} can be approximated as R_L:

$$P_{LOAD} \cong 1 / (2 \times \pi \times R_L \times C_{OUT}) \quad (3)$$

P_{LOAD} will be designated the **Load Pole**.

The frequency of the load pole varies with load resistance. As an example, an LDO using a 10 µF output capacitor driving a 3.3 Ω load has a load pole at:

$$P_{LOAD} \cong 1 / (2 \times \pi \times 3.3\ \Omega \times 10\ \mu F) = 4.8\ kHz \quad (4)$$

However, if the external load is disconnected (leaving only the regulator's internal resistive divider for a "load"), the frequency of the load pole may drop to less than one Hertz. This illustrates how the LDO load pole varies over a wide frequency range from "no load" to "full load" operation.

For this example, assume that the capacitor C_{COMP} will be used to add an "integrator" pole that is at a frequency of about 500 Hz. This means that the loop has two poles, which could potentially produce a phase shift of -180° and cause oscillations. The methods used to add phase lead to offset the phase lag of the poles will be discussed in the following sections.

It should be noted that there are additional high-frequency poles, so care must be taken to ensure that the loop bandwidth does not get too wide, or they will add enough phase lag to create an oscillator. The power device contributes one such pole: for example, the input capacitance of the P-FET used as a pass device forms a pole with the output impedance of the circuitry driving it's gate. Because this high-frequency pole is associated with the power device, it will be referred to as the **Power Pole (P_{PWR})**. For purposes of analysis, it will be assumed to be a fixed pole at a frequency located at about 500 kHz.

4 Methods for Adding Phase Lead

The poles in the loop of the LDO can cause oscillations if not compensated for by other zeroes, which will add some phase lead. One of the traditional methods for doing that is to add a feedforward capacitor across resistor R1 (Figure 2), which forms a pole-zero pair. The zero is at a lower frequency than the pole, which allows placing the zero at a frequency before the unity gain crossover occurs. In this way, the zero adds a significant amount of lead, while the associated pole (which is at a higher frequency) adds only a small amount of additional lag. This results in a net gain of phase lead and improved phase margin.

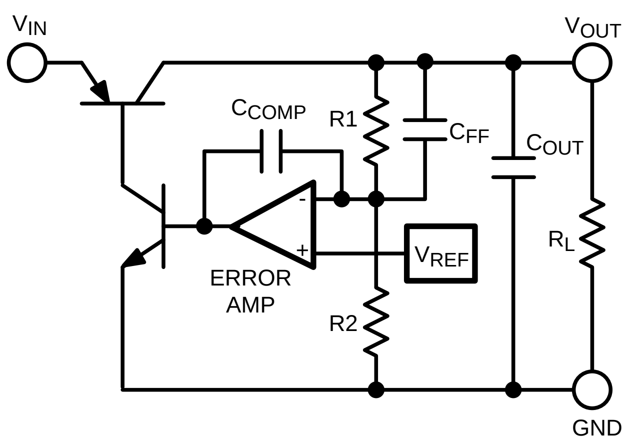

Figure 2. LDO Regulator with Feed-Forward Compensation

The capacitor C_{FF} forms a zero with R1 whose frequency is given by:

$$Z_{FF} = 1 / (2 \times \pi \times R1 \times C_{FF}) \quad (5)$$

And C_{FF} forms a pole with the parallel combination of R1 and R2, whose frequency is given by:

$$P_{FF} = 1 / (2 \times \pi \times R1 // R2 \times C_{FF}) \quad (6)$$

It's important to note that at higher output voltages (where R1 is much larger than R2), the pole and zero are far apart in frequency, allowing a much larger improvement in phase margin. At lower output voltages, the frequency of the pole and zero move closer together. The maximum possible phase lead provided by this method goes away quickly as the output voltage reduces, and it becomes completely useless when the output voltage equals the reference voltage. For this reason, relying on this compensation technique alone is adequate only for higher output voltages.

As an example, the gain and phase of a typical LDO will be calculated. Since LDO bandwidth is maximum at full load, that operating point will be used for the calculation. The following assumptions will be used:

1.25 V reference, regulator set to 6.25 V output.

V_{OUT} / V_{REF} = 5

Open loop gain = 80 dB

P_{COMP} = 500 Hz

P_{LOAD} = 4.8 kHz (C_{OUT} = 10 µF, R_L = 3.3 Ω)

P_{PWR} = 500 kHz

R1 = 40 kΩ

R2 = 10 kΩ

Unity gain crossover frequency estimate = 300 kHz

The optimum frequency location for the feedforward zero is typically about 1/3 of the unity gain crossover frequency. Therefore, a zero frequency of 100 kHz will be assumed for the example, giving a C_{FF} value of 39 pF. The pole formed by C_{FF} and R1//R2 will be located at about 500 kHz, essentially forming a double pole with P_{PWR} at 500 kHz.

Computing the phase for this set of component values and operating conditions shows a calculated phase margin of about 11° at the unity gain crossover frequency of 300 kHz (see Figure 3). This is barely stable, certainly a very marginal design if no other compensation method was used.

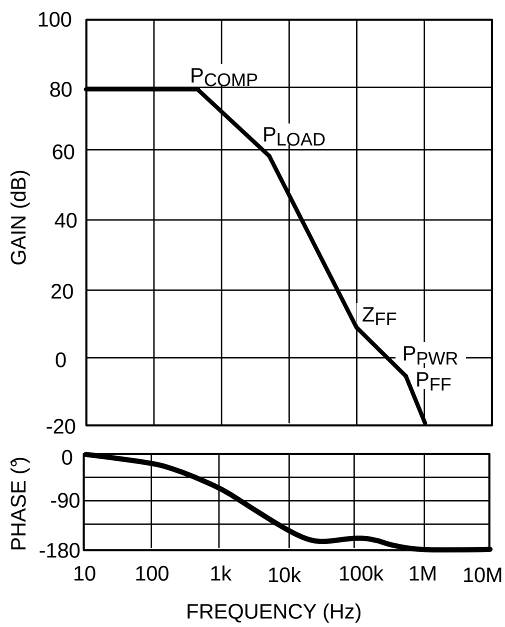

Figure 3. Gain/Phase Plot for Typical LDO Using Only Feed-Forward Compensation

While feedforward compensation is used in most LDO's to obtain whatever positive phase shift it can generate, additional phase lead must usually be derived by other means to obtain an acceptable phase margin. The following section details the method used in the vast majority of LDO regulators: output capacitor ESR compensation.

5 Output Capacitor ESR Compensation

Every capacitor contains some kind of parasitic resistance, which means a real capacitor can be modeled as a resistor in series with an ideal capacitor. This series resistance is typically referred to as **ESR** (equivalent series resistance).

The internal ESR forms a zero with the output capacitor whose frequency can be calculated from:

$$Z_{ESR} = 1 / (2 \times \pi \times ESR \times C_{OUT}) \quad (7)$$

The frequency location of this zero for Tantalum capacitors is typically ideally positioned for LDO compensation: a typical 10 µF Tantalum capacitor might have an ESR in the range of about 0.5 Ω, giving a zero at a frequency of about 30 kHz. This zero will be added to the example previously developed and displayed in a gain/phase plot. Figure 4 shows the additional phase margin derived from the addition of the ESR zero:

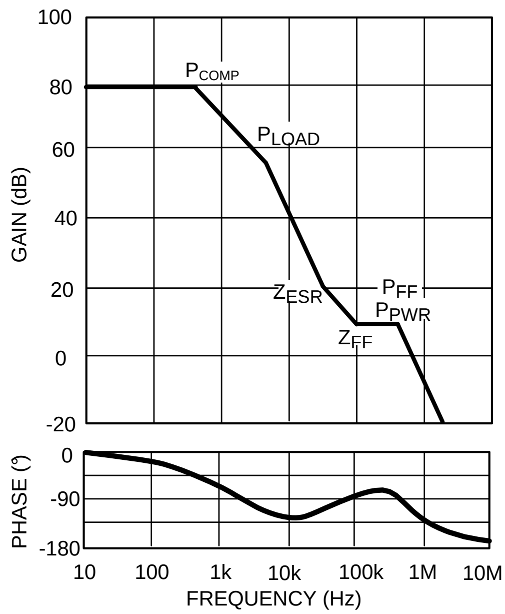

Figure 4. Gain/Phase Plot for Typical LDO Using Both Feed-Forward and ESR Compensation

The inclusion of the ESR zero into the example increased the calculated bandwidth from about 300 kHz to 600 kHz, but most important: it increased phase margin from 11° up to about 68° (which is extremely stable).

This example illustrates why most LDO's have a published "stable range" of ESR values, which the output capacitor must meet to ensure stable regulator operation: the ESR zero is the dominant compensation element for the loop. The "maximum" value boundary for ESR sets the lower limit for the zero frequency, which must not be so low that it increases loop bandwidth to the point that high frequency poles cause instability. The "minimum" ESR value boundary sets the maximum frequency for the zero, which must not be so high that it occurs so far after the unity-gain crossover frequency that it can no longer add enough phase lead to get sufficient phase margin for stable operation.

6 Ceramic Capacitors: ESR = mΩ

Ceramic capacitors do contain some parasitic ESR, but for capacitance values greater than 1 uF, the value of ESR is usually in the range of a few milliohms at high frequencies. This makes ceramic capacitors extremely attractive for bypassing high frequency noise and supporting rapidly changing load transients, but it also makes them unsuitable for use with LDO's, which were designed to rely on the output capacitor's ESR for the loop compensation zero. A 10 µF capacitor whose ESR is in the 5 mΩ range is providing a zero at a frequency above 3 MHz. As illustrated in the previous example, that frequency is too high to add enough phase lead to provide adequate phase margin at the unity-gain frequency.

LDO's that are stable with ultra-low ESR output capacitors have a zero built into the error amplifier compensation network. Instead of a simple integrator using only a single feedback capacitor C_{COMP}, a resistor is added in series (Figure 5). This combination of feedback elements creates both the integrator pole as well as a zero. This resistor (shown as R_{COMP}) provides a zero that performs the same function as the ESR zero, and will allow the use of ceramic output capacitors while maintaining good phase margin.

This design technique lowers the "minimum stable ESR" limit down to essentially 0 Ω, but it also lowers the maximum stable ESR limit as well. To understand why, it should be noted that since the error amplifier provides a zero inside the loop bandwidth, adding another zero will increase the bandwidth too much and allow high frequency poles to create instability.

A typical LDO designed to work with electrolytic output capacitors may have a stable ESR range of about 0.1 Ω up to 10 Ω. The "ceramic stable" version with an internal zero added allows ESR values down to 0 Ω, but the upper limit may be as low as about 0.5 Ω (depending on load current and size of C_{OUT}).

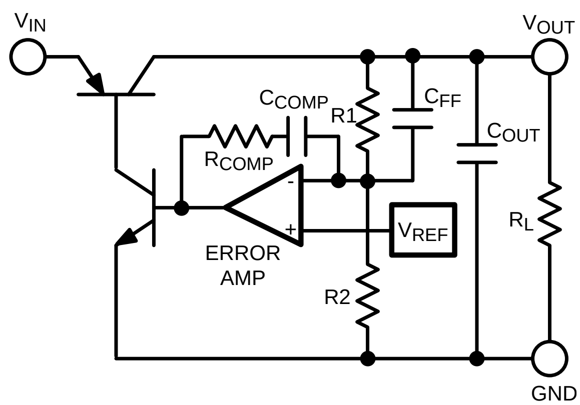

Figure 5. Ceramic-Stable LDO With Internal Compensation Zero

An example of the stable ESR range of a typical "electrolytic stable" LDO is shown in Figure 6. This is a reproduction of the ESR curve shown in the *LP2987/LP2988 Micropower, 200 mA Ultra Low-Dropout Voltage Regulator with Programmable Power-On Reset Delay; Low Noise Version Available (LP2988) Data Sheet* (SNVS004). The data points used to generate such ESR curves are empirically derived from bench testing by using a ceramic output capacitor (that has essentially no ESR) and soldering in discrete resistance values in series with it to find the point of instability at various load currents, with data being taken at both temperature extremes.

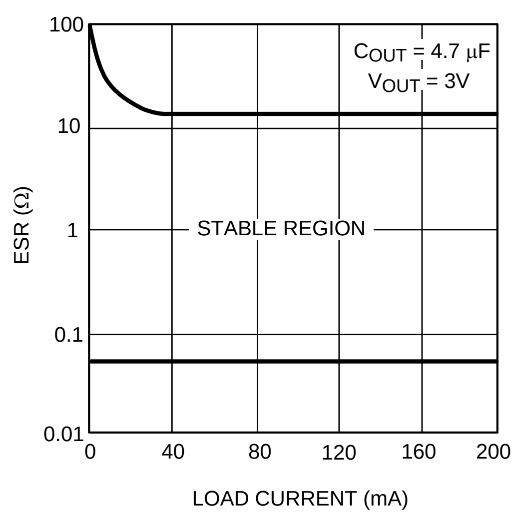

Figure 6. C_{OUT} ESR Stability Boundaries for Typical "Electrolytic Stable" LDO

As show, the lower limit of stable operation is approximately 50 mΩ, which is too high to allow the use of ceramic output capacitors, unless some external resistance is added in series with them. The upper ESR limit (that sets the lower frequency of the ESR zero) shows a ramp up at very light loads. This is due to the fact that the load pole moves to a lower frequency at very light loads (reducing loop bandwidth), allowing the frequency of the ESR zero to go lower and still have stable operation.

The ESR curve for a “ceramic stable” LDO regulator is shown in Figure 7. The lower limit of stable ESR is 0 Ω, and the upper limit is about 0.5 Ω except at very light load currents where the upper limit rises. As before, the reason the limit rises there is that the load pole drops to a very low frequency at light loads making the loop stable with the compensation zero at a lower frequency.

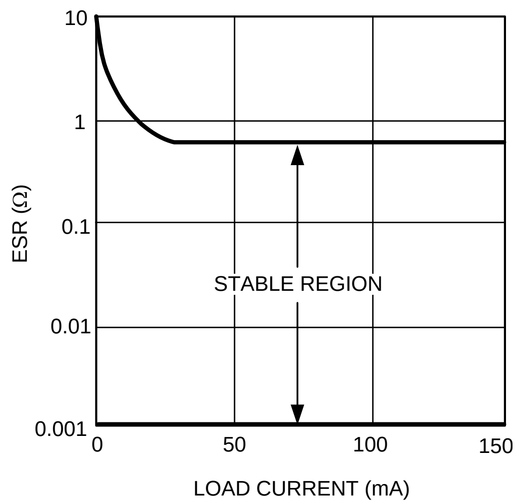

Figure 7. C_{OUT} ESR Stability Boundaries for Typical "Ceramic Stable" LDO

Based on these curves, it can be seen that the use of ceramic output capacitors is generally reserved for parts that are designed to use them. However, the “ceramic stable” LDO does have enough headroom on the upper ESR limit that low-ESR Tantalum and aluminum electrolytics may be used.

7 Additional Poles From Ceramic “Bypass” Capacitors

In many designs, especially ones where digital IC’s are present, bypass capacitors are often sprinkled throughout the PC board at the V_{CC} pin of every device powered by the voltage regulator. In most cases, these are small ceramic capacitors whose value is in the .01 µF to 0.1 µF range. These capacitors can cause LDO regulators to oscillate, and the reason is often not understood by the user.

As previously explained, a capacitor connected to the output of an LDO forms a “load pole” in conjunction with the effective resistance from the output node to ground:

$$P_{LOAD} = 1 / (2 \times \pi \times R_{OUT} \times C_{OUT}) \quad (8)$$

What may not be obvious is that small capacitors connected to the output can add an unwanted pole at a frequency, which can reduce or eliminate phase margin. LDO regulators that use electrolytic output capacitors (and rely on their ESR for the compensation zero) are vulnerable to this effect.

The previously derived example (gain/phase plots are shown in Figure 4) will be used to explain how this can occur:

Open loop gain = 80 dB

$V_{OUT} / V_{REF} = 5$

P_{COMP} = 500 Hz

P_{LOAD} = 4.8 kHz (C_{OUT} = 10 µF, R_L = 3.3 Ω)

P_{PWR} = 500 kHz

R1 = 40 kΩ

R2 = 10 kΩ

C_{FF} = 39 pF (P_{FF} = 510 kHz, Z_{FF} = 100 kHz)

C_{OUT} = 10 µF Tantalum / ESR = 0.5Ω

(ESR zero frequency = 30 kHz)

Unity gain crossover frequency estimate ≅ 600 kHz

Phase margin = 68° (without ceramic output capacitance added)

The previously calculated phase margin is about 68° (very stable) with only a 10 µF Tantalum output capacitor. What happens if a total of ten 0.1 µF ceramic “bypass” capacitors are connected to the output of the LDO, effectively creating a 1 µF ceramic capacitor in parallel with the 10 µF Tantalum?

To calculate the new pole created by the ceramic bypass capacitors:

$$P_{LOAD} = 1 / (2 \times \pi \times R_{OUT} \times C_{OUT}) \quad (9)$$

In calculating R_{OUT}, we are most concerned with the impedance from output to ground at frequencies near the unity-gain crossover (about 600 kHz). In that frequency range, the 10 µF Tantalum capacitor would effectively look like a 0.5 Ω resistor from output to ground, the 3 Ω load resistor would be in parallel with it, yielding an effective value for R_{OUT} of about 0.43 Ω. The pole resulting from this impedance and the ceramic capacitors is:

$$P_{BYP} = 1 / (2 \times \pi \times 0.43 \times 1\ \mu F) = 370\ kHz \quad (10)$$

Assuming the unity-gain frequency is still approximately 600 kHz, this added pole would drop the phase margin from 68° down to about 9° (very poor). This gain/phase plot is shown in Figure 8.

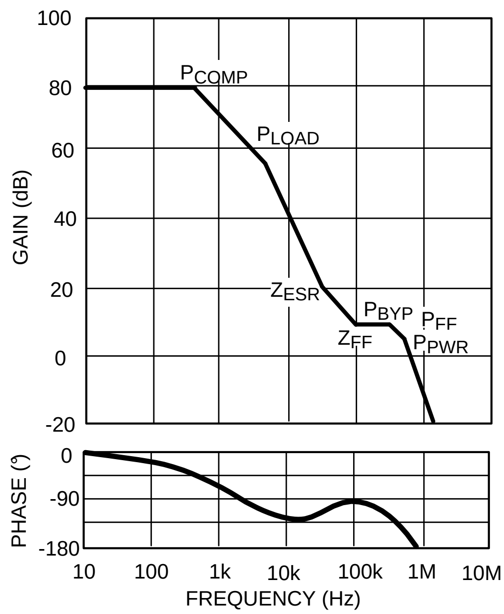

Figure 8. Phase Margin Reduced by 1 µF Ceramic Capacitor Connected to the Output

This example illustrates how even a relatively small amount of ceramic capacitance added to the output of an LDO not designed for ceramics can cause it to go unstable. The incorrect assumption typically made is that when a small capacitor is in parallel with a larger capacitor, the smaller one’s effect will be “swamped out” by the larger one. However, the smaller value of capacitance made up by the “bypass capacitors” will form it’s own pole. If that pole is near or below the unity-gain crossover frequency of the loop, it can add enough phase lag to create an oscillator.

8 Minimizing Effect of Bypass Capacitors

Since small value ceramic capacitors placed on the output of LDO regulators can reduce phase margin, care should be taken to keep these as far as possible from the output terminal of the regulator. Capacitors whose value is in the range of about .01 µF to 0.1 µF are usually the most problematic.

Trace inductance in series with these capacitors will help decouple their resonant effect. Since board layouts vary, a “safe distance” boundary for all applications can not be given. Narrow copper traces have significantly higher inductance than copper planes, so the “affecting distance” of the capacitors increases when power planes and ground planes are used to route power across the board.

The reliable way to determine if board capacitance is reducing phase margin is to perform load step testing on the actual board with all capacitors in place. The IC’s that the regulator powers should be removed (or not installed) and a resistor should be used at the output of the regulator that provides the same load current. The load should be stepped from no load to rated load while the output is watched for ringing or overshoot during the load step transient: excessive ringing indicates low phase margin.

9 References

LP2987/LP2988 Micropower, 200 mA Ultra Low-Dropout Voltage Regulator With Programmable Power-On Reset Delay; Low Noise Version Available (LP2988) Data Sheet (SNVS004)

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