

# Optimizing L Measurement Resolution for the LDC1312 and LDC1314

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#### ABSTRACT

TI's LDC1312 and LDC1314 devices are versatile devices which provide 12 bits of inductive measurement resolution. This application note covers configuration options and methods to improve the effective resolution for these devices.

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## 1 Understanding LDC Resolution

For an ADC, the resolution is generally the number of bits in the output word, and the effective resolution is determined from the either the INL of static linearity or from the SINAD of a full scale sinewave. If the signal amplitude input to an ADC is less than full scale, the resolution of the output word is still the same, but the effective resolution decreases. For example, given an ADC with an input range of 1 VPP and an effective resolution of 16 bits, if the input signal is only 500 mVPP, then the effective resolution will usually be halved to 15 bits.

Most inductive sensors are not able to utilize the full scale input range that TI's LDCs provide. This results in a reduction in the effective resolution of the system. The larger the shift in sensor inductance due to target movement, the more effective resolution the LDC can provide. A system which has an inductance shift of 20% will have twice the effective resolution of an equivalent system which has a 10% shift.

TI's LDC devices measure the inductance by measuring the resonant frequency of a sensor, and so the LDC can be considered a frequency measurement version of an ADC. Where an ADC has an LSB measured in voltage, an LDC has an LSB measured in Hz.

For example, with an LDC system with a frequency resolution of 50Hz (1LSB=50Hz), if the sensor signal varies by 20 kHz, then the LDC would have an effective resolution of 8.6 bits.

There are two basic approaches to increase the effective resolution – first by improving the frequency resolution, and second by increasing the sensor frequency variation.

## 2 LDC Configuration Parameters

There are several LDC parameters which determine the device resolution.

## 2.1 Reference Count and RCOUNT

The primary device setting which determines the conversion resolution is the RCOUNT setting. A higher value for RCOUNT corresponds to a higher resolution L measurement.

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LDC Configuration Parameters

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#### **Table 1. RCOUNT Registers**

DEVICE	REGISTERS
LDC1312	RCOUNT_CH0 (address 0x08) RCOUNT_CH1 (address 0x09)
LDC1314	RCOUNT_CH0 (address 0x08) RCOUNT_CH1 (address 0x09) RCOUNT_CH2 (address 0x0A) RCOUNT_CH3 (address 0x0B)

Due to device restrictions, RCOUNT must be  $\geq$ 3 and  $\leq$ 65535. For the LDC1312 and LDC1314, there are 2 or 4 16-bit wide registers, respectively, for setting RCOUNT independently for each device channel. Setting an RCOUNT value greater than 0x2000 provides no benefit for the LDC131x, and simply reduces the sample rate.

The effective LDC resolution is a function of the RCOUNT and sensor frequency. Higher values of RCOUNT deliver increased resolution, and lower sensor frequencies can provide improved resolution.

## 2.2 Reference Frequency

The reference frequency determines the conversion time for a given RCOUNT value. The basic conversion time equation is shown in Equation 1.

$$t_{\text{CONVERSION}}(s) = \frac{\text{RCOUNT} \times 16}{f_{\text{REF}}}$$

(1)

It is clear that to increase the sample rate, the reference frequency should be increased and/or the setting of RCOUNT should be decreased. As mentioned previously, decreasing RCOUNT will decrease the measurement resolution.

As a general rule, use the highest reference frequency supported by a given LDC. Then set RCOUNT value that the sample rate matches the minimum system requirement.

#### **Table 2. Supported Reference Frequency and Sample Rates**

PARAMETER	LDC131x	
Number of channels	2 (LDC1312) 4 (LDC1314)	
Maximum reference frequency	40-MHz dual channel 35-MHz single channel	
Maximum output resolution	12/16 bits (based on OUTPUT_GAIN setting)	
Conversion time for maximum RCOUNT with maximum f <sub>REF</sub>	26.2 ms at 40 MHz 30.0 ms at 35 MHz	

# 2.3 Using the LDC131x $f_{REF}$ Divider or Reducing $f_{REF}$

The LDC devices include input and clock dividers for more flexibility in setting the sensor frequency and reference frequency in a system. The dividers for the LDC131x can be used as an additional method to tradeoff sample rate for measurement resolution. The lower resolution of the LDC131x means that reducing the sensor frequency can reduce the effective resolution, as shown in Table 3.

f <sub>sensor</sub>	f <sub>REF</sub>	LDC131x OUTPUT CODE (decimal)	LDC131x OUTPUT CODE (binary)	BITS OF AVAILABLE RESOLUTION
9.8 MHz	40 MHz	1004	0011 1110 1100	10
3.2 MHz	40 MHz	328	0001 0100 1000	9
980 kHz	40 MHz	100	0000 0110 0100	7
320 kHz	40 MHz	33	0000 0010 0001	6

Table 3.	LDC131x	Device	Resolution
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It is clear that when the ratio of  $f_{SENSOR}/f_{REF}$  decreases, more of the leading bits are always set to 0. With an  $f_{SENSOR}$  of 980 kHz, the first 5 bits of the LDC131x are always 0, leaving an effective resolution of only 7 bits. This can be compensated by using the Output Gain setting, which is detailed below.

In order to maximize the output code variation, and hence the SNR, decreasing the reference frequency can provide improved resolution by leaving more bits of resolution. This can be viewed as reducing the reference voltage for an ADC to obtain improved conversion resolution:

f <sub>sensor</sub>	f <sub>REF</sub>	LDC131x OUTPUT CODE (decimal)	LDC131x OUTPUT CODE (binary)	BITS OF AVAILABLE RESOLUTION	SAMPLE RATE WITH RCOUNT=0x0400
980 kHz	40 MHz	100	0000 0110 0100	7	2.441k SPS
980 kHz	20 MHz	201	0000 1100 1001	8	1.221k SPS
980 kHz	10 MHz	401	0001 1001 0001	9	610 SPS
980 kHz	4 MHz	1004	0011 1110 1100	10	244 SPS

### Table 4. LDC131x Device Resolution

The reduction of the reference frequency can be done by either changing the external input frequency, or by setting the reference dividers (for example, for a 10-MHz  $f_{REF}$ , if  $f_{CLKIN}$ =40 MHz, then set the  $f_{REF}$  divider to 4).

This technique can be used with the output gain functionality to optimize the effective resolution of the LDC131x.



Figure 1. LDC1312 Clocking Diagram

# 2.4 Resolution as a Function of Sensor Frequency

The effective resolution also varies based on the sensor frequency. At higher sensor frequencies, the LDC will appear to having missing codes, where the gaps between subsequent output codes will become larger and larger as the sensor frequency increases. This is why the effective resolution drops off as the sensor frequency increases. Note that set of output codes is a function of the value of RCOUNT – a different value for RCOUNT will produce a different set of output codes.



#### LDC Configuration Parameters

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At low sensor frequencies, the LDC output code will increment by 1 code as the sensor frequency increases, as expected. However, as the frequency increases further, then the output code will start skipping 1 code, then skipping several codes, and then gap between output codes will become larger and larger.

### 2.5 Sensor Amplitude

The sensor oscillation amplitude indirectly affects the effective measurement resolution of LDC devices. In general, higher sensor oscillation amplitude improves the SNR for a given sensor. The LDC1312 and LDC1314 devices control the sensor amplitude based on the IDRIVE current setting. Configuring the sensor amplitude to the recommended range of 1.2 V to 1.8 V will provide the optimum measurement resolution.

#### 2.5.1 Deglitch Filter Setting

The LDC1312 and LDC1314 devices feature internal filters which improve the frequency measurement accuracy. There are 4 settings: 1 MHz, 3.3 MHz, 10 MHz, and 33 MHz. This setting should be set to the lowest of the 4 values that exceeds the maximum sensor frequency, which typically occurs with the highest target-sensor interaction.

#### 2.5.2 Injection Resonance Locking

In the same way that independent pendulum clocks can become synchronized (as first documented by Christiaan Huygens), the LDC can exhibit resonance locking. With low sensor amplitudes, a small amount of energy can couple from an external clock source into the sensor, and lock the sensor frequency to an integer divider of the clock frequency. For example, if the sensor frequency should be 8.0003 MHz due to the target interaction, the sensor frequency could remain at 8 MHz if the reference frequency was 40 MHz.

This effect is more pronounced with lower value odd dividers of the reference frequency ( $f_{CLKIN}$ ÷3,  $f_{CLKIN}$ ÷5,  $f_{CLKIN}$ ÷7) than higher value dividers or even dividers. It is important to note that it is the external frequency  $f_{CLKIN}$  that couples into the oscillator, not the internal frequency  $f_{REF}$ .

This effect can be reduced by:

- Shifting the sensor frequency away from a strong locking frequency (one way is to simply adjust the sensor capacitance).
- Increasing the sensor current drive value.
- Using a different f<sub>CLKIN</sub> that does not have an odd integer divider in the sensor frequency variation.
- Ensuring the CLKIN line has well-controlled Z0 and does not exhibit significant overshoot/undershoot.
- Using a good ground plane for the LDC
- Maintaining separation between the sensor traces and the CLKIN line.

# 3 LDC Clocking

## 3.1 Internal Oscillator vs External Oscillator

The LDC1312 and LDC1314 devices include an internal oscillator. While the internal oscillator has a small shift across temperature, it is not as stable as a good external oscillator.

The resolution of the LDC131x devices will not be able resolve the internal oscillator's increased noise floor unless RCOUNT < 128. This would correspond to a sample rate of 17.1 kSPS with a 35-MHz  $f_{REF}$ , which exceeds the data throughput of the LDC131x, and so is not a practical restriction. For applications which can tolerate a larger amount of conversion drift, using the internal oscillator of the LDC131x is generally acceptable. However, there are some applications which require absolute matching or better stability sample-to-sample, and so an external oscillator may be needed.

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# 3.2 Single-Channel f<sub>REF</sub> Limitation Work-Around

If using the LDC1312 or LDC1314 device in single channel mode, the maximum reference frequency supported is 35 MHz. This limitation results in a 14% reduction in resolution for a fixed sample rate compared to the 40 MHz maximum for multi-channel operation.

For systems where  $f_{CLKIN} = 40$  MHz, the CLKIN Divider must be set to 2 to comply with the maximum  $f_{REF}$  of 35 MHz. This division produces a  $f_{REF} = 20$  MHz, which results in a 50% drop in resolution compared to a 40-MHz  $f_{REF}$ .

If the Channel 0 activation time (which is roughly  $Q/f_{SENSOR}$ ) is short enough, it may be advantageous to attach an additional sensor onto channel 1 but ignore the conversion data from Channel 1. In this way the LDC131x can operate with  $f_{REF}$ =40 MHz, but at the cost of conversion time on the second channel. The sensor geometries do not need to match Channel 0's sensor.

To maximize the effectiveness of this technique, the Channel 1's conversion time and settling count should be set to the device minimum (RCOUNT\_CH1=3, SETTLECOUNT\_CH1 = 1).

For a 1 MHz sensor with a Q of 20 up to sample rates of 1500 SPS, this technique improves the resolution compared to using a 35-MHz  $f_{REF}$ . For a sensor frequency of 5 MHz with a Q of 20, this technique is useful up to sample rates over 6k SPS.



Figure 2. Effective Resolution Comparison for Various LDC Clocking Configurations

The sensor activation time is based on the sensor frequency and Q. Decreasing the sensor Q and/or increasing  $f_{\text{SENSOR}}$  for the dummy second channel will reduce the activation time, which makes this technique more effective.

# 3.3 Using Offset Gain

The LDC131x is internally a 16 bit device, as all conversions done with 16 bits of resolution, but are quantized to a 12 bit word width. Accessing the additional 4 bits is done by use of the Offset Gain feature, which can provide access to the 4 additional bits of resolution. Measurement timing is unaffected by using gain and offset.

By default, the gain feature is disabled and the DATA registers display the 12 MSBs of the 16 bit word. However, it is possible to shift the data output as shown in Figure 3.

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Figure 3. LDC131x Offset Gain

Setting the gain of 4x, 8x, or 16x causes a 2-bit, 3-bit, or 4-bit data shift which is equivalent to increasing the maximum effective number of bits by 2 bits, 3 bits, or 4 bits, respectively.

#### 3.3.1 Example Use of Offset-Gain

The example uses an LDC1314 EVM (rev A). The target used for this analysis is a flat disk 25 mm in diameter that is moved axially from 0.2-mm distance from the sensor to infinite target distance.

#### 3.3.1.1 Step One: Determine System Boundaries

When moving the quarter between the minimum target distance (0.2 mm) and maximum target distance (infinite), the LDC output is shown in Table 5.

	LDC1314 ch0 DATA OFFSET = 0000 (0x0000)
Min target distance (0.2 mm)	291 (0x123)
Max target distance (infinite)	201 (0x0C9)
Code delta	90 codes
Effective resolution (ENOB)	$Log_2$ (90) = 6.5 bits

Table 5. LDC131x Performance with Gain = 1 (Output\_gain = 0x0)

Using the gain feature discards the MSBs, and therefore it is important to ensure that the maximum output scale does not go below 0 or above full scale of the new data output. The LDC131x data sheet shows that the maximum output range must be:

- $\leq$  100% of full scale with gain = 1
- $\leq 25\%$  of full scale with gain = 4

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- ≤ 12.5% of full scale with gain = 8
- $\leq 6.25\%$  of full scale with gain = 16x



# 3.3.1.2 Step Two: Apply Gain

The full scale data word is  $2^{12}-1 = 4,095$ . This example shows code delta of 90 codes between minimum and maximum target positions, which is only 2.2% of full scale. The LDC131x can therefore use the maximum gain setting of 16x. With this gain setting, the response is now shown in Table 6.

	Gain = 1 (Output_gain =0x0)	Gain = 16 (Output_gain =0x3) <sup>(1)</sup>
Min target distance (0.2mm)	291 (0x123)	4095 (0xFFF) (*)
Max target distance (infinite)	201 (0x0C9)	3212 (0xC8C)
Code delta	90 codes	875 codes (*)
Effective resolution (ENOB)	$Log_2$ (90) = 6.5 bits	N/A (*)

#### Table 6. LDC131x Performance with Gain = 1 vs Gain = 16

<sup>(1)</sup> (\*) indicates signal is clipped

The code delta has improved greatly, but the data output at the minimum target distance clips at full scale of the new data word.

#### 3.3.1.3 Step Three: Subtract Offset

While this system only uses 2.2% of full scale, it crosses the full scale boundary which results in a loss of information. This issue can be fixed by using the offset register to subtract a constant value from the data output. In this way the output code will be within the range of [0:4095]. The maximum target distance output code is 3,212, and so setting the offset to 2,000 codes (0x7D0)+ will suffice.

	Gain = 1 (Output_gain =0x0) offset = 0x000	Gain = 16 (Output_gain =0x3) offset = 0x000 <sup>(1)</sup>	Gain = 16 (Output_gain =0x3) offset = 0x7D0
Min target distance (0.2 mm)	291 (0x123)	4095 (0xFFF) (*)	2670 (0xA6E)
Max target distance (infinite)	201 (0x0C9)	3212 (0xC8C)	1212 (0x4BC)
Code delta	90 codes	875 codes (*)	1458 codes
Effective resolution (ENOB)	$Log_2$ (90) = 6.5 bits	N/A (*)	Log <sub>2</sub> (1458) = 10.5 bits

#### Table 7. LDC131x Performance with Gain = 1 vs Gain = 16

<sup>(1)</sup> (\*) indicates signal is clipped

With a gain of 16x and an offset of -2,000 codes, the LDC now records data between 1,212 and 2,670. This is well within the output code limits of 0 to 4095. The code delta is 1,458 codes, which is a 4 bit improvement over the default case with a gain of 1.

Figure 4 shows the operating output range for this example without gain, with a gain of 16, and with gain of 16 and offset of -2,000.





Figure 4. Conversion Signal Range Increases

# 3.4 Setting LDC131x RCOUNT

Setting the RCOUNT for the LDC131x to greater than 0x2000 provides no additional resolution output for the LDC131x, due to its internal quantization limitation of 16 bits. Higher reference counts will increase conversion time, and so it is not recommended to set any higher value.

If higher resolution is required and slower sample rates are acceptable, it may be better to average multiple conversions.

## 4 Summary

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There are several parameters in the LDC devices which affect the device resolution. These are primarily managing the sensor frequency, RCOUNT values, using a clean reference, and properly setting the sensor current drive.

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