ADC083000,ADC12DL080,ADC14155, ADC14DS105,LMH6515,LMH6552,LMH6555, LMK02000,LMK03001,LMX2531

Selecting Amplifiers, ADCs, and Clocks for High-Performance Signal Paths

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Tips, tricks, and techniques from the analog signal-path experts

Selecting Amplifiers, ADCs, and Clocks for High-Performance Signal Paths

— By Mike Ewer, Principal Applications Engineer

Modern communication and measurement system designs are increasing in complexity as the latest high-performance processors and DSPs enable new signal-processing techniques. As system requirements for speed and resolution increase, more capable Analog-to-Digital Converters (ADCs) emerge, and these in turn require higher-performance Analog Front Ends (AFEs). In many systems the AFE can be considered a key limiting factor in the overall system performance. Applications such as medical ultrasound, RADAR, Radio Frequency Identification (RFID), and video imaging similarly demand high-performance AFEs. AFE designers today are faced with the challenge of selecting the best amplifier to drive the ADC, including how to maximize the dynamic range of the signal path and how to choose the best filter for a given application. This article will address the design of high-speed data acquisition systems, including some of the limiting factors in the overall system performance created by the AFE and the clock driving the ADC.

A generic AFE signal path including a source (Vs), Low-Noise Amplifier (LNA), ADC driver, channel filter, sampling clock, and ADC stages are shown in *Figure 1*.
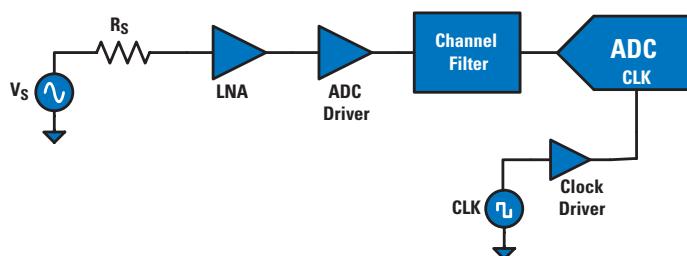

Figure 1. AFE Signal Path

A key measure of any data-acquisition-system performance is the Effective Number Of Bits (ENOB) of resolution it delivers. The ENOB is maximized by minimizing the noise and distortion added by each stage of the AFE to the processed signal. A measure of the noise added by a particular stage is the noise factor, F, which is the total input referred noise of the stage divided by the input noise due to the previous stage. The often-quoted Noise Figure, NF, is 10 log F.

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Ignoring the filter, the noise of the overall cascaded path shown is given by Frii's equation:

$$F_{CASCADE} = F_{LNA} + \frac{F_{DRIVER} - 1}{G_{LNA}} + \frac{F_{ADC} - 1}{G_{LNA} \times G_{DRIVER}}$$

Where F_{LNA} = noise factor of LNA
F_{DRIVER} = noise factor of driver stage
F_{ADC} = noise factor of ADC
G_{LNA} = Gain of LNA
G_{DRIVER} = Gain of driver stage

The noise of the ADC driver is divided by the gain of the LNA and consequently, it is best to select the lowest-noise LNA available and take as much gain as possible at this first stage. Since the noise of the driver is divided by the LNA gain, it becomes less critical to the overall noise performance. In fact, the further along the signal path, the less critical the noise performance of each stage becomes.

The building block after the LNA is the ADC-driver stage. In a system that responds down to signals at 0 Hz, a DC-coupled amplifier is the only choice, while in an AC-coupled system, a transformer can also be used. However, transformers are limited in their frequency range of operation and can have poor differential output balance, which is important when driving differential-input ADCs. When providing gain, transformers also multiply the source impedance driving the ADC by the transformer turns ratio squared. This reduces the pole frequency formed with the ADC-input capacitance, thereby reducing system bandwidth. Even though amplifiers can add more noise than a transformer, they have better gain flatness and can provide a range of desired gains by setting external resistors. The gain of a transformer is limited by achievable turns ratios. Amplifiers have lower output impedance which is not significantly affected by the choice of gain.

The signal path between each stage may be single-ended or differential, depending on the initial signal source. For a source with a single-ended output, a "single-to-diff stage" can be used to create differential-drive signals. Differential signal paths are higher performance, but the drawbacks include an increase in the number of components, board area, cost, and complexity of the filter.

Types of Data Acquisition Systems

Sampled-data systems can be split into two main types. The simplest is the baseband system also known as the "1st-Nyquist-zone" system. The second is the more complex under-sampled system, often referred to as bandpass, narrow band, sub-sampled, or Intermediate Frequency (IF)-sampled system. Baseband-system signal paths are generally DC-coupled while IF-bandpass signal paths tend to be AC-coupled. In a conventional 1st-Nyquist-zone system, the ADC samples the input at sample rate, f_S, which is at least twice the highest signal frequency, f_H, present at the ADC input (*Figure 2a*).

To avoid aliasing of input frequencies above $f_S/2$ back down into the 1st Nyquist zone as shown in *Figure 2b*, the ADC input is normally band-limited to the 1st Nyquist zone by a low-pass channel filter.
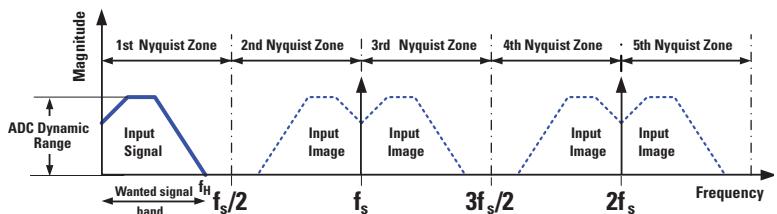

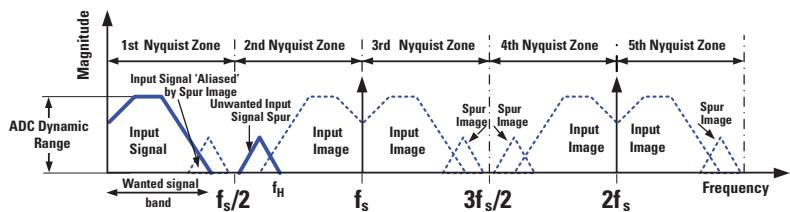**Figure 2a. 1st Nyquist baseband sampling where ($f_S > 2f_H$)**

Figure 2b. 1st Nyquist sampling with no ADC input filter showing input spur >$f_S/2$ aliasing back into 1st Nyquist zone to interfere with input< $f_S/2$

To use the full ADC dynamic range, ensure that any undesired, out-of-band signal components are filtered to less than the ADC Least Significant Bit (LSB) level. This requires high-order filters to obtain a sufficiently sharp roll off if the wanted and unwanted input-signal components approach too close to $f_S/2$ (*Figure 2c*).

One solution is to increase the ADC sample rate and over-sample the input signal. This spreads the Nyquist zones further out in frequency and relaxes the channel-filter design (*Figure 2d*). High-speed baseband sampling is found in many test and measurement applications requiring data conversion from DC to GHz.

An under-sampled system employs an ADC with a full-power bandwidth much higher than $f_S/2$. For example, it is not unusual to find a 1 GHz-input bandwidth on a 100 MHz-sampling ADC. This allows a narrowband input centered at a frequency $>f_S/2$ to be under-sampled at a rate much lower than the conventional Nyquist f_S rate, and aliased or "folded" back down to the 1st Nyquist zone. This is shown in *Figure 3*a where signal A is the desired signal being converted.

At higher input frequencies, the input stage of the ADC becomes slew-rate limited. For optimum distortion performance from the ADC, it is recommended to keep the center frequency of the under-sampled signal to no more than 10% to 30% of the ADC's full-power bandwidth depending on the performance of the ADC.
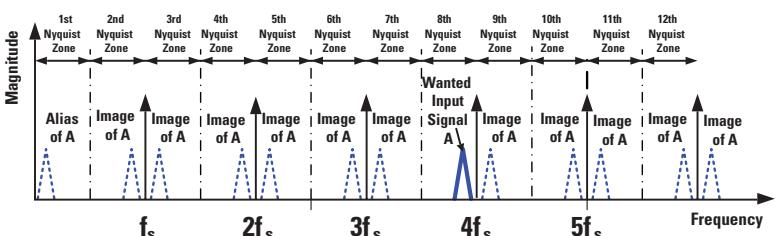
In an under-sampled system, the channel filter is the key to ensuring that the desired signal is optimally recovered at baseband and separated from all the
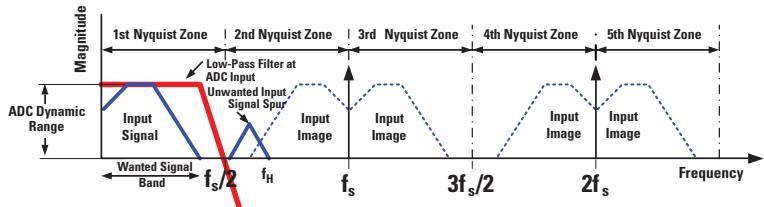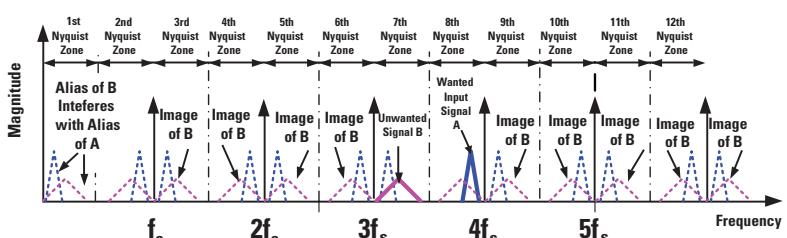

Figure 2c. 1st Nyquist baseband sampling with low-pass filter
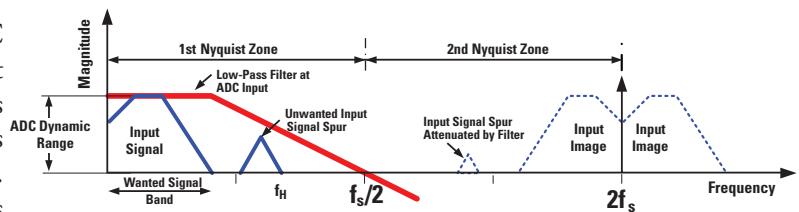
Figure 2d. 1st Nyquist baseband >2x over-sampling with 'relaxed' low-pass filter requirement

Figure 3a. Wanted signal A $>f_S$ under-sampled from 8th Nyquist zone back to 1st Nyquist zone

Figure 3b. Failure to bandpass filter unwanted signal B allows it to alias back to the 1st Nyquist zone and interfere with the recovery of wanted signal A

other aliased components. A bandpass filter is used to remove all interfering frequencies and noise from the ADC input which might otherwise alias back to baseband with the wanted signal. *Figure 3b* shows the effects of a second unwanted signal B folding back from the 7th Nyquist zone to interfere with

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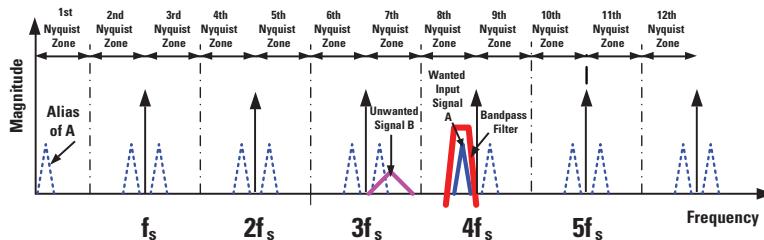
Figure 3c. Unwanted signal B prevented from aliasing B by bandpass filter around A

signal A and prevent recovery at baseband. *Figure 3c* shows the required bandpass filter.

Often in an under-sampled system, the signal bandwidth of interest is over-sampled, such as a 100 MSPS sampling of a 5 MHz-bandwidth signal, and post-filtered digitally to improve the dynamic range of the system. Noise-processing gain is obtained by the fact that the ADC's input referred noise is spread over the entire 1st Nyquist zone from zero to $f_S/2$. By restricting the input bandwidth to less than $f_S/2$, the noise at the input of the ADC is reduced, giving increased dynamic range and resolution. The added processing gain is given by the equation:

$$\text{Processing Gain} = 10 \log [(f_S/2)/ \text{ BW}] \text{ dB}$$

where BW is the post-filtered signal bandwidth. For f_S = 100 MSPS and BW = 5 MHz, this equates to a 10 dB-processing gain. To maximize processing gain, over-sample the signal bandwidth at the highest-possible sample rate, and post-process the narrowest-possible signal bandwidth.

Under-sampling is employed in many modern radio and RADAR systems where a single, analog-mixer stage down-converts an RF signal to an IF signal which, after bandpass filtering, is aliased to digital baseband where the final signal is extracted by further digital processing. This reduces the number of analog-mixer and filter stages. Under-sampling the input signal is equivalent to a baseband ADC plus IF down-conversion mixer. The downside of under-sampling is the higher-frequency performance required from the amplifier and ADC, more stringent jitter requirements on the ADC clock, and the requirements for DSP processing.

Sampling Clock Considerations

Clock jitter on the ADC clock is another key factor affecting the sampling system Signal-to-Noise Ratio (SNR). At high-input-signal frequencies, the SNR of the ADC departs from the familiar quantization-noise-limited level of 6.02n + 1.76 dB (where n = number of bits) to the jitter-noise-limited level of -20 x $\log(2\pi$ x f_{SIGNAL} x $tj_{rms})$. The variable f_{SIGNAL} is the highest-input-signal-frequency component for conversion by the ADC. The variable tj_{rms} is the total-rms clock jitter in seconds, given by the root-sum square of all the rms-timing jitter components from the different stages in the clock path including the clock source, clock buffer, and the internal-clock circuit within the ADC.

For example, to obtain 74 dB-SNR performance at 300 MHz requires the total rms jitter in the clock path including the ADC to be less than 105 femto seconds (fs) rms. National's newest high-sample-rate converters are specified with 2 V_{P-P} differential clocks to minimize jitter and maximize SNR. It is important to drive these inputs with low-jitter clocks. For instance, a 70 fs, external-clock-path jitter combined with a 70 fs, internal-ADC-clock jitter delivers 100 fs total jitter (combined in rss fashion). National offers a family of low-jitter-clock components targeted at this application.

ADC Input Stage

When choosing an amplifier to drive a high-speed ADC, it is important to understand the load that the amplifier is required to drive. The internal front end of an unbuffered ADC typically consists of a sampling-input network controlled by a sample-and-hold clock signal which commands the input network to either sample the applied input signal or hold the input state for conversion (*Figure 4*).

This input network presents a changing capacitive load to the driver stage as it transitions repeatedly between sample and hold, causing transient charging spikes at the ADC input, which are made worse
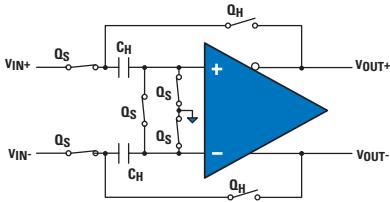
**Figure 4. Unbuffered ADC input sample and hold**

if the driving impedance is too high. If the driver stage is an amplifier, it has to settle after each transition and prepare for the next sample. It must remain stable with the changing capacitive load. The input is sampled on every clock cycle, so an amplifier output would have approximately half a clock cycle to settle, which equates to 5 ns for a 100 MHz clock. If an ADC driver is not used and the input signal has high source impedance, then failure to properly match that to the relatively low ADC-input impedance can lead to inaccuracy and conversion errors. This matching is a key function of the amplifier and channel-filter blocks. The amplifier provides the required output drive to charge the ADC sample-and-hold network, as well as enables other signal-conditioning functions such as level-shifting of the input signal into the range of the ADC input, and applying gain. The filter between the amplifier and ADC limits the noise bandwidth of the signal applied to the ADC, which would otherwise be the full bandwidth of the amplifier. It also isolates the capacitive load of the ADC input from the amplifier to maintain amplifier phase margin and stability, and attenuates the transient-charging glitches on the ADC input as the sample capacitance is switched. The filter should be designed to present a high-enough load to the amplifier to maximize amplifier-distortion performance while presenting low-enough impedance at high frequencies to the ADC to maximize the ADC's performance.

ADC Input Structures and the Choice of Driver

ADC inputs may be single-ended or differential. The single-ended input is most commonly found on lower-speed and lower-resolution ADCs. It is limited by susceptibility to noise, distortion, and DC-offsets which lead to reduced accuracy and

system performance. The differential-input ADC with complementary inputs provides immunity to common-mode errors, such as the noise injected by the sample-and-hold switching process since these errors appear on both inputs and are subtracted.

Similarly, any even-order distortion such as the 2nd harmonic distortion (HD2) created by mismatched input impedances, or other asymmetry within the signal path, is also subtracted. In a low-voltage system where the undistorted signal swing is limited by the operating headroom of active devices along the signal path, a differential-analog signal enables twice the low distortion-voltage swing compared to a single-ended signal. Allowing for a 3 dB increase in noise, a differential stage will net 3 dB of extra SNR from the 6 dB extra signal power that a doubled output swing provides. This improved SNR contributes to improved Signal-to-Noise-and-Distortion (SINAD) and SNR in the overall system.

$$A_V = \left(\frac{R_T}{R_S + R_T} \right) \left(1 + \frac{R_F}{R_G} \right)$$
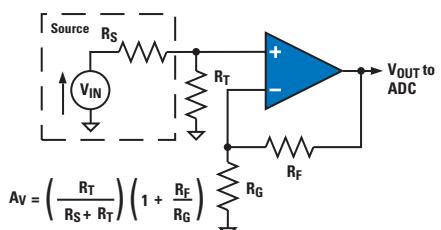
Figure 5a. Non-inverting single-ended amplifier

For the single-ended-input ADC, Current Feedback (CFB) amplifiers are well suited due to their low distortion, high drive, and ability to deliver wide bandwidth at higher gains. The non-inverting-amplifier configuration (*Figure 5a*) has the advantage of very-high-input impedance, which is easy to match to any source-output impedance, R_S, by adding a matching termination resistor, R_T. By contrast, in *Figure 5b*, the input impedance, R_S, of the inverting amplifier is $R_G//R_T$, where R_G's value interacts with R_F in determining the gain. R_T is optional and the input source can be directly matched to R_G without R_T. However, this can lead to a non-optimum value of R_F for a particular gain, bandwidth, and gain flatness, especially in the case

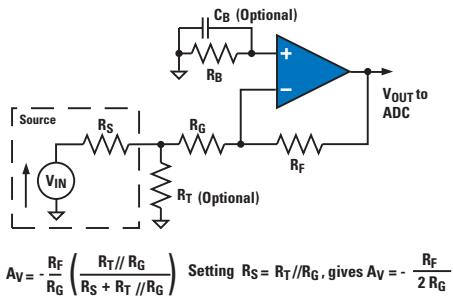## Selecting Amplifiers, ADCs, and Clocks for High-Performance Signal Paths

$$A_V = -\frac{R_F}{R_G}\left(\frac{R_T//R_G}{R_S + R_T//R_G}\right) \text{ Setting } R_S = R_T//R_G, \text{ gives } A_V = -\frac{R_F}{2\,R_G}$$

Figure 5b. Inverting single-ended amplifier

of a CFB amplifier. For a Voltage Feedback (VFB) amplifier, R_B is set equal to the effective impedance seen at the inverting input to cancel errors caused by input-bias current. In the case of high R_B values, C_B may be required to reduce high-frequency noise due to the amplifier input-noise current flowing through R_B.

In the inverting-amplifier configuration, the amplifier inputs are held at a fixed virtual ground while in the non-inverting configuration, the inputs see the full input-signal swing. Consequently, the inverting-amplifier-input stage sees a much smaller voltage on its inputs which reduces any distortion introduced by the input stage.

$$A_V = -\frac{R_F}{R_G}$$
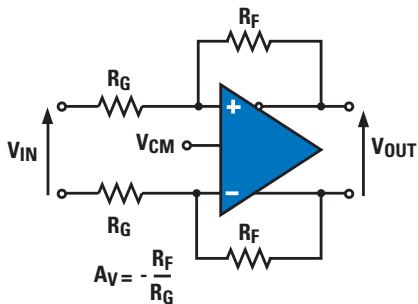
Figure 6a. Fully differential amplifier

In order to obtain the full performance, a differential-input ADC must be driven differentially. *Figure 6a* shows an integrated amplifier with differential outputs and differential inputs. Capable of either AC- or DC-coupled operation, the amplifier gain is set by four external resistors per the equation given in the diagram. The amplifier can also be driven by
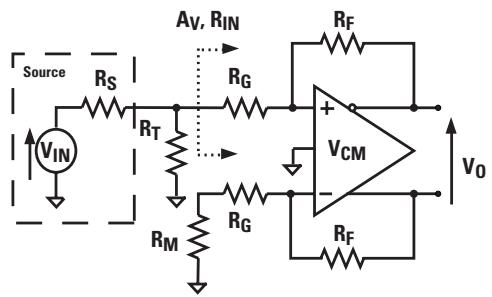
To match circuit input impedance R_{IN} to source impedance R_S, set $R_T//R_{IN} = R_S$, with $R_M = R_S//R_T$ then

$$A_V = \left(\frac{2(1-B_1)}{B_1 + B_2}\right) \qquad B_1 = \left(\frac{R_G}{R_G + R_F}\right)$$

$$R_{IN} = \left(\frac{2R_G + R_M(1-B_2)}{1 + B_2}\right) \qquad B_2 = \left(\frac{R_G + R_M}{R_G + R_F + R_M}\right)$$

Figure 6b. Single-ended input with differential output

a single-ended source, as in a single-to-differential amplifier, with the unused amplifier input grounded as shown in *Figure 6b*.

Resistors R_F and R_G should be well matched and strict symmetry should be observed in PC-board layout. This ensures optimum output balance, necessary for low distortion, and good Common Mode Rejection Ratio (CMRR) from this circuit. The output common-mode level is set by the V_{CM} common-mode control, independently of the input common-mode level, which is ideal for level-shifting the amplifier input signal to match the required ADC-input common-mode level. The fully-differential amplifier can be thought of as two forward-amplification channels plus a third feedback amplifier which senses the output common mode of the two forward channels and servos it to the level of the V_{CM} pin. The V_{CM} common-mode feedback loop forces the two outputs to be equal and opposite, thereby controlling the amplifier-output balance even when only one input channel is driven and the other input is grounded, as in the single-to-differential amplifier application.

Setting the output common-mode voltage with the V_{CM} pin also affects the amplifier-input common-mode voltage. It is essential to stay within

the datasheet-specified, input common-mode-voltage-range limits. For AC-coupled input operation, the input common mode will be at the same potential as the output common mode, or the V_{CM}-pin voltage. For DC-coupled single-to-differential operation, the input common-mode voltage is the output common-mode voltage divided down by R_F and R_G. This is not an issue with split-voltage supplies such as ±5V. However, for single-supply operation such as GND and +10V, the divided-down-output common-mode voltage, appearing as the input common-mode voltage, must not exceed the amplifier's rated operating-input common-mode-voltage range. Lack of headroom on the input can force the use of a negative rail lower than ground. For the best distortion performance, unlimited by amplifier input or output headroom, split ±5V supplies are recommended.

An ideal amplifier for ADC driving would be completely transparent to the ADC and not degrade its performance. Although this is a challenge, it is possible to minimize performance degradation. From a DC-specification perspective, the most fundamental amplifier requirement is that the output-voltage range of the amplifier supports the ADC-input-voltage range for full-scale output. From an AC perspective, the amplifier must have flat bandwidth and gain such that the wanted signal is not attenuated by the amplifier's frequency response, as well as low-enough noise and distortion levels that they do not impact the ADC's performance.

The required amplifier bandwidth is dictated by the input-signal-frequency spectrum to be processed and requirements for good distortion performance at high frequencies. The maximum signal frequency and the ADC's full-scale input-voltage level determine the required amplifier slew rate and Large Signal Bandwidth (LSBW). These specifications determine the channel bandwidth when driving the ADC input at full scale.

Due to the roll off of the amplifier open-loop gain, amplifier distortion starts to degrade at frequencies much lower than the amplifier LSBW. In the case of VFB amplifiers with a fixed-gain-bandwidth product, the amount of available gain for very-high-frequency signals can be limited. A CFB amplifier with relatively wide-gain independent bandwidth and excellent gain flatness is a good choice for very-high-frequency signals. The actual gain flatness required will depend on the application requirements.

Assuming all of the other AC and DC specifications can be met, noise and distortion will ultimately be the two main specifications of interest for a given ADC and amplifier combination since these determine the SINAD. The ENOB can be calculated from the SINAD using the equation:

$$\text{ENOB} = (\text{SINAD} - 1.76)/6.02, \text{ where SINAD is in dB}$$

Since distortion and noise are specified separately for the amplifier and ADC, it is necessary to look at how combining the amplifier with the ADC affects the overall subsystem's performance. The noise of the driving amplifier and the noise of the ADC are uncorrelated and can be rss-summed together for the purpose of analysis. In order for the amplifier noise not to degrade the ADC performance, the amplifier output noise over the frequency band of interest ideally should be at least 6 dB less than the ADC input noise.

The amplifier output-noise voltage spectral density measured in $V/\sqrt{Hz}$, is calculated by root-sum-squaring the output-noise voltage contributions arising from the amplifier's input-voltage noise and current noise, with the additional noise of any external resistors around the amplifier. The total noise seen at the ADC input depends on the channel bandwidth, so it is critical to optimize the design for minimum acceptable bandwidth in order to maximize noise performance. Unless limited by a channel filter, noise and distortion products from the entire amplifier bandwidth will all be sampled by the ADC and aliased back down into the 1st Nyquist zone. In addition to band-limiting to $f_S/2$, the channel filter is chosen to limit the amplifier-noise bandwidth and attenuate any distortion products.

Ideally, any in-band, amplifier-distortion products should be 6 dB lower than the ADC's own distortion products. Choosing the sample frequency carefully
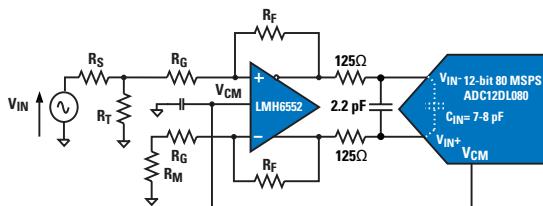
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with respect to the wanted signal can prevent distortion products appearing all over the baseband. In applications involving multiple closely-spaced-frequency tones, good Intermodulation Distortion (IMD) and related third-order Output Intercept Power (OIP3) are required from the amplifier. This minimizes difference-frequency distortion products that are otherwise created too close to the signal of interest to be filtered out. Ideally, any distortion specifications quoted for the amplifier should be for the signal level and load conditions presented by the application. In many applications where the dynamic range is increased by processing gain, distortion will be the number one concern in maximizing resolution.

The final stage before the ADC is the noise filter. The simplest solution for a DC-coupled baseband application is a passive first-order low-pass RC. For this simple first-order filter, the -3 dB frequency, $F_{-3\ dB}$, is given by the formula:

$$F_{-3dB} = \frac{1}{2\pi RC}$$

The 0.1 dB bandwidth is 0.15 x $F_{-3\ dB}$ and the effective-noise bandwidth for noise calculations is 1.57 x $F_{-3\ dB}$. Higher-order filters can be designed to meet specific passband-flatness needs based on various filter polynomials such as Butterworth, Bessel, and Chebyshev. These will give sharper roll off and lower noise bandwidths in addition to making it easier to meet the sharp roll-off requirements of *Figure 2c*. An example of a first-order low-pass filter is shown in *Figure 7* where National's new LMH6552 1 GHz fully-differential amplifier drives one half of a dual ADC12DL080 12-bit 80 MSPS ADC

Figure 8. LMH6552 and ADC12DL080 SFDR and SNR performance vs frequency

via a 65 MHz first-order low-pass filter, formed by the two series 125Ω-output resistors and the 2.2 pF-output capacitor in parallel with the ADC's input capacitance.

Figure 8 shows the LMH6552 and ADC12DL080 Spurious Free Dynamic Range (SFDR) and SNR performance versus frequency.

The LMH6552 amplifier is based on a CFB architecture and consequently delivers relatively constant bandwidth as the gain is varied. For example, the unity gain LSBW at 2 Vp-p output is 950 MHz, and for higher gains the BW reduction is small with 820 MHz at G = 2, 740 MHz at G = 4, and 590 MHz at G = 8. A VFB device would require almost 5 GHz gain-bandwidth product to achieve 590 MHz BW at G = 8.

The LMH6552 is ideal for a range of 8- to 14-bit applications depending on the specific speed, distortion, and noise requirements of the end application. Optimum performance is delivered on split ±5V supplies but the LMH6552 will also run on single supplies as low as single 5V. The amplifier input-voltage noise is $1nV/\sqrt{Hz}$ and the input-current noise is 19.5 pA/$\sqrt{Hz}$. The output noise is strongly influenced by the input-current noise and the value of the feedback resistor R_F and not so strongly by the input-voltage noise and closed-loop gain, as would be the case for voltage-feedback amplifiers. Consequently, the LMH6552 device can operate at much higher values of gain without

Figure 7. The LMH6552 Amplifier driving the ADC12DL080 converter

incurring a substantial noise-performance penalty simply by choosing a suitable R_F . The LMH6552 amplifier noise figure is 10.3 dB for a gain of nine. The second and third harmonic-distortion (HD2/HD3) specifications at 20 MHz are -92/-93 dBc respectively, equal to 14-bit converter distortion levels; while at well over 100 MHz, both HD2 and HD3 exceed the -60 dBc HD performance of high-speed 8-bit converters.

Alternatively, you may use the ADC14DS105 high-speed ADC and the LMK02000 clock conditioner with the LMH6552. The ADC14DS105 is a 14-bit dual 105 MSPS ADC with serial LVDS outputs, featuring full power bandwidth of 1 GHz and the industry's highest SFDR of 81 dB at 240 MHz. The LMK02000 clock conditioner incorporates the industry's highest performance PLL and divider blocks and delivers the industry's lowest additive jitter, as low as 20 fs. Combined with the LMH6552, these devices are suitable for up to 40 MHz Nyquist frequency baseband applications or oversampled baseband applications on signal bandwidths of 26.5 MHz and lower. A second or higher order low pass filter is recommended before the ADC in order to minimize the effect of noise and distortion on system performance. Together, these devices are ideal for use in communications applications such as in low IF narrowband sampling below 70 MHz IF where a fourth or higher order bandpass filter would be recommended.

For under-sampled IF applications, *Figure 9* shows National's new fully-differential LMH6515 Digital Variable Gain Amplifier (DVGA) driving the ADC14155 converter. The filter in this example is a second-order RLC bandpass filter which is tuned to the desired IF frequency by appropriate selection of the output inductor, L, and output capacitor, C, according to the equation:
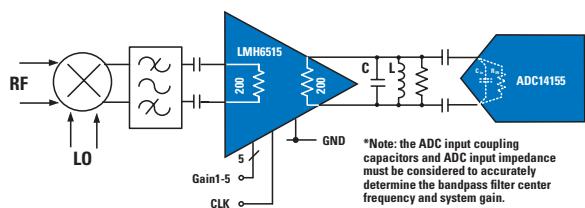
$$F_{-3dB} = \frac{1}{2\pi\sqrt{LC}}$$

The LMH6515 provides digitally-programmable gain from -7 dB to 24 dB in 1 dB steps, with 600 MHz of bandwidth, 37 dBm OIP3 at 150 MHz, and 8.3 dB-noise figure for 100Ω total load. The gain selectability of the LMH6515 allows better utilization of the ADC full-scale range and results in a larger system dynamic range. The ADC14155 has 1.1 GHz full-power bandwidth and delivers 11 ENOB at 238 MHz. The combination of the ADC14155 and LMH6515 is suitable for a wide range of IF-sampled communication applications.

Another option is to use the ADC14V155 high-speed A/D converter and LMK03001 clock conditioner with the LMH6515. The ADC14V155 is a 155 MSPS ADC with 1.1 GHz full-power bandwidth and features the industry's best SFDR above 170 MHz input frequency. At 238 MHz, the SFDR is 85 dB. The LMK03001 is the industry's first complete clock-conditioner chip and features the industry's best jitter performance: 200 fs rms from 10 Hz to 20 MHz bandwidth in clock-generator mode and 400 fs from 12 kHz to 20 MHz bandwidth in jitter-cleaner mode.

This article has shown that sampled-data systems can be divided into two main types: Nyquist-sampled and under-sampled. Depending on the type of system a given application may use, a DC-coupled wideband amplifier or an AC-coupled, narrow-band IF amplifier may be used in order to drive the ADC. As illustrated, National has a variety of solutions that can meet the noise and distortion needs of these various systems whether it be for 8- to 10-bit GSPS or for higher-resolution, 12- to 14-bit at >100 MSPS. ■

Figure 9. LMH6515 and AD14155 IF-sampled application

Gigahertz Differential Amplifiers for All Speeds and Resolutions

LMH6552 High-Speed Differential Amplifier from the PowerWise® Family Offers 1.5 GHz Bandwidth at 112.5 µW Power Consumption

LMH6552 Features

- 1.5 GHz bandwidth at $A_V=1$; 750 MHz at $A_V=8$
- 450 MHz, 0.1 dB flatness
- -90 dB THD at 20 MHz, -74 dB THD at 70 MHz
- 10.3 dB noise figure
- 10 ns settling time to 0.1%
- 5 to 12V operation
- Ideal match for 8/10/12/14-bit high-speed ADCs
- Reference board available with LMK02000 clock conditioner and ADC14DS105 high-speed ADC

LMH6555 Features

- 1.2 GHz bandwidth
- -50.5 dBc THD at 750 MHz
- 15 dB noise figure
- 13.7 dB fixed gain
- 3.3V operation
- Ideal match for 8-bit ADCs up to 3 GSPS, such as the ADC08(D)1000/1500/3000 family
- Reference board available with LMX2531 clock conditioner and ADC083000 3-GSPS ADC

Low IF Receiver Subsystem
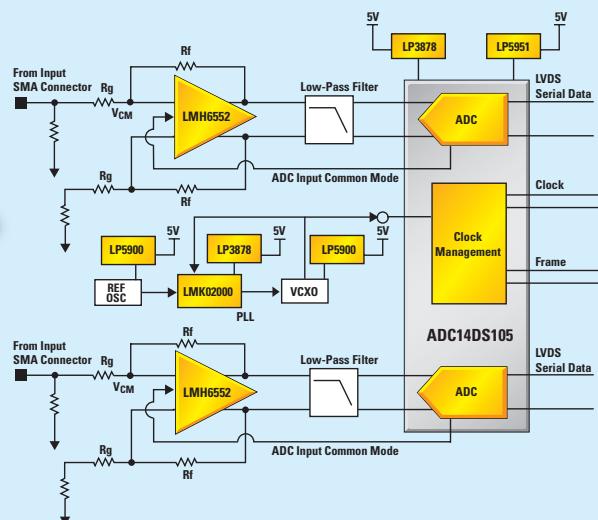
Low IF Receiver Subsystem Measured Performance
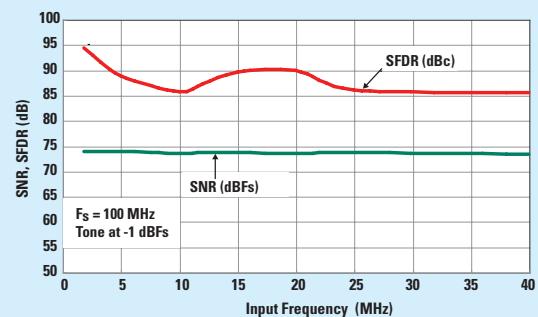
Ideal for use in communications receivers, high-speed differential signaling, intermediate frequency amplifiers, and data acquisition front ends

For reference design, samples, datasheets, and more information on Signal-Path and PowerWise® solutions, contact us today at:

http://signalpath.national.com

Or call: 1-800-272-9959

3 GSPS 8-Bit ADC with Over 3 GHz Full Power Bandwidth

1.9W Ultra Low Power ADC from the PowerWise® Family is Easily Interleaved for 6 GSPS Operation

ADC083000 Features

- 1.9W operating power consumption is less than half competitive solutions
- 3 GHz full power bandwidth
- Bit Error Rate (BER): 10^{-18}
- Single supply operation: +1.9V
- Integrated 1:4 output demultiplexer
- Adjustable input full-scale range and offset
- Guaranteed no missing codes
- Integrated 4K capture buffer available (ADC08B3000)

ADC083000 Benefits

- Clock phase adjust for multiple ADC synchronization allows 6 GSPS operation with 2 interleaved ADCs
- Test pattern simplifies high-speed data capture
- Serial interface for controlling extended functionality
- Reference board available with LMX2531 clock conditioner and LMH6555 high-speed amplifier, for inputs between DC and 750 MHz
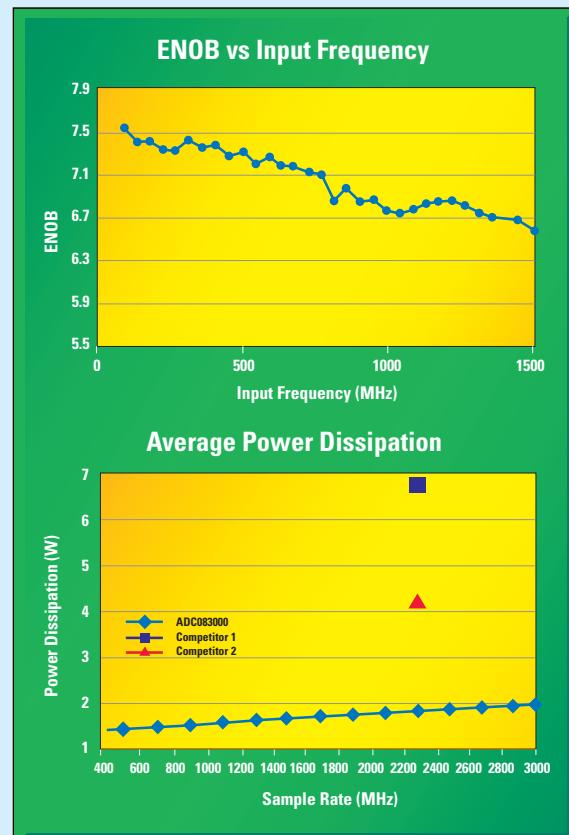
Ideal for use in communications infrastructure, test and measurement equipment, data acquisition systems, and military or consumer applications such as software-defined radio

ENOB vs Input Frequency

Average Power Dissipation

Design Tools

WEBENCH® Signal Path Designer® Tools

Design, simulate, and optimize amplifier circuits in this FREE online design and prototyping environment allowing you to:

- Synthesize an anti-alias filter
- Select the best amplifier/ADC combo for your system specs
- Make trade-offs based on SNR, SFDR, supply voltage
- Simulate real-world operating conditions using SPICE
- Receive samples in 24 hours

webench.national.com
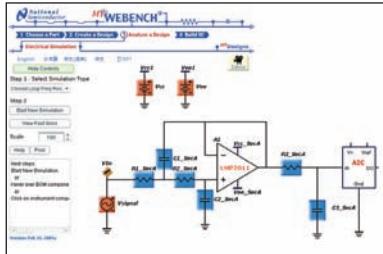
WaveVision 4.1 Evaluation Board

Test and evaluate A/D converters with National's easy-to use WaveVision 4.1 evaluation board. Each evaluation board comes complete with USB cable and support software.

Features and benefits:

- Plug-n-play ADC evaluation board
- USB 2.0 interface to PC
- PC-based data capture
- Easy data capture and evaluation
- Highlighted harmonic and SFDR frequencies
- Easy waveform examination
- Produces and displays FFT plots
- Dynamic performance parameter readout with FFT
- Produces and displays histograms

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