AN-2146 Power Design for SDI and other Noise Sensitive Devices

ABSTRACT

This application report discusses various solutions for meeting the power requirements of serial digital interface (SDI) video components.

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1 Overview

Power supply design for high-speed devices can often drive the need for low noise, low ripple voltage rails. Serial digital interface (SDI) components, like other high-speed devices require the control of output voltage (V_{CC}) ripple and noise in order to fully maximize their performance. The V_{CC} ripple and noise requirements for individual SDI components are discussed in detail in application note AN-2145 (SNOA560). Each SDI component within the signal path can have differing V_{CC} ripple and noise requirements ranging from 5-100mV. There are numerous options for converting power for V_{CC}, which can result in a low ripple, low noise voltage rail.

If specified, the manufacturer's datasheet often lists the output voltage ripple for power regulators at 20MHz measurement bandwidth. This is fine for comparative purposes, but not when evaluating power components for SDI applications. Doing so misses the high frequency switching artifacts that are typically seen on an output voltage measurement as spikes or noise. Those higher frequency switching-related artifacts cannot be ignored when considering the power requirements for SDI components which are, by their function, high bandwidth devices.

Figure 1 shows the difference between an output voltage ripple measurement of a buck converter (24V to 3.3V@ 2A) with 20MHz measurement bandwidth (BW) and with full BW. While the full bandwidth ripple/noise amplitude of about 18mV p-p is good, it may not be sufficient for some SDI applications and could limit their performance. For discussion purposes in this article, all ripple and noise references will be full BW unless noted otherwise.
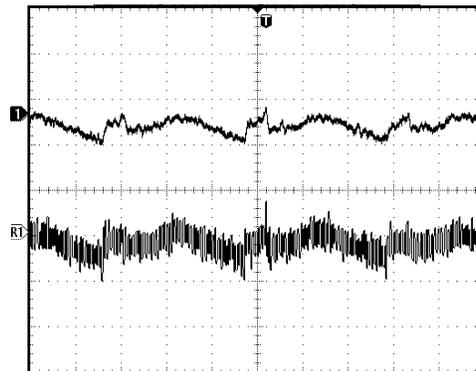

Figure 1. 20 MHz BW (top) and 300 MHz BW (bottom)

2 Switch-Mode Power Solutions

There are many options for converting power for SDI and other devices in a product. As a result, many designers are unsure about which power supply topology is most efficient or, in the case of powering SDI, which option has the lowest V_{CC} ripple and noise. Power converters like Texas Instruments SIMPLE SWITCHER® Power Modules are a good option for powering SDI and other circuits requiring low V_{CC} ripple and noise. The modules shown in Table 1 include an internal inductor and MOSFETs and have output ripple/noise performance suitable for many of the SDI components, without the need for additional filtering. However, the ripple and noise requirements for 3G reclockers and cable drivers can be < 5mV and are best met using a secondary stage like a linear/low drop-out regulator (LDO) or a Pi filter, which will be discussed later in this article.

Table 1. Select TI Power Modules

Device	Output Current	Input Voltage	Output Voltage	Peak Efficiency	Ripple (p-p)	Package Dimensions (including leads)
LMZ10503/4/5	3/4/5A	2.95 to 5.5V	0.8 to 5V	96%	6mV	10.16 × 9.85 × 4.57mm
LMZ14201/2/3	1/2/3A	6 to 42V		90%	16mV	
LMZ22005/6	5/6A	6 to 20V	0.6 to 6V	92%	20mV	
LMZ22008/10	8/10A	6 to 20V	0.6 to 6V	93%	40mV	15 × 15 × 5.9mm

When designing any switch-mode power supply (SMPS), including a power module, it's important to select output capacitors for minimizing voltage ripple. For many SMPS, this means selecting a sufficient amount of output capacitance with low ESR (effective series resistance). Voltage ripple is a function of the inductor ripple current, the switching frequency (F_{SW}) and the output capacitor's ESR. Therefore, minimizing the ESR in the output capacitors will minimize the output voltage ripple.

The output voltage noise, also known as switching artifacts, is another matter. This is typically related to a number of factors such as PCB layout of the power supply, turn-on and turn-off transitional times of power transistors, reverse recovery of diodes (as applicable) and the inter-winding capacitance of the switch-mode inductor. The resulting noise-related issues are difficult to predict and mitigate, making the choice of a power module attractive, given most of these issues are addressed in the module's design. However, even power modules can have switching-related noise on their outputs, including the modules shown in Table 1.

In addition to the large value of capacitance used to filter the voltage ripple, adding a small value ceramic capacitor on the output can help reduce the voltage "spikes" that are often seen on the output. There are numerous theories on selecting the value of this capacitor, but selecting the value based on its resonant frequency (Equation 1) and matching the resonant frequency to that of the ringing of the voltage spike is effective. In general, the goal is creating a low impedance AC path to ground for this high frequency noise. This capacitor is typically effective with a value of 1µF or less. The benefit this capacitor contributes will be enhanced if the capacitor's parasitic inductance, along with the inductance contributed by the PCB layout, is limited.

$$f = \frac{1}{2p\sqrt{LC}}$$

(1)

The inductance for a small (0603 or 0805 size) ceramic capacitor is typically about 1nH of inductance, so it's of little consequence. The parasitic inductance resulting from the layout of the capacitor can be a bigger contributor given trace inductance can be about 10nH/in. and each via will add about another 1nH. So, it's best to minimize trace length by dropping power and ground vias to their respective planes at the capacitor mounting pads, which should be placed right at the output of the regulator. Placing this capacitor on the board, even if unmounted is cheap insurance.

3   LDOs Low Noise and High PSRR

LDO regulators are a common choice for powering a quiet voltage rail, and for good reason, given their high power supply rejection ratio (PSRR). This is often a good decision, but without proper care in the selection of the LDO, the results could be far less than desired. The PSRR is the ratio of the input power supply noise/ripple and the amount that is transferred to the output of the regulator in decibels (dB). The PSRR of a LDO is characterized by imposing a sinusoidal signal on the DC input voltage and varying its frequency over some range and measuring the amount of signal passed through to the output.

Of course, the ripple and noise on the output of a SMPS that feeds a LDO is not sinusoidal, but instead is a complex mixture of ripple and switching-related artifacts. If viewed in the frequency domain, one would see switching related noise well above F_{SW}. This puts considerable demand on the LDO for higher frequency signal attenuation. However, the bandwidth limitation of the internal error amplifier in an LDO results in a PSRR that rolls off with frequency.

The LDO with the PSRR curve in Figure 2, shows the PSRR at 1 kHz = 75dB, however, at 1MHz the PSRR is reduced to 22dB. Many LDOs have a PSRR near zero above a few hundred kilohertz. Careful LDO selection is important, otherwise, the result will be more noise and ripple on the output of the LDO than expected.
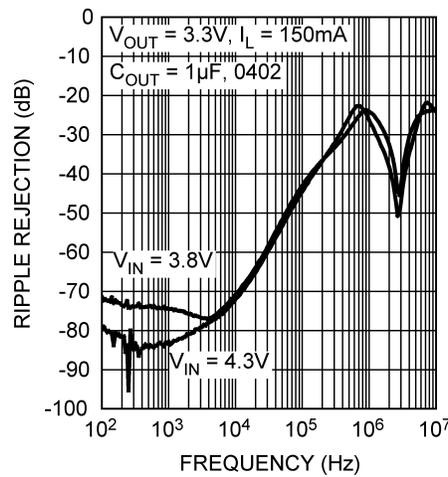
Figure 2. LP5900 PSRR

The LDOs in Table 2 have sufficient PSRR in the frequency range of most contemporary switch-mode supplies. Based on the PSRR curves intrinsic to an LDO's architecture, the LDO should be considered a high-pass filter for power-related input noise. Understanding the frequency content of the noise and ripple on the voltage input of the LDO will help in selecting a regulator with sufficient PSRR to power noise sensitive devices.

Table 2. Low Noise LDO Selection (2.5V and 3.3V out)

Device	Output Current	Input Max Voltage	Drop-out Voltage	Output Voltage	PSRR (dB)	PSRR (dB) @ 500KHz
LP3999	150mA	6V	60mV	2.5V, 3.3V	-60	-10
LP5900	150mA	5.5V	80mV	3.3V	-75	-30
LP5904	200mA	5.5V	95mV	1.2V-4.4V (25mV steps)	-85	-50
LP3997	250mA	6V	140mV	3.3V	-61	-25
LP3878	800mA	16V	105mV	ADJ	-68	-27

4   Power π (Pi) filter

When the PSRR of a LDO is incapable of rejecting higher frequency noise, consider using a Pi filter on the output of a SMPS or between a SMPS and a LDO as shown in Figure 3. A Pi filter is typically comprised of two ceramic capacitors and an inductor or ferrite bead as shown (C2, L1 and C3) in the schematic. The choice of whether to use an inductor or ferrite bead in the Pi filter depends on the frequency of the voltage ripple or "noise" that needs to be filtered out. In general, inductors are a good choice for further reducing voltage ripple, whereas ferrite beads are useful for filtering high frequency content from power; like switching-related artifacts, that is, voltage spikes.

Wound inductors, on the other hand, don't serve well for filtering frequencies that are much above F_{SW}, since their inter-winding capacitance acts like a high-pass element. It is the inter-winding capacitance of the switch-mode inductor that passed the noise to the output in the first place. Ferrite beads have low DC resistance (<0.01Ω) and also have peak impedances of >1KΩ which is specified at a given frequency (for example, 1KΩ @ 100MHz). The ferrite's impedance profile is specified by way of an impedance curve as a function of frequency.
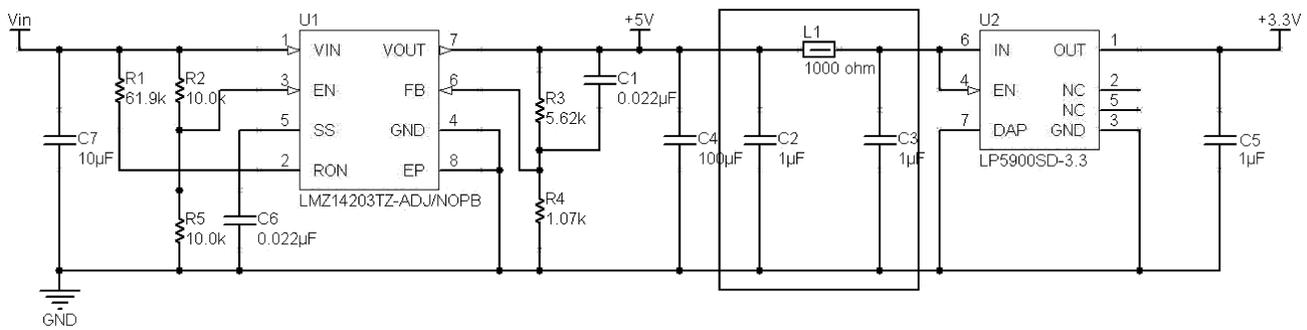
Figure 3. Example of a Low Noise/Ripple Voltage Source

The Pi filter in the circuit shown in Figure 3 provided about -15dB of ripple and noise attenuation, as seen in the oscilloscope image in Figure 4. The voltage spikes shown on the bottom two traces are the switching artifacts often seen and referenced in this article. The LP5900 provided another 6dB of attenuation resulting in about 3.5mVp-p of ripple and noise at the output of the LDO. The amount of actual attenuation provided by a Pi filter or LDO is dependent on both the characteristics of the components and the frequency of the noise imposed on the DC input.

A compact circuit layout of the Pi filter and use of 0603 (or smaller) capacitors, in order to minimize parasitic inductance, are beneficial in reducing the voltage spikes. Placing the Pi filter, after the LDO, at the point of load can also be beneficial to filter out any noise coupled onto the power trace in route. Using the LMZ15054, with its lower output ripple and noise, in place of the LMZ14203 for the circuit in Figure 3 yielded about 2.5mV p-p of output ripple and noise. The Pi filter is a low pass filter, which when properly combined with a LDO can result in voltage and ripple levels sufficient for the most sensitive SDI components.
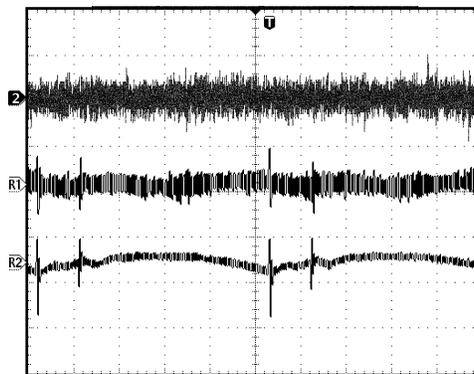

Figure 4. LMZ14203 with Pi Filter and LP5900

Measuring small amplitude ripple and noise requires some care. The use of 10x oscilloscope probes with ground leads inches in length will not suffice. The large loop area formed by the long ground lead will act like an antenna, which picks up switching noise that is not real voltage ripple amplitude. A scope probe like the one shown in Figure 5 will provide accurate measurements and pick up very little noise. This probe uses a piece of wire wrapped around the ground shaft in order to create a small loop area, which minimizes measurement error.

For low amplitude measurements (<10mV/div), like those shown in Figure 4, a custom 1x probe was made from a piece of 50Ω; coaxial cable. It was AC-coupled (1µF X5R for example) at the point of measurement, at the output capacitor, and was connected at the scope with an external 50Ω pass through terminator.
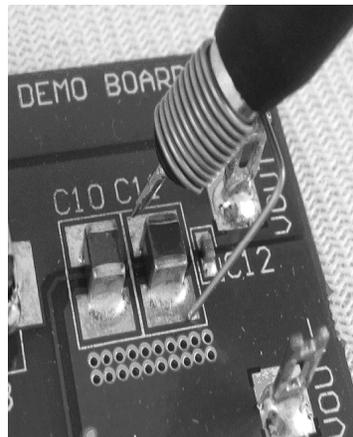
Figure 5. Good Ripple/Noise Scope Probe (cropped version of 30092806)

In conclusion, it's important to understand the V_{CC} ripple and noise requirements for the component being powered. Consider the higher frequency noise and voltage spikes related to switching artifacts on the V_{CC} rail and how best to minimize or reject them. Care in selecting the right power product for the application is important in order to fully maximize the performance of an SDI design. Power modules like those from Texas Instruments are a good choice.

Selecting the right power converter is still not sufficient; the PCB layout has a big role in minimizing output noise. Finally, consider using a LDO with sufficient PSRR at >F_{SW} and a Pi filter for any remaining noise. Figure 6 provides a visual summary of the V_{CC} ripple and noise requirements, and possible high-level options for powering them. For ripple and noise requirements above 30mV, a SMPS will satisfy that need, though some care in the design is still required, see *AN-1950 Silently Powering Low Noise Applications* (SNOA543). Beyond that, a LDO and or a Pi filter will be required as discussed.

Since low noise power design is an inexact practice (given the number of parameters, parasitic and otherwise that can influence the final result), it is good practice to prototype the design. A manufacturer's evaluation boards are a convenient means for evaluating the design.

All measurements for this article were made with 300MHz BW, limited by the scope, unless noted otherwise.
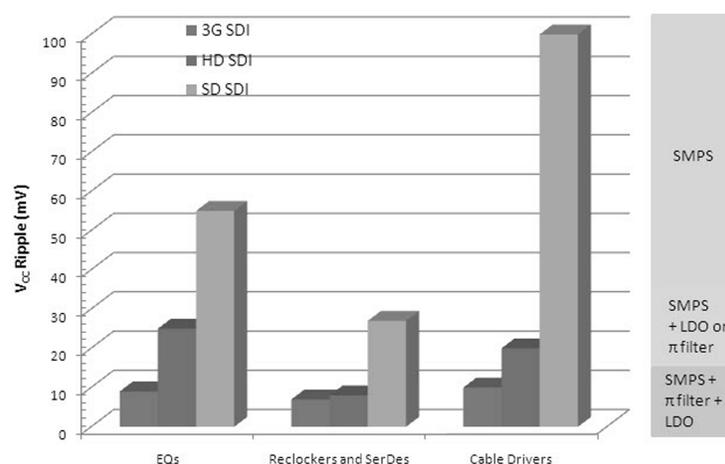

Figure 6. SDI V_{CC} Ripple/Noise and Solutions

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