Application Report
SNLA285–October 2017

Simplifying 4K SDI Video Design with a Bidirectional I/O

ABSTRACT

In 4K serial digital interface (SDI) video designs, flexibility, scalability, and cost savings are essential to maximize design reuse and develop an extensive 12G-SDI portfolio. A bidirectional input/output (I/O) addresses these critical needs. This application note explains how the features and diagnostic tools of the LMH1297 12G-SDI bidirectional I/O enable various SDI design benefits. This application note also provides several application examples where the LMH1297's versatility simplifies 4K video design.

Contents

List of Figures

List of Tables

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1 Introduction

As 4K video becomes the norm for the professional video industry, high-quality serial digital interface (SDI) components and meticulous board layout are imperative for a high-performance end product. In addition, flexibility, scalability, and cost savings are necessary to maximize design reuse. These principles are especially applicable when expanding a 12G product portfolio or making the transition from 3G-SDI to 12G-SDI.

A bidirectional input/output (I/O) addresses these critical needs. This application note explains how a bidirectional I/O works and how it benefits video design. In addition, this application note highlights TI's LMH1297 bidirectional I/O performance data and application examples that demonstrate the bidirectional I/O's versatility.

2 What is a Bidirectional I/O?

A bidirectional I/O is a device that is configurable as either a receive cable equalizer (EQ) or a transmit cable driver through the same port. Rather than use a stand-alone cable EQ or cable driver to designate a port as input or output only, the bidirectional I/O enables the port direction to be determined after the board layout is complete.

NOTE: A bidirectional I/O functions as either cable EQ or cable driver at any one time. The device cannot behave as both cable EQ and cable driver simultaneously.

2.1 The Original SDI Bidirectional I/O: LMH0387

The first SDI bidirectional I/O was released in 2010 for 3G-SDI applications by National Semiconductor (currently TI) with the LMH0387. The LMH0387 combines the silicon die for both cable EQ and cable driver into a single chip, enabling flexibility to configure one port as either input or output as shown in Figure 1.

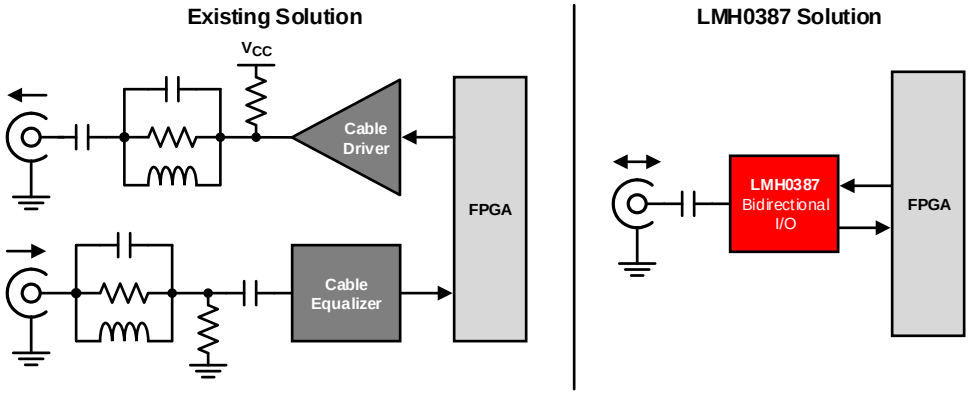

Figure 1. National Semiconductor's LMH0387, the SDI Industry's First Bidirectional I/O Device

However, there are some inherent performance tradeoffs compared to stand-alone cable EQs and cable drivers. Because the LMH0387 uses a Multi-Chip Module (MCM) approach to enable bidirectional I/O functionality, the LMH0387 IC is more than double the size of a stand-alone 3G-SDI cable EQ or cable driver. In addition, the LMH0387 exhibits a shorter cable reach compared to stand-alone cable EQs such as the LMH0394.

2.2 TI's 12G-SDI Bidirectional I/O: LMH1297

As data rates quadruple from 3G to 12G, several key trends have emerged. One, signal conditioning devices are critical to achieve optimal performance. Two, there is a greater demand for on-chip integration due to increasing system port density and limited board space for discrete components.

With these technological trends at 12G in mind, TI released the LMH1297 in 2017. This next-generation bidirectional I/O supports SDI rates up to 12G with improved performance and integrated features. A detailed view of key LMH1297 components is shown in Figure 2.

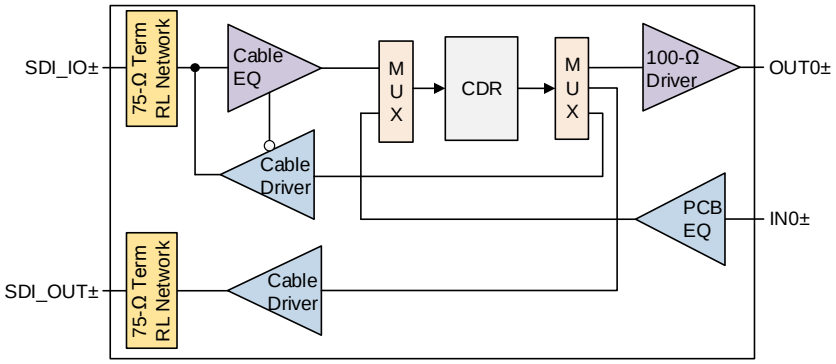

Figure 2. Internal Architecture of LMH1297 Bidirectional I/O

NOTE: Connections to SDI_IO or SDI_OUT are considered as “line-side” with 75-Ω single-ended characteristic impedance. Connections to IN0 and OUT0 are considered as “host-side” with 100-Ω differential characteristic impedance.

The signal paths of the LMH1297 in Equalizer (EQ) Mode and Cable Driver (CD) Mode are shown in Figure 3 and Figure 4, respectively.

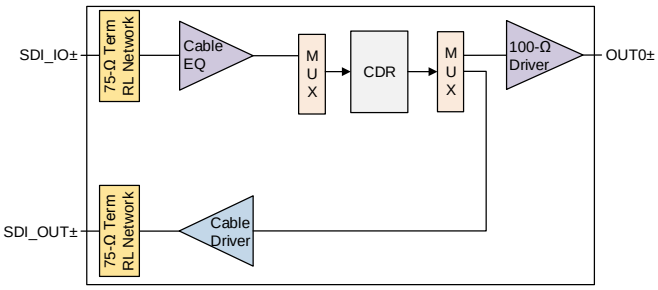

Figure 3. LMH1297 Signal Path in EQ Mode

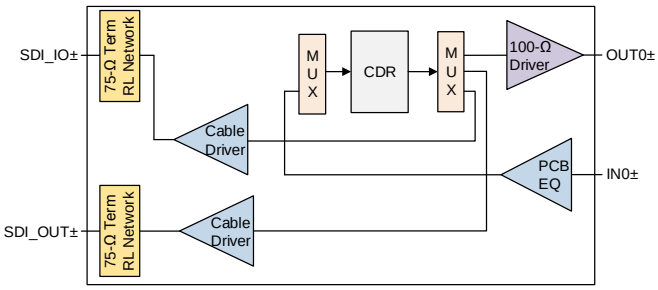

Figure 4. LMH1297 Signal Path in CD Mode

The LMH1297 features a 75-Ω return loss network, integrated terminations, adaptive cable EQ, and SMPTE-compatible cable driver, similar to the LMH0387. Unlike the LMH0387, there is a higher level of integration within the LMH1297. The LMH1297 integrates a reclocker, additional 75-Ω loop-through cable driver output, and a 100-Ω loopback printed circuit board (PCB) driver output. The reclocker reduces high-frequency input jitter and automatically determines the cable driver output slew rate and pre-emphasis levels. The additional outputs improve system diagnostic capability and efficiently expand signal distribution.

Furthermore, TI’s bidirectional I/O is implemented on a single-die solution instead of an MCM. With the single-die approach, the LMH1297 achieves performance equivalent to or exceeding that of many other stand-alone cable EQs and drivers. This also allows the LMH1297 to fit in a 5 mm-by-5 mm very thin quad flat no-lead (WQFN) package.

A side-by-side comparison of the LMH1297 family compared to the LMH0387 is shown in Table 1.

Table 1. LMH1297/0397 vs. LMH0387 Comparison

FEATURES	LMH1297	LMH0397[1]	LMH0387
Supported Data Rates	12G, 6G, 3G, 1.5G, 270M	3G, 1.5G, 270M	3G, 1.5G, 270M
Cable Reach in EQ Mode, B1694A (m)	75m @ 12G 120m @ 6G **200m @ 3G** **300m @ HD** **600m @ SD**	**200m @ 3G** **300m @ HD** **600m @ SD**	120m @ 3G 200m @ HD 400m @ SD
Adaptive Cable EQ	Yes	Yes	Yes
Integrated Return Loss Network	Yes	Yes	Yes
Integrated Reclocker	**Yes**	**Yes**	No
Configurable Slew Rate Cable Driver	Yes	Yes	Yes
Line-Side 75-Ω Loop-Through Output	**Yes**	**Yes**	No
Host-Side 100-Ω Loopback Output	**Yes**	**Yes**	No
Programmability	SMBus, SPI, Pin	SMBus, SPI, Pin	SPI, Pin
Package Size	**5x5 mm, QFN-32**	**5x5 mm, QFN-32**	7x7 mm, TLGA-48

(1) The LMH0397 is a pin-compatible 3G-SDI version of the LMH1297.

3 Bidirectional I/O System Benefits

Bidirectional I/Os come with numerous SDI system-level benefits from both a design simplicity and product differentiation standpoint. This section elaborates on the inherent value of bidirectional I/Os versus traditional designs in an SDI system.

3.1 Increased Design Flexibility

Traditional SDI designs have a fixed number of input and output ports. Because cable EQs and cable drivers are not interchangeable at the same port, designing a new system is necessary whenever a different combination of inputs and outputs is required. With a bidirectional I/O, multiple configurations of inputs and outputs are supported by the same design, as illustrated in Figure 5.

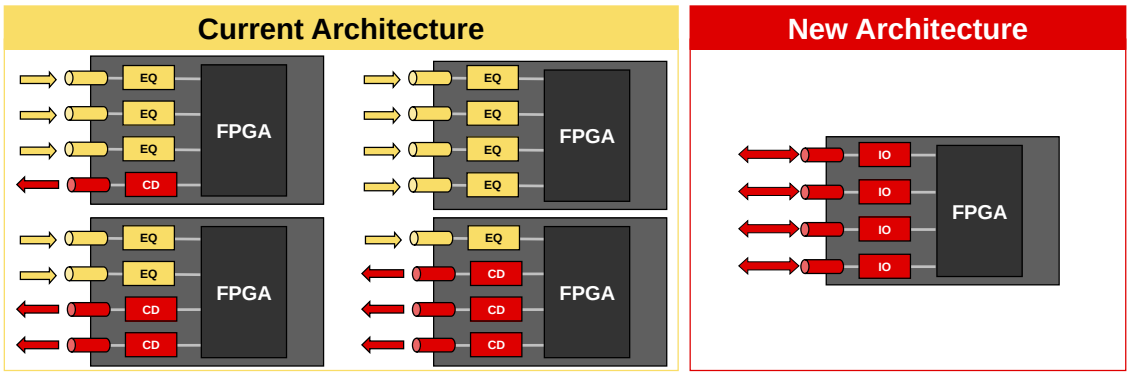

Figure 5. Multiple Input and Output Port Configurations Supported by a Single Bidirectional I/O

TI's 12G bidirectional I/O, the LMH1297, also enables dynamic port provisioning, meaning that end users can configure the port as an input or output in real-time through pin or register control. This design flexibility and scalability reduces both overall development time and the cost of stocking unique boards to support each port-configuration combination.

3.2 Board Space and Bill-of-Materials Cost Reduction

In a traditional design, two ports support input and output functionality, resulting in a four-chip solution. A bidirectional I/O minimizes board space by reducing the overall number of ports. With the LMH1297 family, only one port is needed, resulting in a single-chip solution. Comparing these two design approaches in Figure 6, a bidirectional I/O significantly reduces the number of board components.

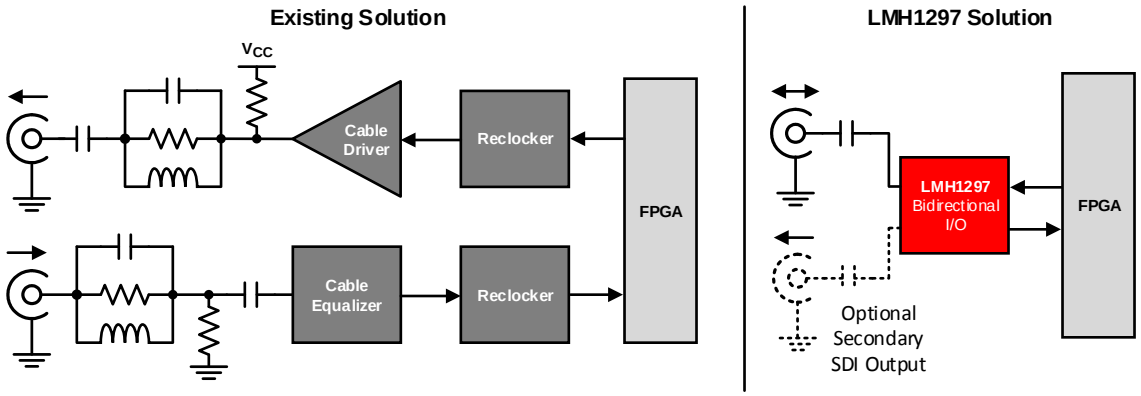

Figure 6. Ports and External Passive Components Reduced by a Single Bidirectional I/O

In addition to reducing the solution size to a single IC, TI's 12G bidirectional I/O takes BOM cost savings a step further with an integrated reclocker, return loss network, and terminations. The integrated reclocker ensures a clean output signal with minimal jitter. Meanwhile, the integrated return loss network and terminations eliminate the need for an external return loss network, not to mention time spent fine-tuning these network parameters.

3.3 TI's Easy SDI Upgrade Path

Before taking the first steps to designing with a bidirectional I/O, it is worth considering whether alternative upgrade options are available to prepare current designs for the next generation. As the SDI community trends upward from 3G-SDI to 12G-SDI, having a pin-compatible upgrade path minimizes board redesigns and future-proofs current SDI products.

The LMH1297 comes with several pin-compatible alternatives in an identical package for easy upgrade. These alternatives are also software compatible. As shown in Figure 7, the LMH0397 is a 3G bidirectional I/O with an integrated reclocker, while the LMH1228 and LMH1208 are 12G dual cable drivers.

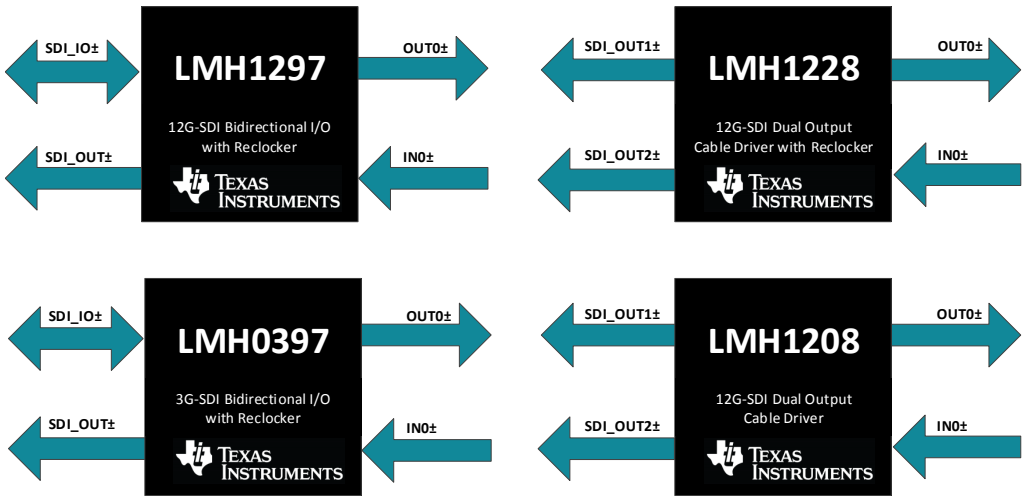

Figure 7. LMH1297 Pin and Software Compatible Portfolio

4 LMH1297 Device Performance

4.1 EQ Mode, Cable EQ Performance

In EQ Mode, the LMH1297 is capable of achieving equivalent cable reach to that of the LMH1219, a stand-alone 12G cable EQ. Table 2 shows the maximum cable reach achieved with BER ≤ 10E-12 by the LMH1297 with Belden 1694A cable using a PRBS-10 pattern. Longer cable reach can be achieved by using cables with a lower insertion loss profile.

Table 2. Belden 1694A Cable Reach with LMH1297

DATA RATE	SDI_OUT DISABLED
12G-SDI (11.88 Gbps)	75 m
6G-SDI (5.94 Gbps)	120 m
3G-SDI (2.97 Gbps)	200 m
HD-SDI (1.485 Gbps)	300 m
SD, DVB/ASI (270 Mbps)	600 m

Figure 8 and Figure 9 show eye diagrams of OUT0 at 12G, taken before and after the reclocker at the maximum Belden 1694A cable reach.

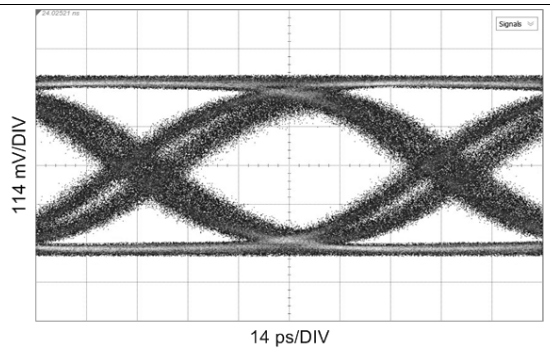

Figure 8. EQ Mode, Cable EQ Output Only, 11.88 Gbps, 75-m B1694A, SDI_OUT Disabled, PRBS-10

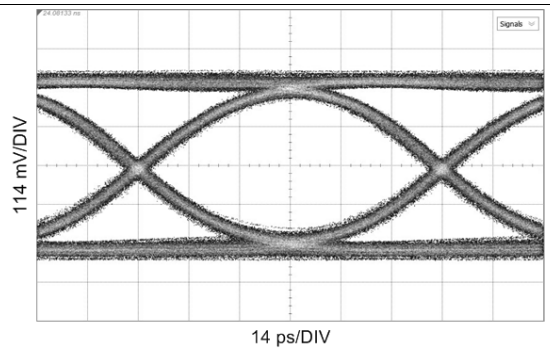

Figure 9. EQ Mode, Cable EQ and Reclocker Output, 11.88 Gbps, 75-m B1694A, SDI_OUT Disabled, PRBS-10

4.2 CD Mode, PCB CTLE Performance

In CD Mode, the LMH1297 is capable of achieving equivalent FR4 trace reach to that of the LMH1218, a stand-alone 12G cable driver. The LMH1297's adaptive PCB CTLE equalizes up to –27 dB of PCB trace loss, allowing convenient board design with FR4 instead of higher cost PCB material such as Megtron-6 or Rogers RO4000®. Table 3 shows the performance of the LMH1297 adaptive PCB CTLE with BER ≤ 10E-12 using a 12G-SDI EQ pathological pattern. Longer PCB trace can be achieved by using a PCB material with a lower insertion loss profile.

Table 3. LMH1297 PCB CTLE Performance with 12G-SDI EQ Pathological Pattern

TRACE LENGTH (in.)	SDD21 (dB) at 6 GHz	CTLE INDEX	HEO (UI)(1)	VEO (mV)(1)
5	–4.5	0x00	0.75	450
10	–9.0	0x10	0.72	425
15	–13.5	0x50	0.67	425
20	–18.0	0x50	0.63	375
25	–22.5	0x51	0.63	363
30	–27.0	0x94	0.58	325

(1) Horizontal eye opening (HEO) and vertical eye opening (VEO) are measured by the integrated reclocker.

Figure 10 and Figure 11 show eye diagrams of SDI_IO at 12G, taken before and after the reclocker with 20" FR4 input trace and a PRBS-10 pattern.

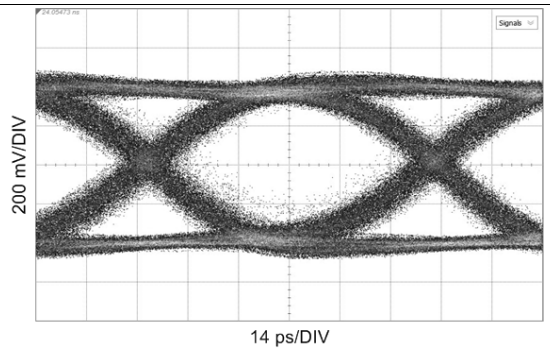

Figure 10. CD Mode, PCB CTLE Output Only, 11.88 Gbps, 20” FR4 Input, PRBS-10

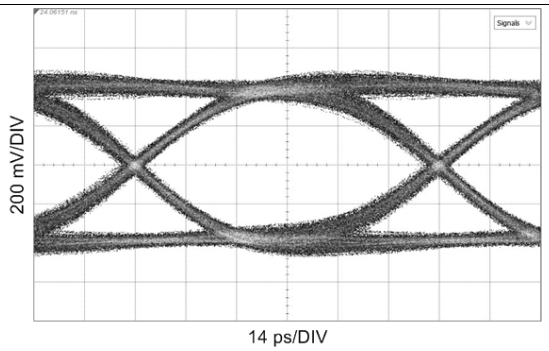

Figure 11. CD Mode, PCB CTLE and Reclocker Output, 11.88 Gbps, 20” FR4 Input, PRBS-10

4.3 CD Mode, Cable Driver Performance

In CD Mode, the line-side cable driver output is compatible with SMPTE requirements. Both SDI_IO and SDI_OUT cable driver outputs meet slew rate, jitter, and VOD amplitude SMPTE requirements from SD to 12G-SDI. Figure 12 shows results taken from the LMH1297EVM cable driver output at 12G, with comparisons with key SMPTE cable driver requirements listed in Table 4.

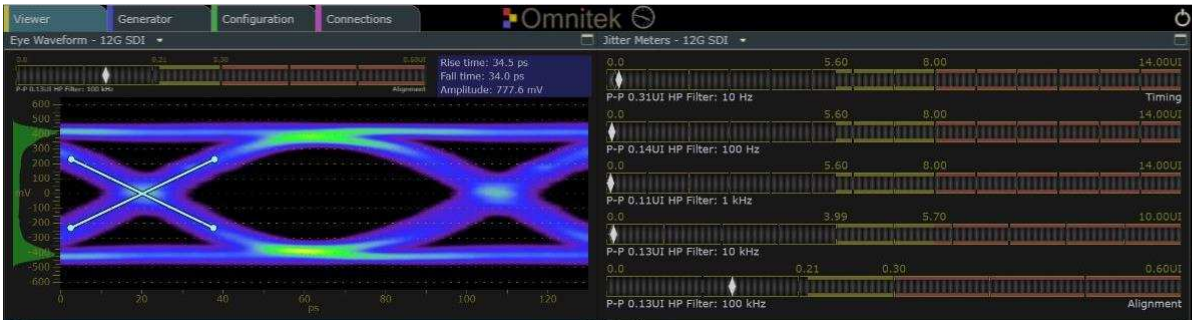

Figure 12. LMH1297 Cable Driver Performance at 12G with Color Bar

Table 4. LMH1297EVM Performance vs. SMPTE Requirements

SMPTE PARAMETER	LMH1297EVM	SMPTE REQUIREMENT
Output Alignment Jitter (UI)	0.13	0.3
Output Timing Jitter (UI)	0.14	8.0
Rise/Fall Time (ps)	34	45
VOD Amplitude (mVpp)	777	720 to 880

4.4 Return Loss Network

The integrated return loss network within the LMH1297 eliminates the need to select and tune external inductors and capacitors to meet SMPTE's stringent return loss requirements. Instead, only an external AC coupling cap is needed. The LMH1297's integrated return loss network on SDI_IO and SDI_OUT exhibits at least 5-dB margin when compared with SMPTE specifications.

5 LMH1297 System Diagnostic Tools

SDI video is typically used in professional and prosumer broadcast and video recording applications, where the reliability of real-time, high-quality video is critical. A reliable SDI end product must strongly adhere to SMPTE specifications while also possessing the ability to diagnose system issues efficiently. The LMH1297 enables both SMPTE-compliant performance and diagnostic capability with an internal eye opening monitor (EOM), system threshold interrupts, line-side loop-through, and host-side loopback.

5.1 Eye Opening Monitor (EOM)

The LMH1297 EOM allows the FPGA to capture the eye diagram after cable EQ input (EQ Mode) or PCB CTLE input (CD Mode), just before the reclocker. In addition, the horizontal eye opening (HEO) and vertical eye opening (VEO) status can be monitored by register control. This internal EOM feature provides a non-intrusive way to observe the signal quality after the EQ. The EOM measurements are independent of the video pattern and may be performed while live video streams through the device.

5.2 System Threshold Interrupt

The LMH1297 can be configured to flag system interrupts. These system interrupts provide feedback to the FPGA upon the occurrence of the following events:

- CDR Lock achieved
- IN0 Signal Detect asserted (CD Mode only)
- SDI_IO Signal Detect asserted (EQ Mode only)
- HEO or VEO threshold reached
- CDR Lock lost
- Loss of Signal (LOS) on IN0 (CD Mode only)
- Loss of Signal (LOS) on SDI_IO (EQ Mode only)

Enabling the desired interrupts in the LMH1297 alleviates the FPGA from needing to poll the LMH1297 eye diagram constantly.

5.3 Loop-Through and Loopback

System diagnostics often require a loopback mechanism for the FPGA to run tests between itself and SDI cable EQ or cable driver. These tests ensure connection robustness and often include industry-standard test patterns such as color bar, PRBS, or pathological test patterns.

As a result, line-side loop-through and host-side loopback are important for troubleshooting, especially after equipment installation is complete. These diagnostic features are integrated into the LMH1297 and help to isolate faults easily on end-to-end SDI video transport networks.

5.3.1 Line Side Loop-Through (EQ Mode)

On the line-side, various factors at 12G-SDI video rates such as repeated connector insertion or aging may degrade performance before the signal arrives at the LMH1297 SDI_IO+ input. The LMH1297 SDI_OUT_SEL pin can be configured to enable SDI_OUT as a reclocked loop-through output. This feature is useful in broadcast monitor or processor applications to provide easy access to the input video signal quality.

Figure 13 shows a typical system example where loop-through is enabled for line-side system diagnostics.

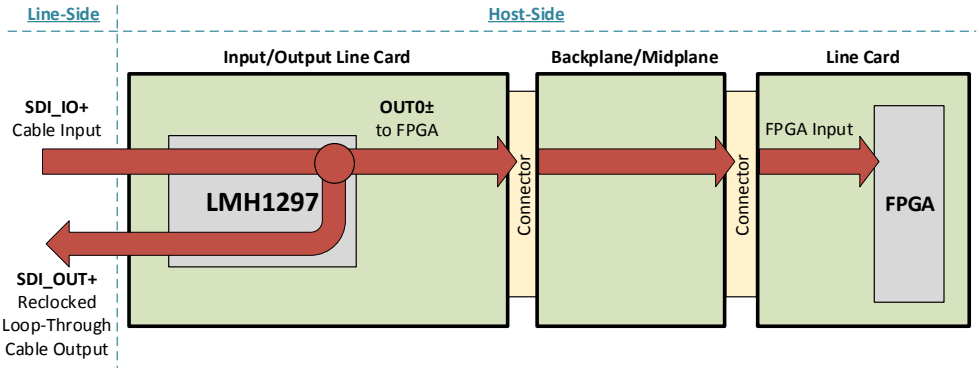

Figure 13. Line-Side Loop-Through, LMH1297 in EQ Mode

5.3.2 Host-Side Loopback (CD Mode)

On the host-side, the 12G-SDI signal from the FPGA may traverse through a combination of PCB trace and connectors before arriving at the LMH1297 IN0± 100-Ω input. The LMH1297 OUT0_SEL pin can be configured to enable OUT0 as a reclocked loopback output. This output provides a video payload back to the FPGA that is equivalent to the line-side data. This feature can be used in combination with a system threshold interrupt to manage the link integrity in real-time between FPGA and LMH1297.

Figure 14 shows a typical system where loopback is enabled for host-side system diagnostics.

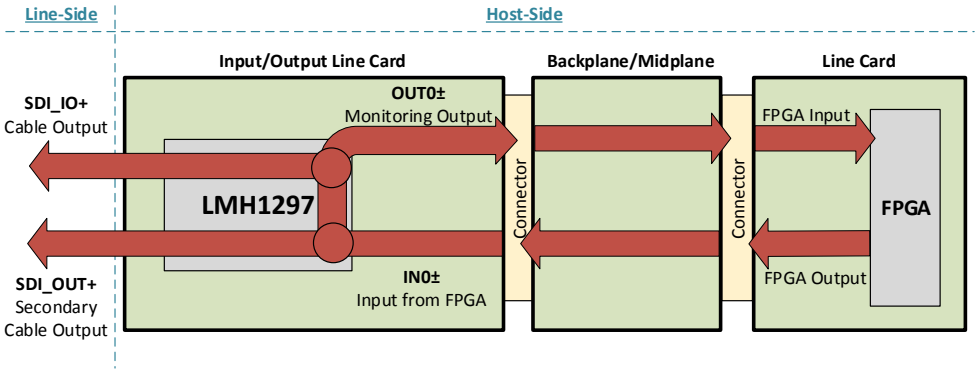

Figure 14. Host-Side Loopback, LMH1297 in CD Mode

6 Bidirectional I/O Applications

6.1 SDI Transport Converter (Gearbox)

The LMH1297 can be configured as a cable EQ or cable driver after board layout. This allows one generic board to serve multiple purposes depending on application requirement. A block diagram of a 12G-SDI-to-quad 3G-SDI converter and quad 3G-SDI-to-12G-SDI converter is shown in Figure 15. By reconfiguring the LMH1297s in software from input to output (or vice versa), both converters may be implemented with a single board design.

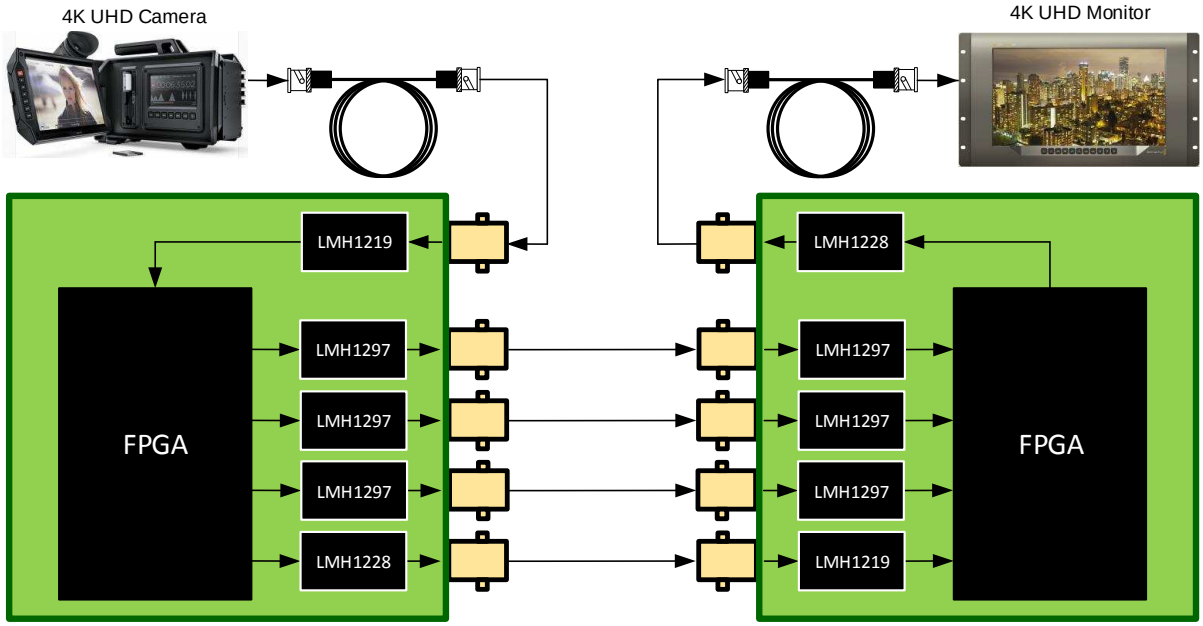

Figure 15. 12G-SDI-to-Quad 3G-SDI and Quad 3G-SDI-to-12G-SDI Converter (Gearbox) Block Diagram

The NEWT reference design, shown in Figure 16 and co-developed by TI and COVELOZ Technologies, demonstrates how one board design may be reused for both 12G-SDI-to-quad 3G-SDI and quad 3G-SDI-to-12G-SDI conversion.

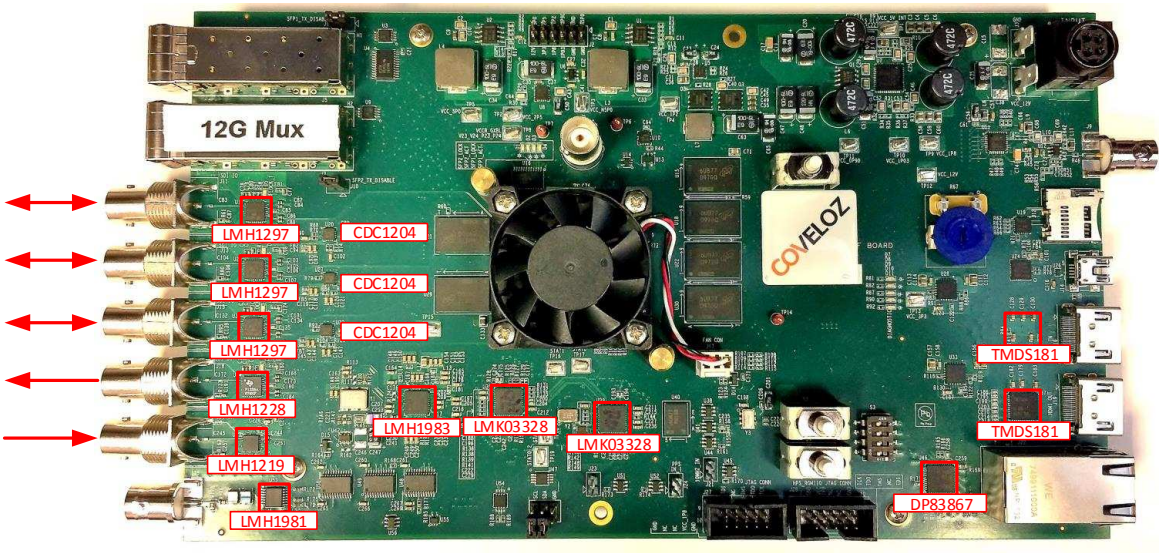

Figure 16. NEWT SMPTE ST-2110 OEM Module for Professional Video Connectivity and Processing

Table 5. BNC I/O Configuration based on SDI Transport Converter (Gearbox) Application

FUNCTIONALITY	INPUTS	OUTPUTS
Quad 3G-SDI-to-12G-SDI	3 x LMH1297 (EQ Mode) 1 x LMH1219	1 x LMH1228
12G-SDI-to-Quad 3G-SDI	1 x LMH1219	3 x LMH1297 (CD Mode) 1 x LMH1228

The NEWT reference design is versatile and may be re-purposed for other applications using the on-board Intel Arria 10 FPGA. In addition to the SDI transport converter (gearbox) application mentioned in this subsection, the NEWT reference design provides a hardware and software design platform to jumpstart other SDI designs, including the following:

- Distribution Amplifier (DA)
- IP Gateway
- SDI-to-HDMI Converter

6.2 Video Wall Controller and Processor

In various monitor and display applications, both SDI input and SDI loop output are needed. By configuring for EQ Mode, the LMH1297 offers a single-chip solution to enable both Cable EQ and loop-through functionality when the SDI_OUT loop-through cable driver is enabled. Figure 17 shows a typical subsection of a video wall controller block diagram that incorporates the LMH1297 and other TI interface devices.

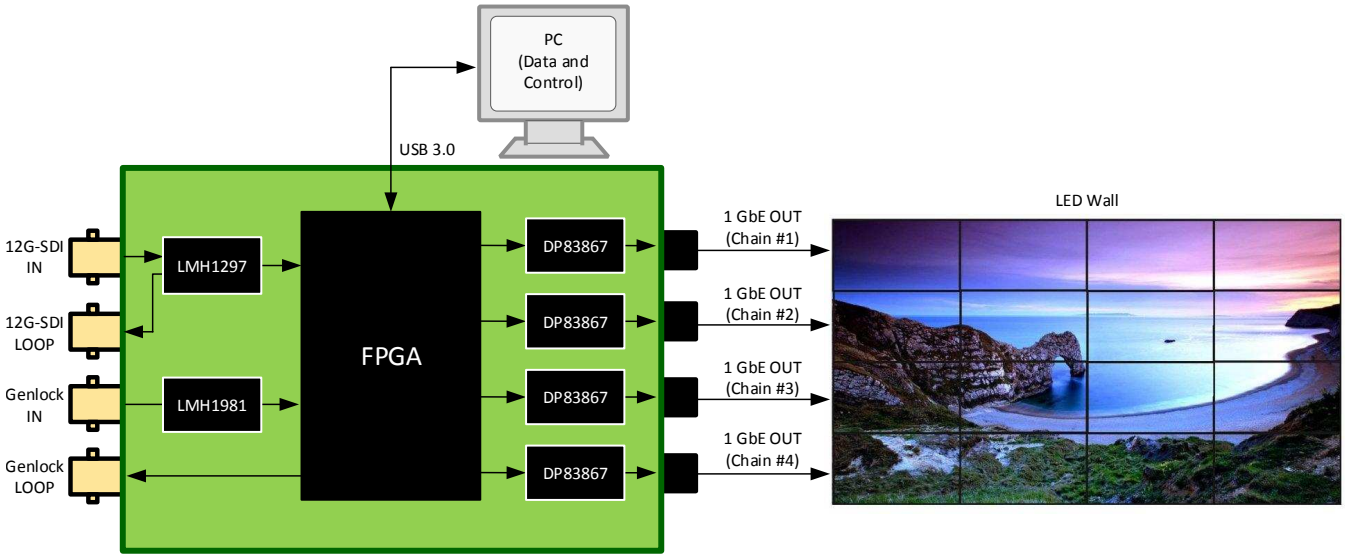

Figure 17. Video Wall Controller Application Block Diagram

6.3 Distribution Amplifier (DA)

For video distribution applications, the LMH1297's OUT0 loopback in CD Mode can be used to simplify designs. This functionality is particularly convenient for 1:N distribution amplifiers (DAs). A typical application block diagram for an SDI DA is shown in Figure 18, with this DA supporting a 1:6 fan-out.

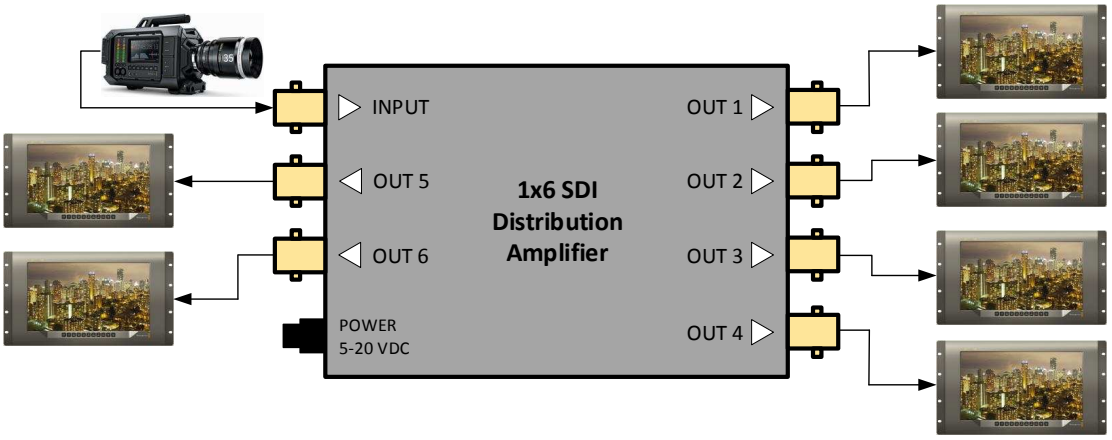

Figure 18. Application Block Diagram of 1x6 SDI DA

Rather than adding a large crosspoint to enable SDI video distribution, the LMH1297 OUT0 acts as a daisy-chain output that feeds into the next cable driver in the chain. In Figure 19, a 1x6 SDI DA can be realized with a single cable EQ and three LMH1297 bidirectional I/Os operating in CD Mode.

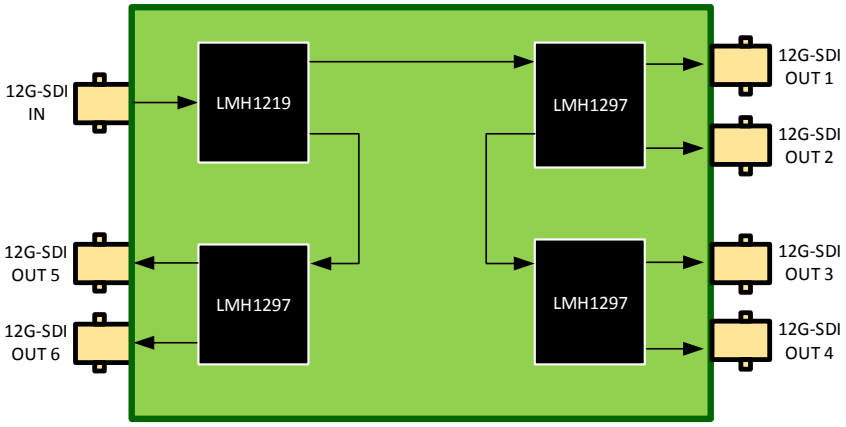

Figure 19. 1x6 SDI DA Implementation Block Diagram

NOTE: Designers may create a 1x12 DA using the design topology in Figure 19 by routing both positive and negative polarities from each LMH1297 cable driver output to BNC connectors.

7 Summary

In summary, the LMH1297 12G-SDI bidirectional I/O enables flexibility, scalability, and cost savings. With built-in diagnostics and convenient line-side loop-through and host-side loopback, the LMH1297 simplifies new 4K SDI designs while maximizing opportunities for design reuse in a variety of applications. Rather than re-invent the wheel for each project, maximize efficiency and simplify future SDI designs with a bidirectional I/O.

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