Application Report
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Enabling GPIOs in the DS90UB925 and DS90UB926

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ABSTRACT

The 24-bit RGB interface is widely used in automotive infotainment. In addition to the 24-bit RGB interface, separate slower speed control signals are also needed. The DS90UB925 and DS90UB926 have additional pins for such applications with the additional control signals. Examples of control signals needed to be sent from the H/U (head unit) to display are display enable, display reset, and backlight brightness control signals. When using the DS90UB925 and DS90UB926 in the 24-bit RGB mode, there are additional unused pins available. The I2S pins and/or unused HS/VS/DE pins can be used to transfer the control signals across from the DS90UB925 to DS90UB926. This article will show how to use unused I2S and HS/VS/DE as GPIOs in DS90UB925 and DS90UB926.

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1 Enabling GPIOs in the DS90UB925 and DS90UB926

1.1 Signals from H/U to Display

1.1.1 Typical Block Diagram

Below is a diagram shows an example of typically used signals between H/U and remote display. In this article, we will only discuss how to utilize the GPIOs signals from H/U to display.

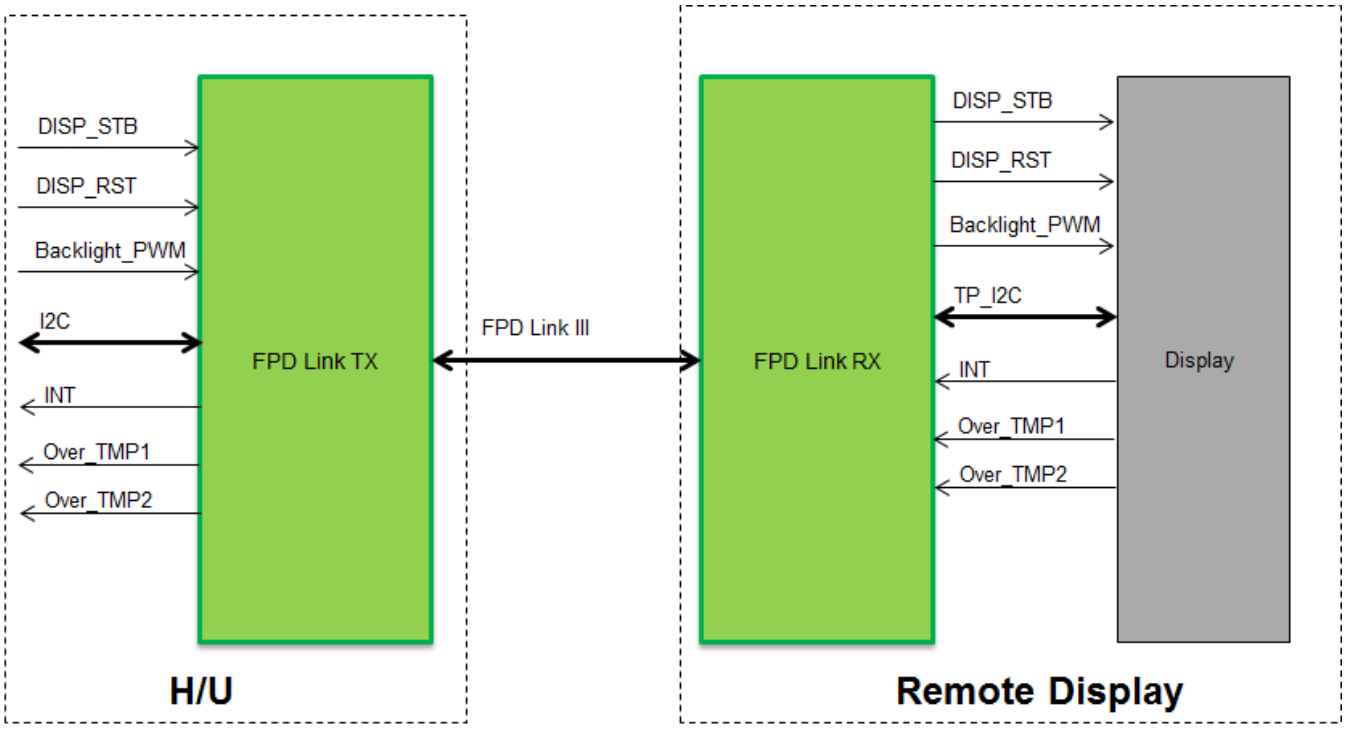

Figure 1. Typical Application for GPIOs between H/U and Remote Display

1.1.2 Control Signal Characteristics

“DISP_STB” and “DISP_RST” are the display enable signal and reset signal. Normally they are logic signals and do not toggle all the time. We can consider them as very low frequency signals.

“Backlight_PWM” is the backlight brightness control signal. The duty cycle is used to control the brightness of the backlight. Normally, the toggling frequency is several hundred Hz to tens of KHz with a duty cycle resolution higher than 1%.

“INT” is the interrupt signal from Touch controller, in DS90UB925/6, there is a dedicated signal/pin for this function.

“Over_TMP1” and “Over_TMP2” are the over temperature from NTC signals in the display. Usually the design will require additional logic or a comparator to convert the NTC signal to Logic signal.

1.2 Option 1: Enabling GPIO8, GPIO7, GPIO6 for Control Signals from the DS90UB925 to DS90UB926 Direction

Register programming is required for programming I2S pins as GPIOs for DS90UB925 input to DS90UB926 output configuration.

I2S_CLK, pin 13, can be configured as GPIO8.

I2S_WC, pin 12, can be configured as GPIO7.

I2S_DA, pin 11,can be configured as GPIO6.

1.2.1 Enabling GPIO8 for the 925 to 926 Direction

1. Set the DS90UB925 GPIO8 (I2S_CLK) as an input, set register 0x11[4] =1 and 0x11[5] =1.
2. Set the DS90UB926 GPIO8 (I2S_CLK) as an output, set register 0x21[4] =1 and 0x21[6] =1.

1.2.2 Enabling GPIO7 for the 925 to 926 Direction

1. Set the DS90UB925 GPIO7 (I2S_WC) as an input, set register 0x11[0] =1 and 0x11[1] =1.
2. Set the DS90UB926 GPIO7 (I2S_WC) as an output, set register 0x21[0] =1 and 0x21[2] =1.

1.2.3 Enabling GPIO6 for the 925 to 926 Direction

1. Set the DS90UB925 GPIO6 (I2S_DA) as an input, set register 0x10[4] =1, 0x10[5] =1, and 0x10[6] =1.
2. Set the DS90UB926 GPIO6 (I2S_DA) as an output, set register 0x20[4] =1 and 0x20[6] =1.

The recommended maximum switching rate when LFMODE=0 (15-85MHz operation) is 100KHz and 50KHz when LFMODE=1 (5-15MHz operation).

1.3 Option 2: Utilizing the I2S Pins as GPIOs for Control Signals from the DS90UB925 to DS90UB926 Direction

When all 24-bit RGBs on the 925/926 are used, there are only 3 pins left that are potentially available that can be used as GPIOs. These pins are the I2S_CLK, I2S_WC, I2S_DA (they are pins 13, 12, and 11 in the DS90UB925). We also know that not all the synchronization signals HS, VS, DE (they are pins 3, 4, and 5 in the DS90UB925) are needed at the same time for LCD display. These unused signals/pins can also be used as GPIOs.

We will discuss the possibility to use these pins as GPIOs in the application without a register configuration. i.e. the default register values are not overwritten.

1.3.1 Using I2S_CLK as a GPIO

The 925 the I2S_CLK should be lower than PCLK/4 to provide 4x over-sampling. For low frequency signals lower than 1MHz on the I2S_CLK pin, the I2S jitter cleaning function will also need to be disabled by setting register 0x2B[7]=1 in the DS90UB926.

In actual audio applications, the I2S_CLK frequency should be lower than 16MHz even if the PCLK frequency is higher than 64MHz.

For proper use of the I2S_CLK configured as a GPIO, the requirement is:

1. I2S_CLK < PCLK/4
2. I2S_CLK < 16MHz
3. Disable I2S jitter cleaning function by setting in the DS90UB926, 0x2B[7]=1

If using the I2S_CLK pin as the Backlight_PWM, you will need to calculate if this meets the duty cycle accuracy requirement.

Figure 2 shows the I2S_CLK waveform working as a GPIO.

NOTE: The I2S_CLK frequency is lower than PCLK/4.

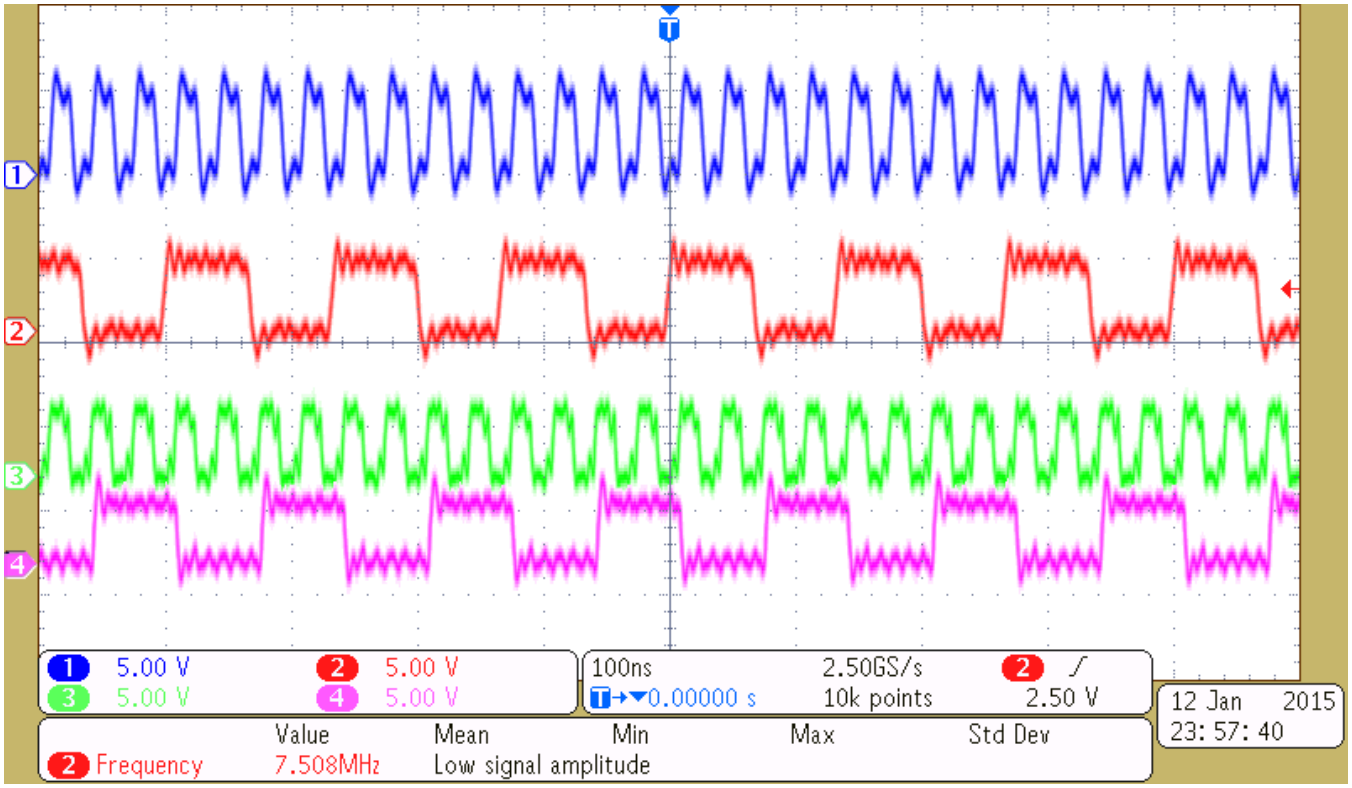

Figure 2. I2S_CLK Used as a GPIO

CH1: UB925 PCLK = 30MHz

CH2: UB925 I2S_CLK = 7.5MHz

CH3: UB926 PCLK output

CH4: UB926 I2S_CLK output

UB926 I2S_CLK jitter cleaning disabled by setting register 0x2B[7] = 1

1.4 Option 3: Using the DS90UB926 I2S_WC and I2S_DA as GPO_REG7 and GPO_REG6

1.4.1 Using the DS90UB926 I2S_WC and I2S_DA as GPO_REGx for Static HIGH or Static LOW Output from GPO_REGx with I2C Control

From the DS90UB926 pinout description, we find that I2S_WC is shared with GPO_REG7 and I2S_DA is shared with GPO_REG6. To enable these 2 GPOs, set registers 0x21 bit 0 and 0x20 bit 5 in the DS90UB926 by writing 1b. The GPO output state will depend on register 0x21[3] bit 3 and 0x20[8] bit 8 in the DS90UB926. When the bit is 1b, the GPO output will be driven to a static HIGH level and when the bit is 0b, the GPO output will be static LOW.

These two DS90UB926 registers can be controlled from the DS90UB925 by remote I2C writes.

1.4.2 Using the I2S_WC and I2S_DA as a GPIO from the GPIO Pin Control

I2S_CLK must be toggling or the I2S_WC and I2S_DA output is gated, meaning they will not toggle either, and no signal will be sent from DS90UB925 to DS90UB926 side. To enable toggling on the I2S_WC and I2S_DA, a clock must be applied to the I2S_CLK and PCLK. The recommended I2S_CLK is 1MHz - 10MHz.

The I2S_WC and I2S_DA toggling frequency must be lower than I2S_CLK/2. Basically, the I2S_WC and I2S_DA HIGH and LOW time must be larger than double of I2S_CLK period.

Figure 3 and Figure 4 are waveforms that show the I2S_WC and I2S_DA working as a GPIO. We can see when I2S_WC, I2S_DA frequency lower than PCLK/2.

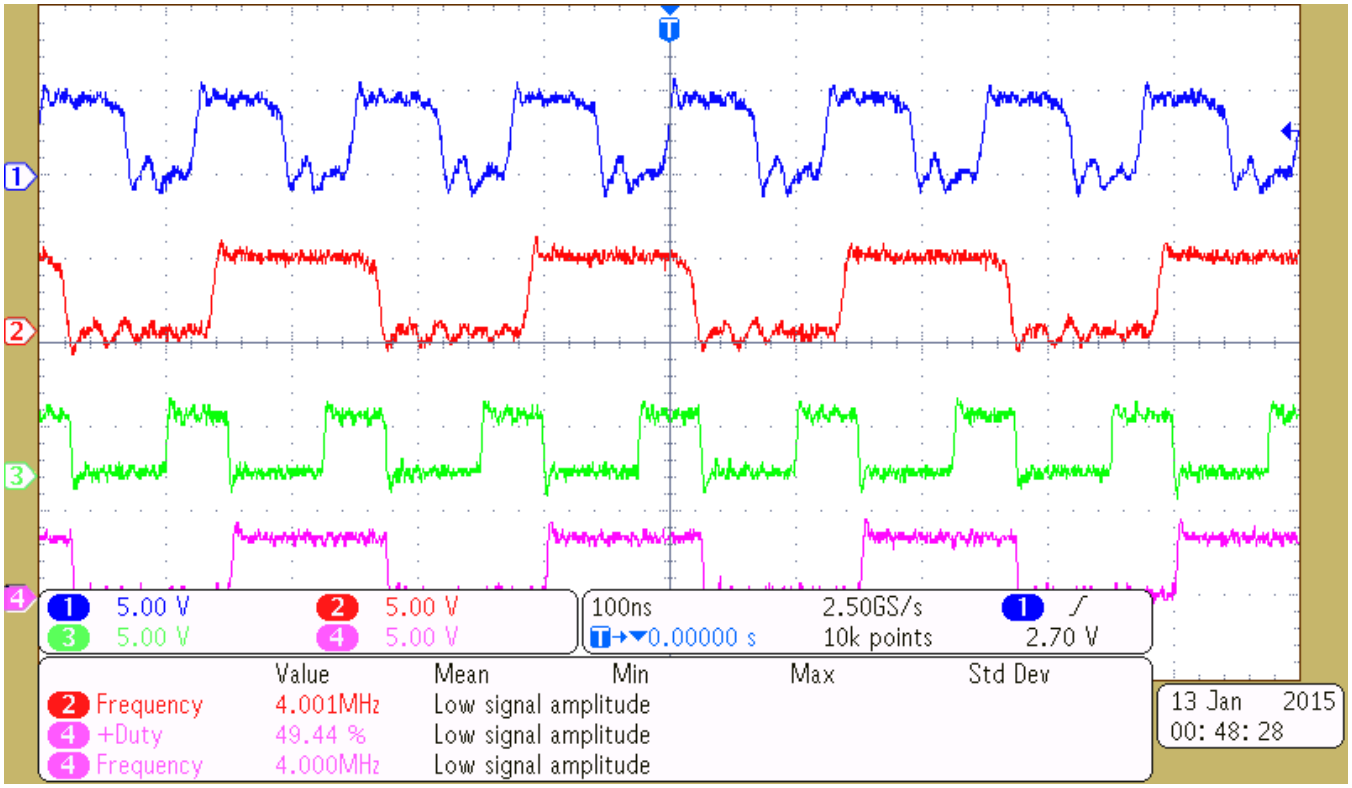

Figure 3. I2S_WC Used as a GPIO

CH1: UB925 I2S_CLK = 8MHz

CH2: UB925 I2S_WC = 4MHz

CH3: UB926 I2S_CLK output

CH4: UB926 I2S_WC output

UB925 PCLK = 40MHz

UB926 I2S_CLK jitter cleaning disabled by setting register 0x2B[7] = 1

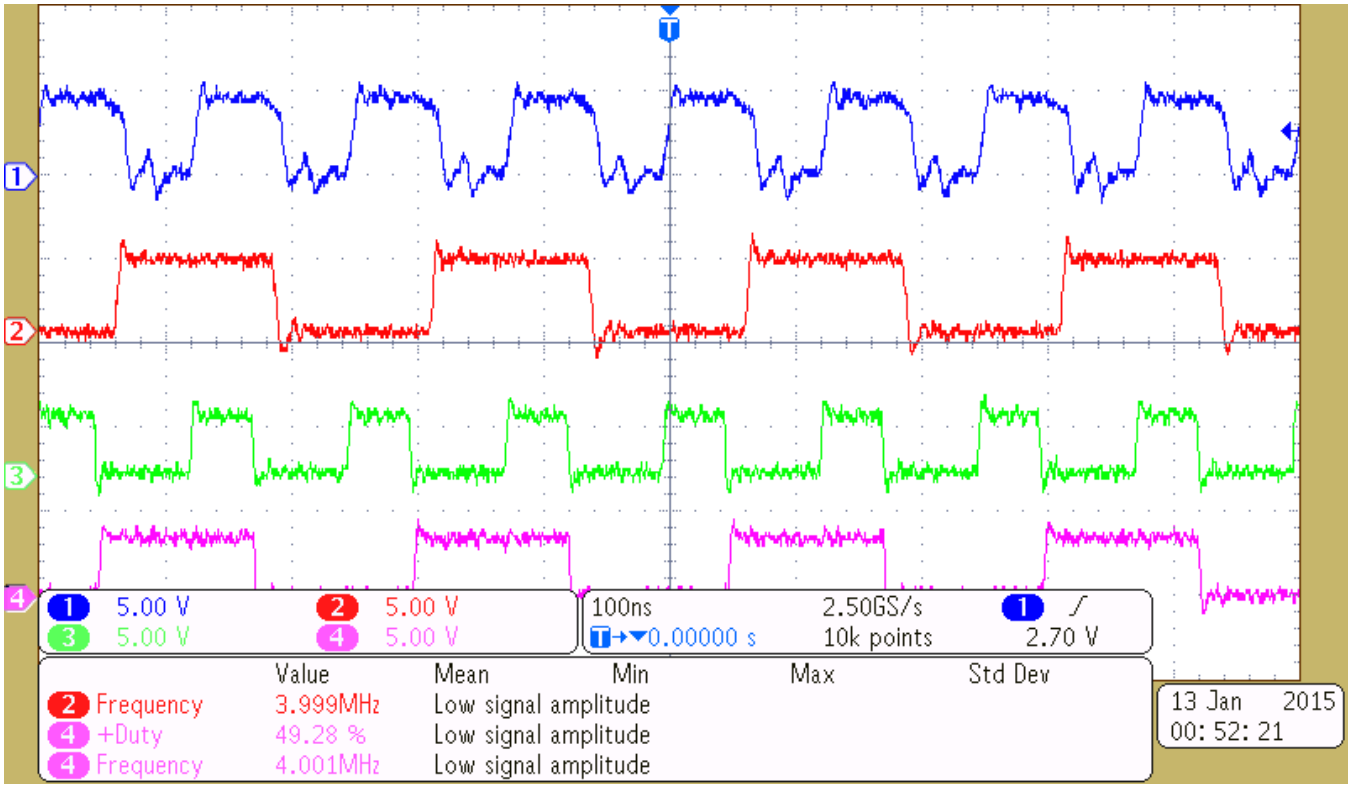

Figure 4. I2S_DA Used as a GPIO

CH1: UB925 I2S_CLK = 8MHz

CH2: UB925 I2S_DA = 4MHz

CH3: UB926 I2S_CLK output

CH4: UB926 I2S_DA output

UB925 PCLK = 40MHz input

UB926 I2S_CLK jitter cleaning disabled by setting register 0x2B[7] = 1

1.5 Using Unused HS, VS or DE

The HS/VS and DE frequency should be much lower than PCLK, especially for the VS signal.

The frequency of VS should be below PCLK/800. The example below still shows PCLK/400 output is clean but PCLK/800 is suggested.

Figure 5, Figure 6 and Figure 7 are the waveforms that show the HS, VS, and DE work as GPIOs. These signals can work correctly as a GPIO function.

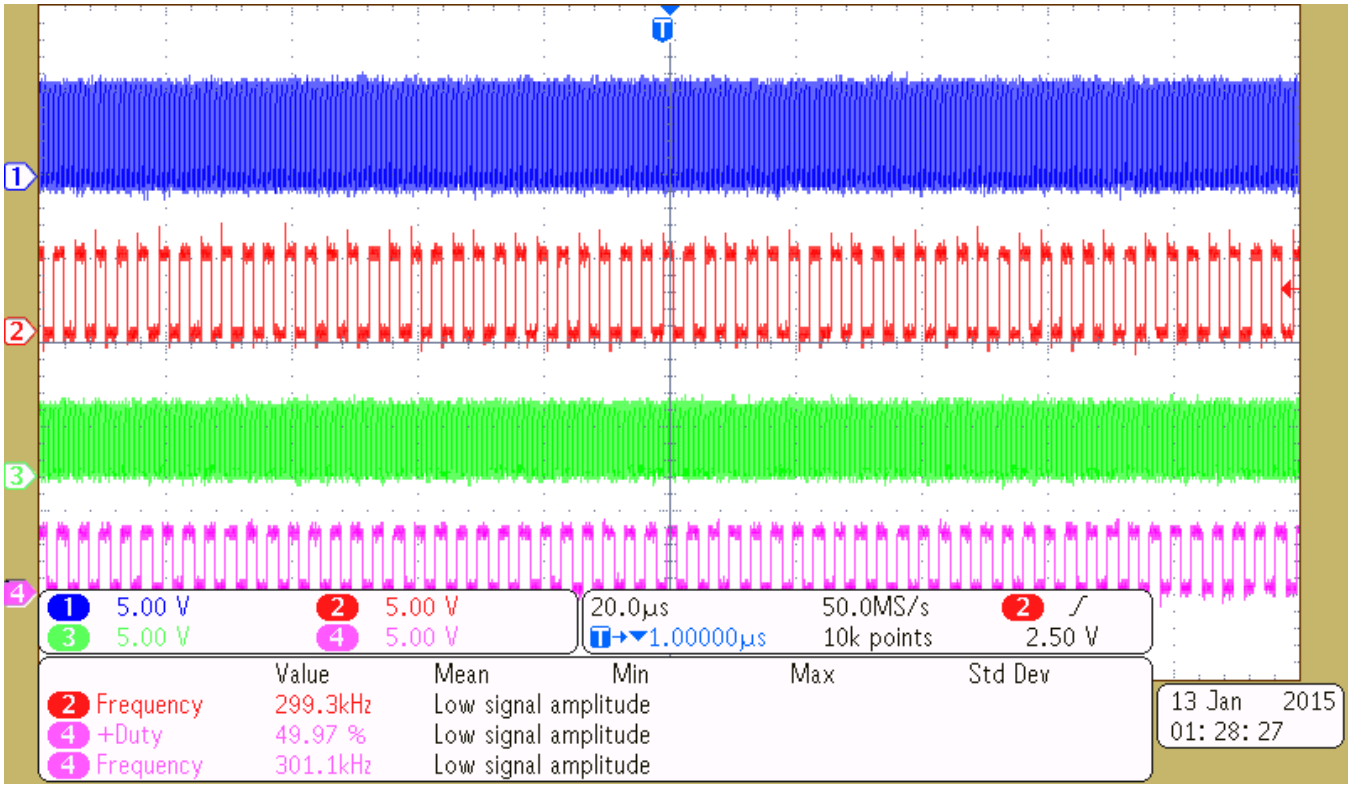

Figure 5. HS Used as a GPIO

CH1: UB925 PCLK = 40MHz

CH2: UB925 HS = 300KHz

CH3: UB926 PCLK output

CH4: UB926 HS output

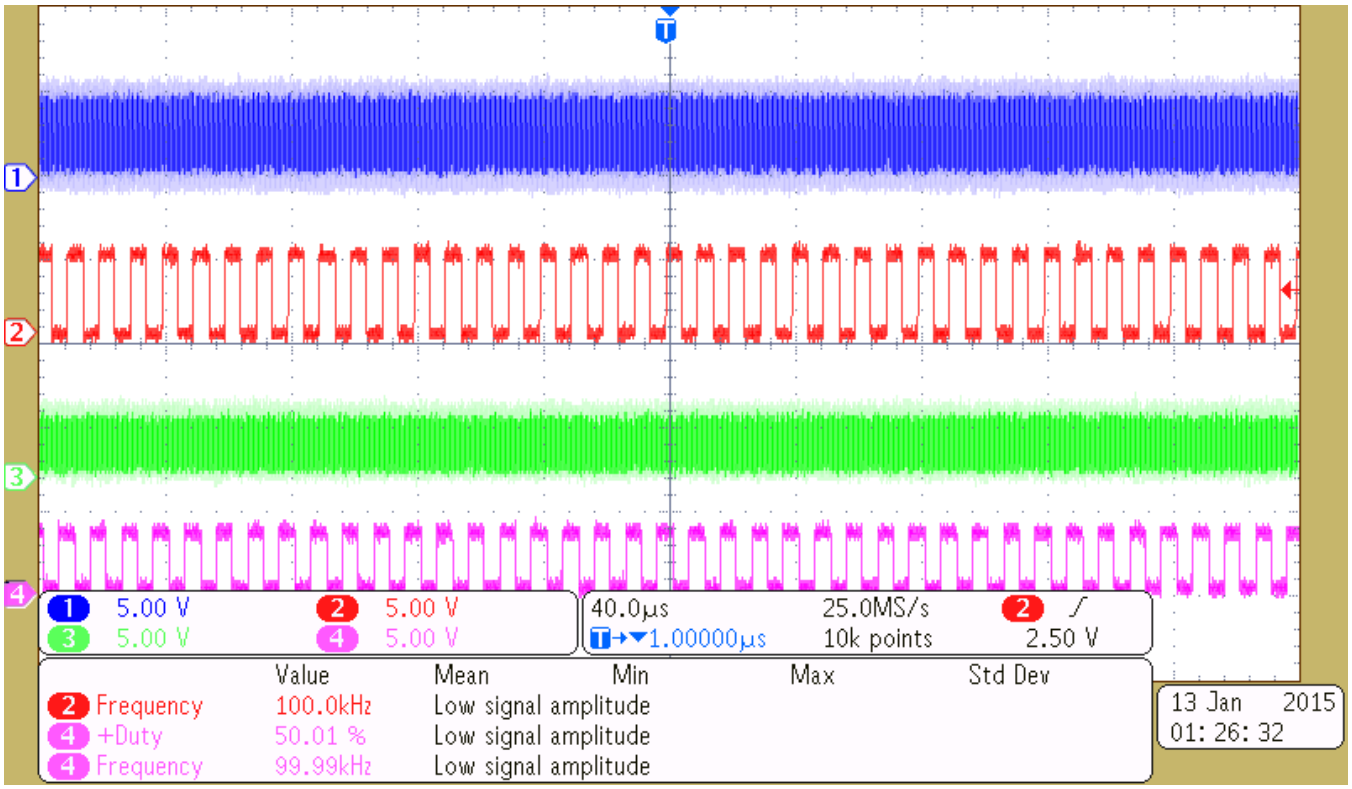

Figure 6. VS Used as a GPIO

CH1: UB925 PCLK = 40MHz

CH2: UB925 VS = 100KHz

CH3: UB926 PCLK output

CH4: UB926 VS output

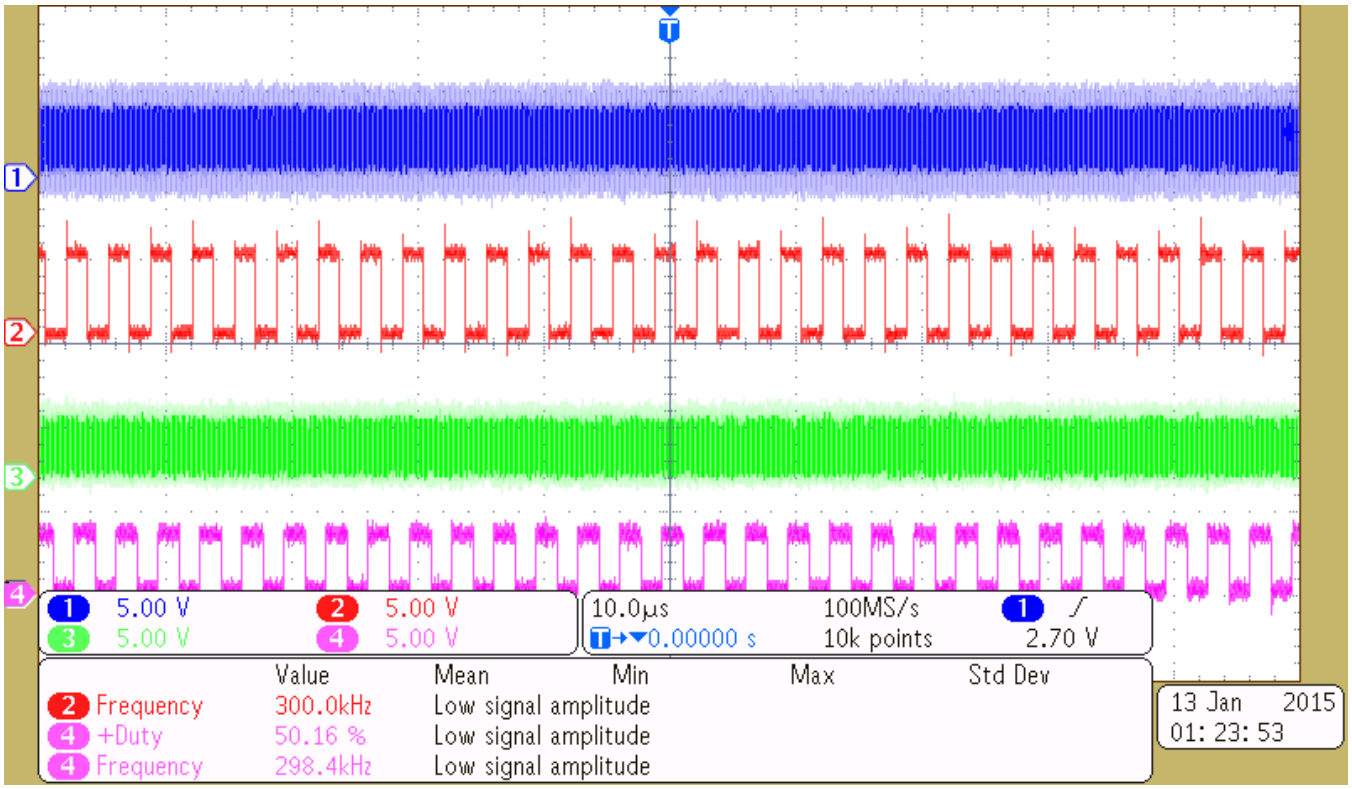

Figure 7. DE Used as a GPIO

CH1: UB925 PCLK = 40MHz

CH2: UB925 DE = 300KHz

CH3: UB926 PCLK output

CH4: UB926 DE output

1.6 Conclusion

When the DS90UB925 and DS90UB926 are sending 24-bit RGB, there are up to 6 GPIOs available for low frequency control signals to be sent from the DS90UB925 to DS90UB926.

1.7 References

1. DS90UB925 datasheet (SNLS407D)
2. DS90UB926 datasheet (SNLS422A)
3. DS90UB925 EVB guide (SNLU113)
4. DS90UB926 EVB guide (SNLU114)

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