DS92LV2421,DS92LV2422,DS92LX1621, DS92LX1622

Go the Distance: Industrial SerDes with Embedded Clock and Control

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No. 122

Go the Distance: Industrial SerDes with Embedded Clock and Control

— Don Rhodes, Field Applications Engineer

Industrial serializers and deserializers, also known as SerDes devices, offer a means of reducing the bus width of a high-bandwidth data interface. The data is converted from a wide parallel data stream to a reduced number of bits or even a single Low-Voltage Differential Signaling (LVDS) lane with a serializer, enabling low-cost and flexible cabling options. The data is then expanded with a deserializer at the destination back into a parallel data stream. The applications for these devices are wide and varied. A few examples and applications will be discussed in this article, as well as the benefits and primary trade-offs of this technology.

Early SerDes products, like the Channel Link I devices shown in ***Figure 1***, serialized a wide parallel data bus (up to 48 bits) into a multi-lane LVDS bus with a separate clock line. This was a significant improvement from the days when the best option for getting data from point A to point B was a wide data bus over a broad ribbon cable. However, there were a number of problems such as inter-pair skew (timing), Electro-magnetic Interference (EMI), and limited cable length, to name but a few. The problem of inter-pair skew either limited the cable length that a system designer was able to use, or it forced the use of low-skew cables which were both expensive and often a challenge to source. Until recently, this was not only the best option, but also it was the only option.

Newer industrial SerDes devices have solved many of the problems that plagued the previous generation of

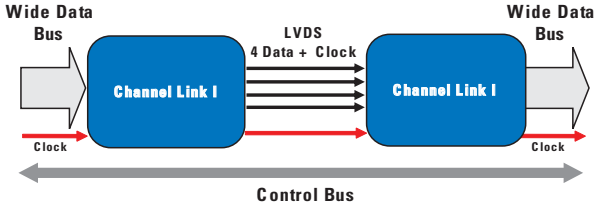

Figure 1. Early Serializers Converted a Wide Bus to Four Data Lanes and a Clock

SerDes. They have done so by serializing both the data and clock into a single differential pair, thereby eliminating cable skew issues and giving designers numerous cable options from which to choose. Instead of being limited to expensive skew-controlled cables, the new generation of SerDes solutions allows the use of low-cost cable options such as Unshielded Twisted Pair (UTP) or coax. Another significant improvement is the reduction of EMI-related problems. Of course there is an inherent improvement in EMI based on the implementation of LVDS signaling as opposed to a wide single-ended bus. However, many of the newer SerDes employ embedded EMI-mitigation techniques which include the use of Spread Spectrum Clock Generation (SSCG) as well as data scrambling and randomization techniques within the data encoding to break up discrete frequencies and harmonics.

To date, cable reach has been limited by the issues previously noted as well as an inability of the SerDes to adequately equalize the incoming data to compensate for the parasitic losses in the transmission medium. Trying to extend the cable reach beyond what was practical would most often result in a closed-eye timing diagram indicating that the data was non-recoverable.

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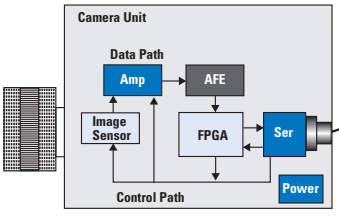

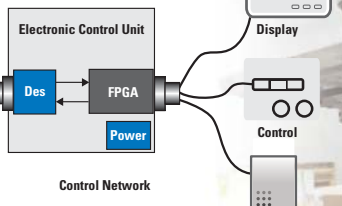

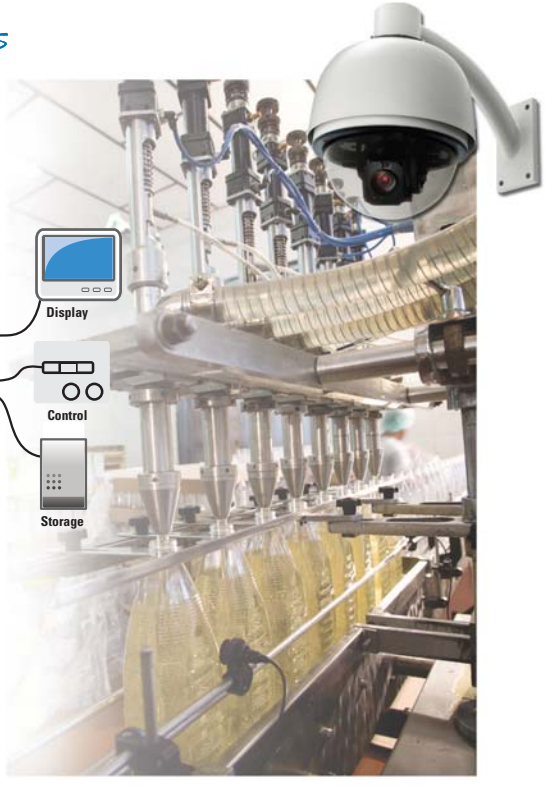

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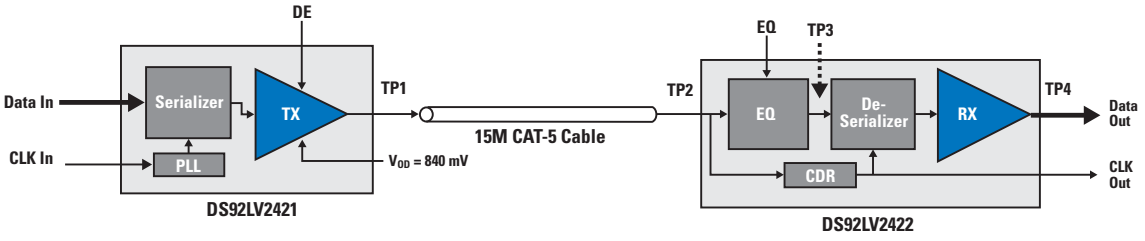
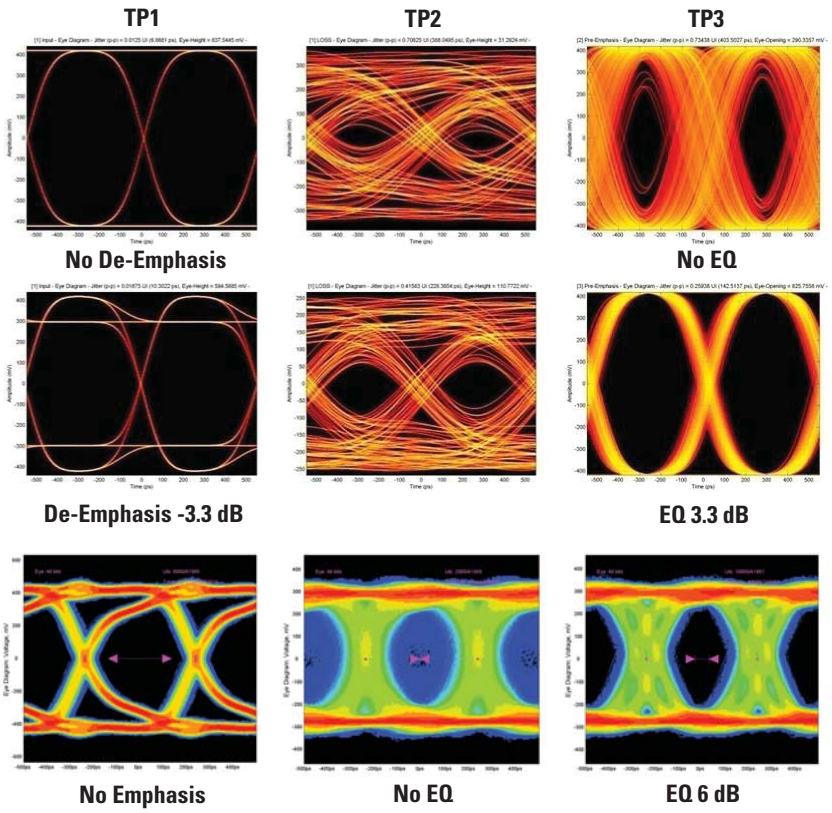


Figure 2. Channel Link II SerDes I/O Block Diagram and Test Case

A realist with a little insight into high-speed-transmission line theory would argue that a cable is simply a low-pass filter. These next-generation SerDes often include de-emphasis and cable equalization to compensate for high-frequency losses and amplify the received signal, thereby enabling much longer cable lengths than previously possible. In doing so, they have the ability to "open" the eye on the timing diagram which reduces, if not eliminates, the bit errors in the data.

National Semiconductor's Channel Link II SerDes, shown in ***Figure 2***, have de-emphasis on the transmit stage of the serializer, DS92LV2421, and cable equalization on the receive stage of the deserializer, DS92LV2422. The photos that follow show simulated signals at three test points along the signal path operating at a data rate of 1.8 Gbps. The top two photos in the first column show the waveform at TP1 with de-emphasis off and set at -3.3 dB, as noted. The de-emphasis compensates on the transmit end for expected high-frequency losses in the transmission medium. In the case of the Channel Link II devices, the de-emphasis and Equalization (EQ) are controlled by internal registers and have eight settings. The use of de-emphasis and EQ can have a dramatic effect as shown in the data at TP3. With a V_{OD} = 840 mV (differential output voltage at TP1), the signal with no de-emphasis or EQ has an amplitude at TP3 of 290 mV and 403 pS of jitter, whereas the signal with DE = -3.3 dB and the EQ = 3.3 dB has an amplitude of 825 mV and 142 pS of jitter.

Oscilloscope screen shots of data from TP1 and TP3, using 10 meters of CAT-6 STP cable operating at a data payload of 1.8 Gbps are also shown. In this case, given this is not a simulation, the measured data point is at the input to the deserializer, not post



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EQ. As can be seen, the equalizer has a dramatic effect on the received data. With the EQ set at 0 dB, the eye is virtually closed, whereas with the EQ set at 6 dB, the eye is sufficiently restored. Essential to the recovery of the data is the Clock and Data Recovery (CDR) circuit which follows the EQ stage within the deserializer. The CDR is designed to recover the data, free of bit errors, from an eye diagram that is closed by 50% or 0.5 UI (typical).

National's Channel Link III devices, the DS92LX1621 bidirectional control serializer and the DS92LX1622 bidirectional control deserializer, are further examples of SerDes that have overcome the issues of the past. For example, ***Figure 3*** shows a serializer that can be directly interfaced to a 16-bit LVCMOS parallel bus of a camera which then serializes the data over a single, AC-coupled, CML lane. As shown, both the clock and the bidirectional I²C compatible control lines for the camera are also encoded in the serialized data. The serialized data, clock, and I²C compatible lines are then deserialized back into a 16-bit parallel bus with discrete clock and I²C on the receive end to interface to a frame grabber or Field-Programmable Gate Array (FPGA). There is no need for an external clock for the deserializer, thereby reducing both the cost and complexity of the design. Furthermore, the deserializer auto syncs to the serializer, enabling true "plug and lock" performance.

Another application that is both easier and more flexible with industrial SerDes is shown in ***Figure 4***, where a display is mounted remotely from a graphics or video processor. In this example the video processor has a 21-bit parallel bus, and the display which could be an I²C compatible controlled, touchscreen panel is located up to 15 meters away.

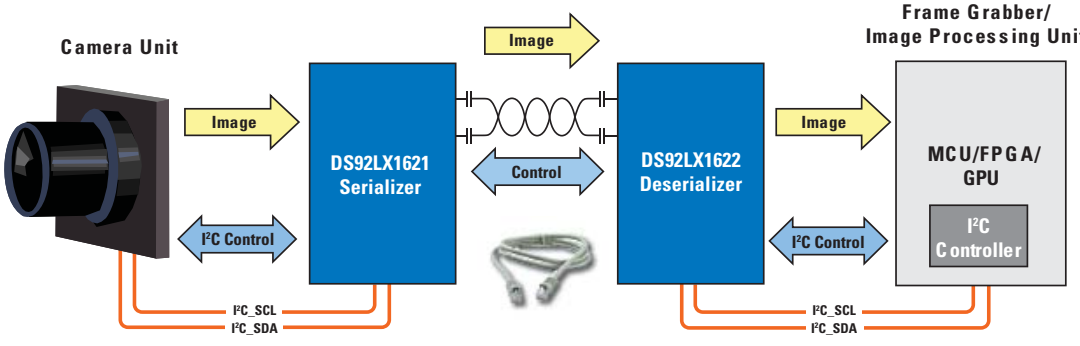

Figure 3. Camera Application, 16-Bit LVCMOS Bus and Embedded I²C Compatible Control

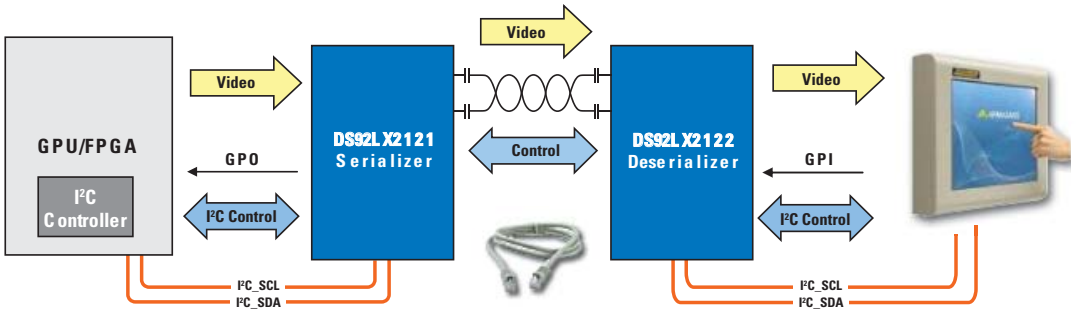

Figure 4. Display Application, 21-Bit LVCMOS Bus and Embedded I²C Compatible Control

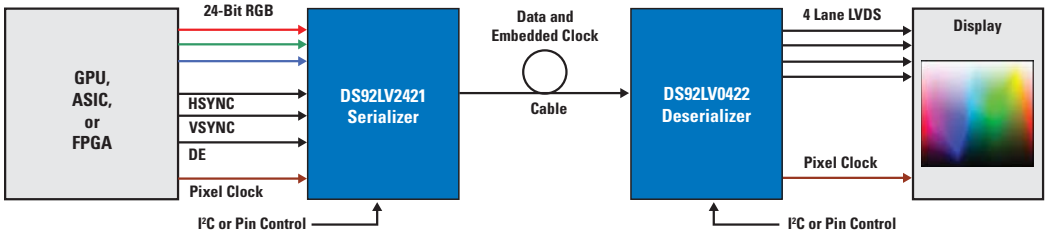

Figure 5. Format Conversion with Channel Link II and III SerDes

Like the previous example, the data, clock, and I²C compatible lines are all serialized into a single differential pair capable of a 1.05 Gbps (21 x 50 MHz) data payload. This has the ability to provide a great deal of design flexibility. Many of these industrial SerDes, including the ones described in this article, can be used for a wide range of applications—when it is necessary to move data over a low-cost medium, over some appreciable distance, and from point to point.

Not only do industrial SerDes have a wide array of product applications, they also have excellent flexibility in how they can be implemented. In the examples noted in ***Figures 3*** and ***4*** the data format was the same before and after the serialization and deserialization process. What might be surprising is that it is possible to use some of these SerDes to convert the data format with the deserializer itself. For example, ***Figure 5*** shows the DS92LV2421 serializer taking in 24-bit RGB data with discrete sync, clock, and control signals and then serializing the data onto a differential pair. The data on the receive end of the cable is then deserialized by a DS92LV0422 into four LVDS lanes and a clock. This has the potential of simplifying and reducing the cost of a design.

The SerDes devices discussed in this article have a wide range of product applications, reaching far beyond the featured video application examples. They have the ability to simplify a product's architecture, reduce cost, and also improve design flexibility. Additionally, many of these SerDes including those highlighted from National have Built-In Self Test (BIST) capabilities which allow the testing of the high-speed serial link. This can be very helpful in system debug as well as production test. They are also designed to mitigate EMI with the use of SSCG. The SSCG feature is under I²C compatible control and allows the selection of the appropriate percentage of clock spread (±0.5%, ±1%, and ±2%) for a given application.

For more information on National's SerDes chipsets, visit: **national.com/serdes**.

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