# LMH0002,LMH0030,LMH0031,LMH0034,LMH0044, LMH0046,LMH1981

***Timing is Everything ?Co The Broadcast Video Signal Path***

Literature Number: SNLA207

SIGNAL PATH designer®

*Tips, tricks, and techniques from the analog signal-path experts*

No. 106



# Timing is Everything – The Broadcast Video Signal Path

*— By Mark Sauerwald, Applications Engineer*

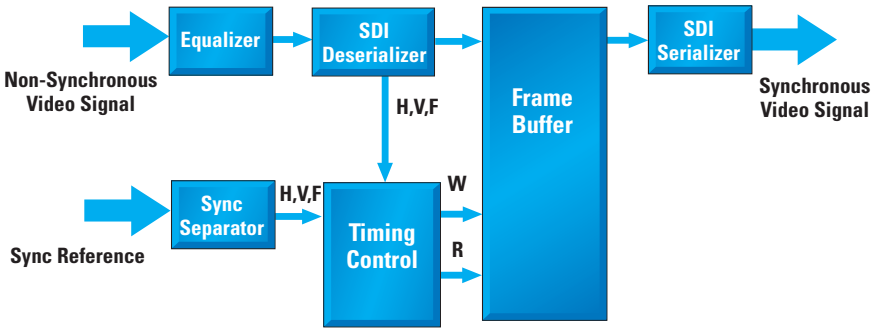


**Figure 1. Major Components of a Genlock System**

A casual observer would note that there are many different broadcast video studios in the world, operating in different formats, some of them analog and some digital. There are multiple high definition television raster formats in use in the United States today. If you tried to count the number of different raster formats covered by the SMPTE292M HD standard, you would run out of fingers and toes. Within any studio there are many different signals, and they are all synchronized in lock step with one another. In video parlance, they are "genlocked."

Genlocking allows for easy switching from one signal to another (i.e., regular programming to commercials) without disrupting the synchronization circuits that are in the viewer's receiver. To do this requires that any signal coming from an outside source be genlocked to the rest of the signals in the studio. Most studios use an analog signal as their timing reference signal, and the timing information needs to be extracted from this signal to allow it to be used to genlock the incoming signal.

When a new signal is brought into a studio, whether it is coming from a satellite receiver, a camcorder, or any other source, the first thing to do is to synchronize it with the rest of the signals in the studio using a genlock circuit.

*Figure 1* shows a block diagram for a genlock which takes an SDI (Serial Digital Interface) input signal, and synchronizes it with an analog reference

**NEXT ISSUE:**
**Delay Calibration**

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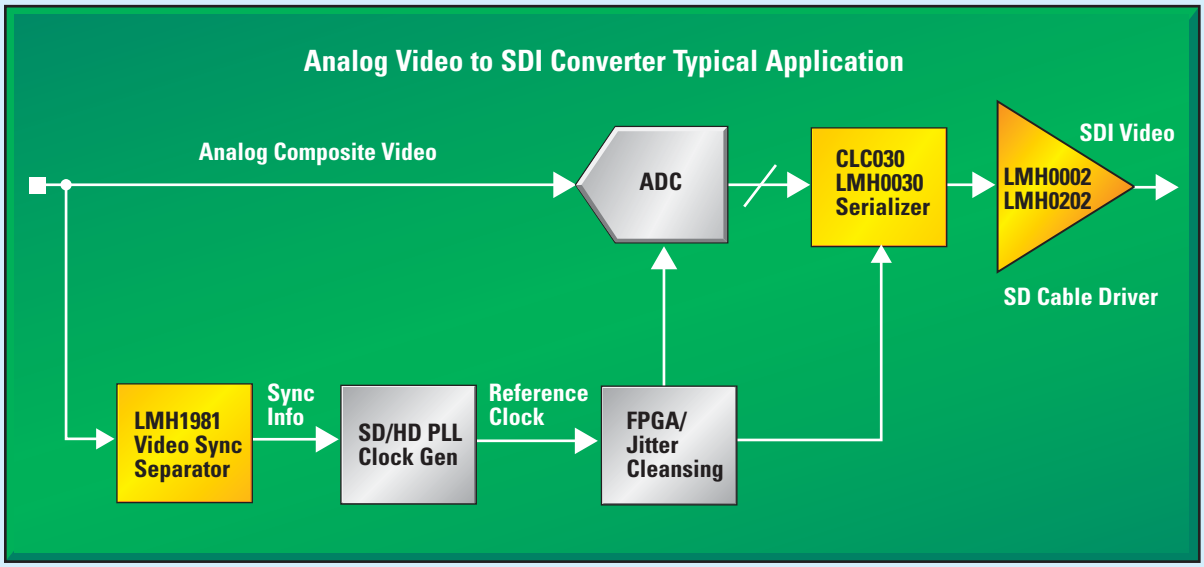
# High Performance Analog Video Solutions




| Product ID | Type | Supported Video Formats | Inputs | Outputs | Spec Supply Range (V) | Packaging |
|---|---|---|---|---|---|---|
| **Sync Separators** | | | | | | |
| **LMH1981** | 50% slicing | NTSC, PAL, SECAM, 480i/p, 576i/p, 720p, 1080i/p | 0.5 to 2.0 Vpp | H-sync, V-sync, odd/even, burst/clamp, video format, composite sync | 3.3 to 5 | TSSOP-14 |
| **LM1881** | 70 mV fixed | NTSC, PAL, SECAM | 0.5 to 2.0 Vpp | V-sync, odd/even, burst/clamp, composite sync | 5 to 12 | SOIC-8, DIP-8 |
| **Video Converters** | | | | | | |
| **LMH1251** | YPbPr to RGBHV converter | 480i/p, 576i/p 720p, 1080i, 1080p XGA, SXGA, UXGA | YPbPr | RGBHV | 5 | TSSOP-24 |

| Product ID | Type | SSBW (MHz) | $A_V$ (V/V) | Slew Rate (V/µs) | $I_{CC}$ (mA/Ch) | Spec Supply Range (V) | Packaging |
|---|---|---|---|---|---|---|---|
| **Analog Crosspoint Switches** | | | | | | | |
| **LMH6582** | 16 x 8 | 500 | 1 | 3000 | 110 mA (total) | ±3.3V to ±5V | TQFP-64 |
| **LMH6583** | 16 x 8 | 500 | 2 | 3000 | 110 mA (total) | ±3.3V to ±5V | TQFP-64 |
| **Analog Multiplexers** | | | | | | | |
| **LMH6570** | 2:1 Mux | 500 | 2 | 2200 | 15 | 6 to 12 | SOIC-8 |
| **LMH6572** | Triple 2:1 Mux | 350 | 2 | 1400 | 23 | 6 to 12 | SSOP-16 |
| **LMH6574** | 4:1 Mux | 500 | 2 | 2200 | 13 | 6 to 12 | SOIC-14 |

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that is being supplied. In this edition of the Signal Path Designer, we will look at this application in detail, and examine the design considerations for each of the six blocks.

## Cable Equalizer

The SDI inputs on video broadcast equipment typically support long cable lengths: over 140m for high definition signals, and over 300m for standard definition signals. In order to support long cables, there needs to be a cable equalizer.

Long cables have a low-pass characteristic, where the attenuation of the input signal is proportional to the length of the cable, and the square root of the frequency. ***Figure 2*** shows the frequency response of a 100m length of a common (Belden 1694A) cable used in video installations.

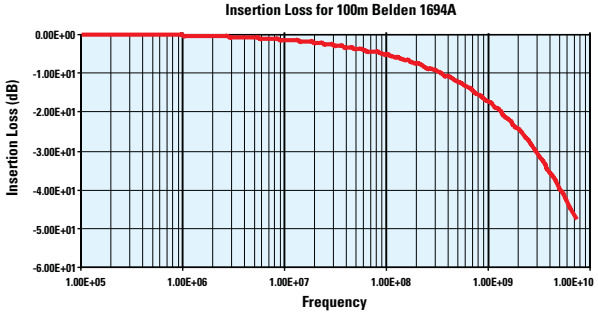



**Figure 2. Belden 1694A Frequency Response**

Although seeing the attenuation with frequency is helpful in designing the complementary filter that you will need to recover the signal, the image that you really want to see is the eye diagram. This tells you if there is there an opening big enough to recover the data. ***Figure 3*** shows the eye diagrams for a 1.5 Gbps signal (an HD-SDI signal) after it has gone through various different lengths of cable. From the standpoint of this article, the primary result of the skin effect is that as the frequency increases, a smaller and smaller portion of the cross section of the cable will be carrying the signal, so there will be greater signal attenuation at higher frequencies than at lower frequencies. The response curve for this loss will be proportional to the $\sqrt{\omega}$ which makes compensation difficult for standard types of filters.

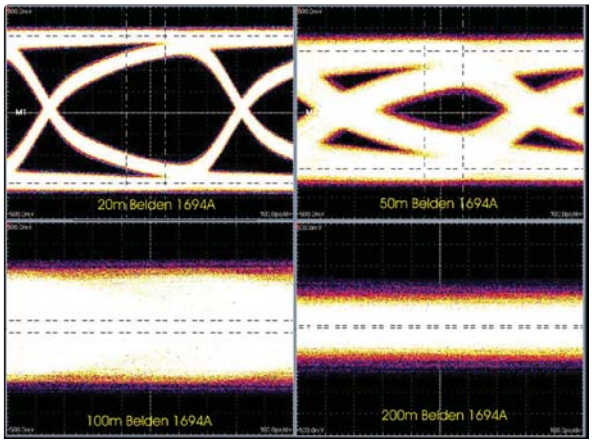



**Figure 3. Oscilloscope Traces of an HD-SDI Signal After Going Through Coax Cable**

To attempt to match the frequency response of the cable, the designer carefully places the zeroes in his or her filter such that the resulting response is a close approximation to the $\sqrt{\omega}$ response of the cable.

To deal with the fact that both high gain and high bandwidth are required at the same time, equalizer circuits are realized in exotic, high-speed processes such as the National's 0.25 µm BiCMOS SiGe process. An example of one of these equalizers is the LMH0044 cable equalizer. With this part, you can recover signals at data rates of up to 1.5 Gbps through 200m of Belden 1694A cable.

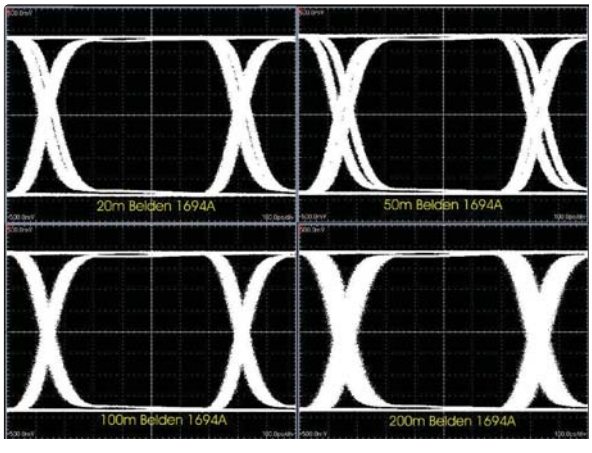
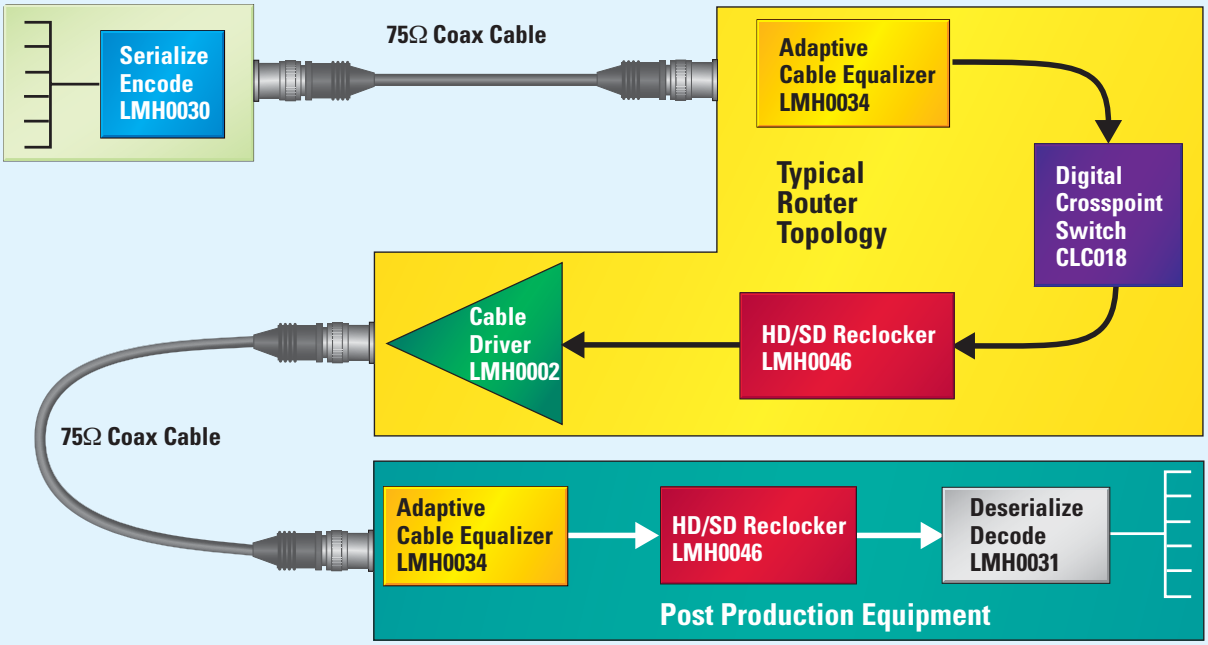
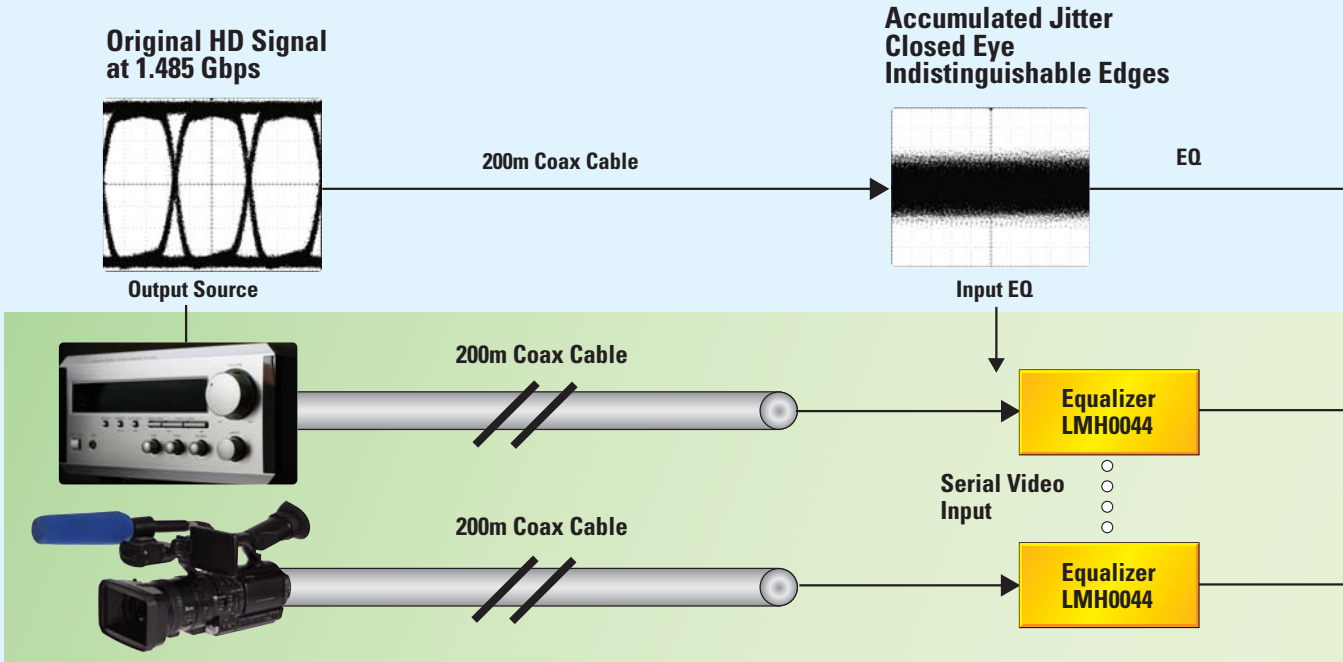



**Figure 4. Equalized Outputs**

# HDI-SDI Signal Path Solutions




## SDI Signal Conditioning

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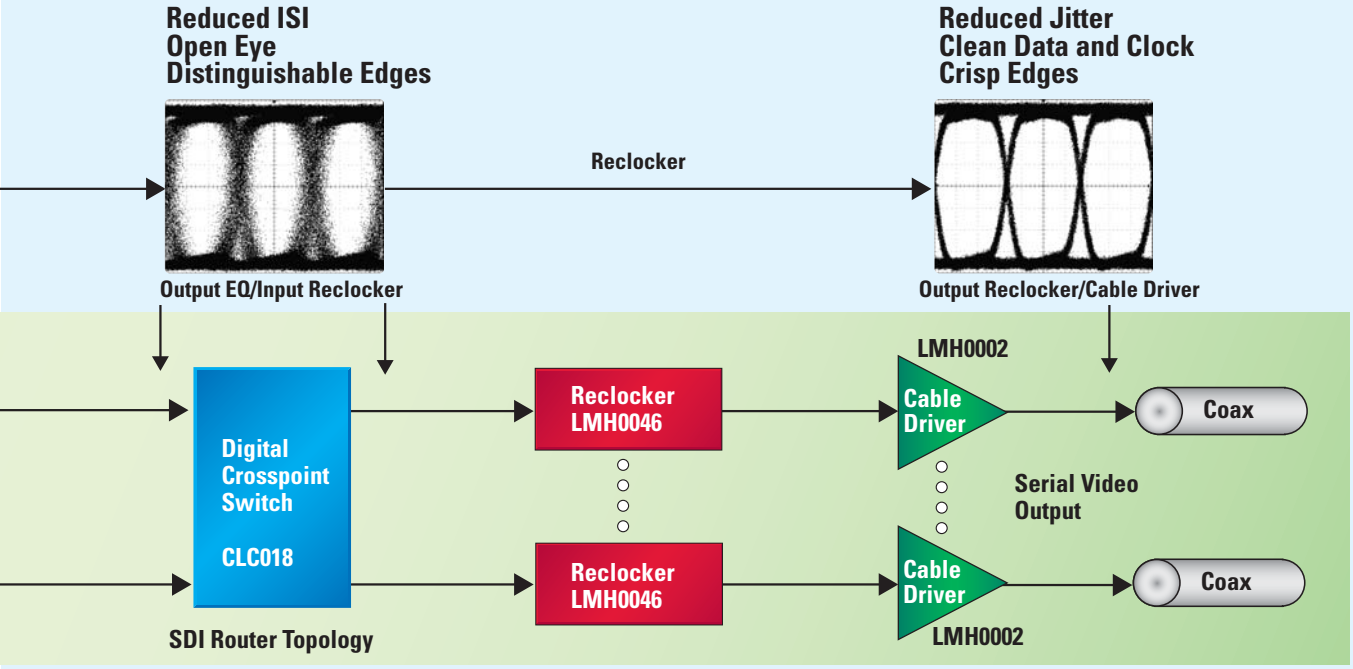
| Product ID | Function | Max Speed (Mbps) | Temp Range (°C) | Eval Board | Comments | Packaging |
|---|---|---|---|---|---|---|
| **Cable Drivers** | | | | | | |
| **LMH0002MA** | HD/SD Serial cable driver | 1485 | -40 to 85 | SD002EVK | Selectable slew rate | SOIC-8 |
| **LMH0202MT** | Dual HD/SD Serial cable driver | 1485 | 0 to 70 | SD0202EVK | Dual differential input, dual differential output | TSSOP-16 |
| **Adaptive Equalizers** | | | | | | |
| **LMH0034MA** | HD/SD Adaptive cable equalizer | 143 to 1485 | 0 to 85 | SD0342EVK | SMPTE 292M/259M Serial recovery | SOIC-16 |
| **LMH0024MA** | 3.3V SD Adaptive cable equalizer | 143 to 540 | -40 to 85 | SD024EVK | Footprint compatible with LMH0034 | SOIC-16 |
| **LMH0044SQ** | HD/SD Adaptive cable equalizer | 1.485 Gbps | 0 to 85 | SD044EVK | Equalize up to 200m of cable at HD (1.485 Gbps) | LLP-16 |
| **Encoder/Decoders** | | | | | | |
| **LMH0030VS** | SMPTE 292M/259M Digital video serializer/encoder | 270 to 1485 | 0 to 70 | SD130EVK | Integrated cable driver, FIFO, BIST, and TPG | TQFP-64 |
| **LMH0031VS** | SMPTE 292M/259M Digital video serializer/ decoder | 270 to 1485 | 0 to 70 | SD131EVK | FIFO, BIST, and TPG | TQFP-64 |
| **Reclockers** | | | | | | |
| **LMH0046MH** | HD/SD Reclocker | 1.485 Gbps | -40 to 85 | SD046EVK | Dual differential outputs, optional data rate clock; 27 MHz reference | TSSOP-20 |



# Broadcast Video Signal Path

## Deserializer

Once you have done the hard work of opening the eye of the signal coming in, you have to make sense of the bits that are coming at you, and this is the job of the deserializer. Video images have a very regular, repetitive format. They are composed of individual bits which are, at the next highest level of organization, divided into 10-bit words which are in turn divided into pixels. A series of pixels comprises a line, a series of lines makes up a field, and one or more fields are needed to complete the video frame. To sort out this organization, the SMPTE data sends a special sequence known as a Timing Reference Signal (TRS) at the start and end of each line. By detecting this TRS, it allows the receiver to figure out both the word and line alignment for the signal. At the end of each line, there are a couple of extra words inserted which tell the receiver what the line number is. A CRC is also included, so that the receiver will know if it has properly received all of the data in the line. There are a couple of things that can wreak havoc with receivers: DC content and long periods of time with no transitions. Most communications systems have a way to control this. In the case of the SMPTE 292 serial standard (HD-SDI) it is done with a combination of scrambling and encoding the data.

A good deserializer will extract all of this information for you, and present you with what you need. For this application, it consists of the picture data and the timing data. A deserializer such as the LMH0031 will do this for us, presenting the picture data on two 10-bit data busses. The timing data is presented in the form of three digital signals representing H (start of a horizontal line), V (start of a vertical interval), and F (start of Frame). If the raster format is not interlaced, then you can use just H and V because they are the same.

The serial data is brought into the deserializer where it is decoded and descrambled. Then it is analyzed to find the TRSs which allows the deserializer to know how to break the bits into words. The TRSs' are further analyzed to extract the timing information which is encoded and the data is scrambled, it decodes and descrambles, then the framing is determined so that the deserialized data can be properly word aligned. All of this activity is generally done in the deserializer.

## Sync Separator & PLL

Although the video world has gone mostly digital, one area where analog is still very common is in the sync-reference signal, which the studio uses to synchronize all of their equipment. The most common reference to use is a video signal which does not include picture information. This will consist of a series of pulses indicating the start of each video line, with a specific pattern that indicates the end of each field or frame. In this block of our genlock circuit, a sync separator circuit extracts H, V, and F (start of a horizontal line, start of a field, and start of a new frame) from the reference signal, and a PLL circuit generates a pixel clock which is synchronous with the reference signal.

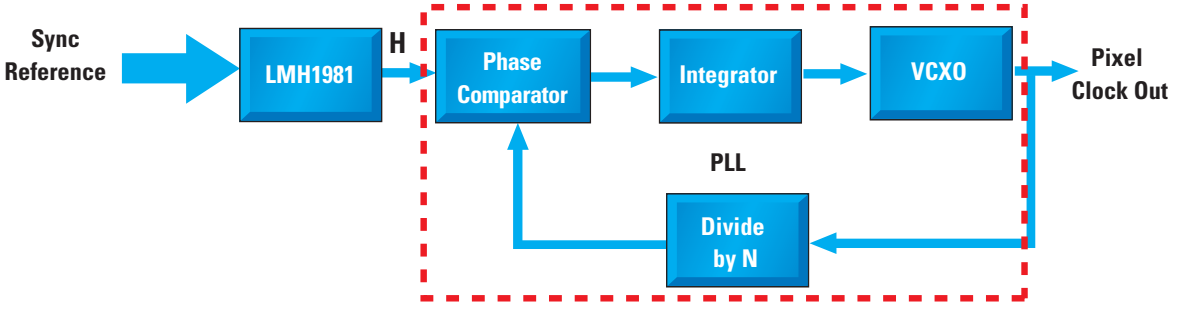



**Figure 5. Block Diagram of the LMH1981 Sync Separator & PLL Generating the Pixel Clock**

For example, the LMH1981 is a high-performance multi-format sync separator that accepts standard analog SD or HD video signals with either bi-level or tri-level sync. It automatically detects the input video format and applies 50% sync slicing to ensure accurate sync extraction even if the input has irregular amplitude, offset, or noise conditions. To generate the pixel clock, a PLL should be set up to lock to the Hsync output of the LMH1981 and generate the desired clock frequency, which is typically 27 MHz for SD or about 74 MHz for HD. Something to consider when using a PLL for clock generation is that the divide ratio can be quite large and reduce loop bandwidth, which could make the PLL quite sensitive to jitter on Hsync. This makes it especially important to select a sync separator with a very low jitter Hsync output.

## Frame Buffer

The frame buffer is simply a block of memory large enough to hold at least one entire frame of the image. This buffer needs to be dual port so that the data coming from the deserializer can be written into one side of the buffer, while data can be read from the other side of the buffer to be fed to the serializer. The buffer is organized in the same way as the video image, with consecutive pixels forming complete lines and consecutive lines forming the complete frame.

## Timing Control

The timing control is the heart of the entire genlock system. The basic function is to control the writing into the frame buffer and the reading from the frame buffer. The timing control needs to keep track of two different timing domains. On the input side it receives the data, the timing information, and a clock from the deserializer. This data is written into the frame buffer, with a series of counters that keep track of the pixel and line information. This data is written synchronously with the clock being recovered from the deserializer. At the same time, the timing control takes the timing information coming from the sync separator and the pixel clock. These are used with a second set of counters to read data out of the frame buffer. This data is being read synchronously with the reference sync signal so that the image which was received by the deserializer is now being read synchronously with the reference. The data, along with the pixel clock are fed to the serializer for output. Although video signals have very tight timing specifications, there will be some difference between the input and the output data rates, which means that eventually the frame buffer will either empty out, or overflow. The timing control circuitry has to recognize this situation and periodically repeat a frame or drop a frame to maintain the timing difference between input and output smaller than the size of the frame buffer.

## Serializer

Once the data is read out of the frame buffer, it is in parallel format. Before it can be sent to the next piece of equipment it needs to be serialized and formatted to meet the SMPTE 292M HD-SDI standard. From a digital standpoint, new TRS characters are generated and inserted, new line numbers and CRCs are calculated and inserted, the data is then scrambled via the SMPTE scrambling algorithm and converted to NRZI format before being shifted out of a parallel to serial shift register. The key to doing all of this properly is to use a clock clean enough to meet the tight video timing specifications to shift the data out. SMPTE 292M allows no more than 0.2UI of jitter peak-to-peak on the serialized output, which means that the clock jitter needs to be below about 100 ps p-p. Most serializers take a clock which is at the parallel data rate as their input clock (for HD this would be approx 74 MHz) and then multiply it up to the serial rate of 1.5 GHz. Most good serializers will use a PLL for this multiplication that will reject some of the jitter in the original parallel clock. However, for the best performance it is best to start with the cleanest clock possible. In the example sync separator/clock generation circuit, you generated a pixel clock with a VCXO that has very low jitter so that added to the jitter rejection characteristics of the serializer will lead to a very low jitter output. Using the LMH0030 serializer with the VCXO clock source, you could expect your serial jitter to be approx 75 ps, well below the 0.2UI limit.

## Summary

Using a handful of simple, off-the-shelf components, you can take a radical input video signal, which is marching to the beat of a different drummer, and get it to straighten up, and march with the rest of our signals. This way, you can switch from one program to another without disrupting the image on your screen. ■

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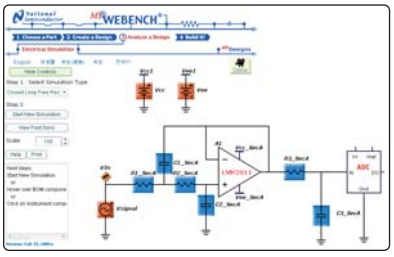

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