LMH0307,LMH0356

Literature Number: SNLA178

National Semiconductor

Design Considerations for SMPTE 3 Gbps SDI Interfaces

Mark Sauerwald
National Semiconductor

When SMPTE 424M came out with the standard for a 3 Gbps Serial Digital Interface, much of what was standardized was similar to the 1.5 Gbps HD-SDI interface, SMPTE 292M, that is so well established and understood. The assumption of many early adopters of this standard was that you could use the same architectures to build 3 Gbps equipment as what had been used for HD SDI, and then build studios with this equipment in order to support the higher definition formats. Unfortunately when SMPTE 424M was approved, it included a relaxed jitter specification, allowing up to 0.3UI of alignment jitter rather than the 0.2UI which is specified in SMPTE 292M. This paper explores the consequences of this relaxed specification on system performance and looks at new architectures for studio equipment which are able to better tolerate the increased jitter, as well as discussing the fact that studio designers may want to look more closely at some performance measures of 3 Gbps equipment rather than just looking for 'SMPTE 424M Compliant'

Tutorial: The Eye Diagram

Throughout this paper we will be looking at 'eye diagrams' and making judgments about the signal integrity of various signals based on these waveforms. An eye diagram is a way of evaluating the integrity of a signal in a system. To capture an eye diagram, the signal is provided to the input of an oscilloscope, and the scope is triggered with a clock signal for the input data signal with the display persistence set to a long period. The result is something like that shown in Figure 1 where the display takes on the shape of an eye. From this display many parameters of the signal can be directly measured – Rise and Fall times, Amplitude, Over/undershoot, unit interval etc. Jitter may be estimated by looking at how fat the vertical lines are. The scope shown in Figure 1 is able to make some of these basic measurements automatically for you. In general, you want the opening of the eye to be as large as possible in order to be able to accurately receive it. Figure 1 shows a fairly good signal – the rise and fall times are a small portion of the unit interval, there is little noise, as seen by the fact that the lines are thin, and there is very little over/undershoot. The signal in Figure 2 has much longer rise and fall times compared to the unit interval, and there is a lot more noise or jitter on the signal which has resulted in a significant amount of closure of the eye. Recovery of an error free signal from the example shown in Figure 1 will be much easier than recovery of an error free signal from the example shown in Figure 2.

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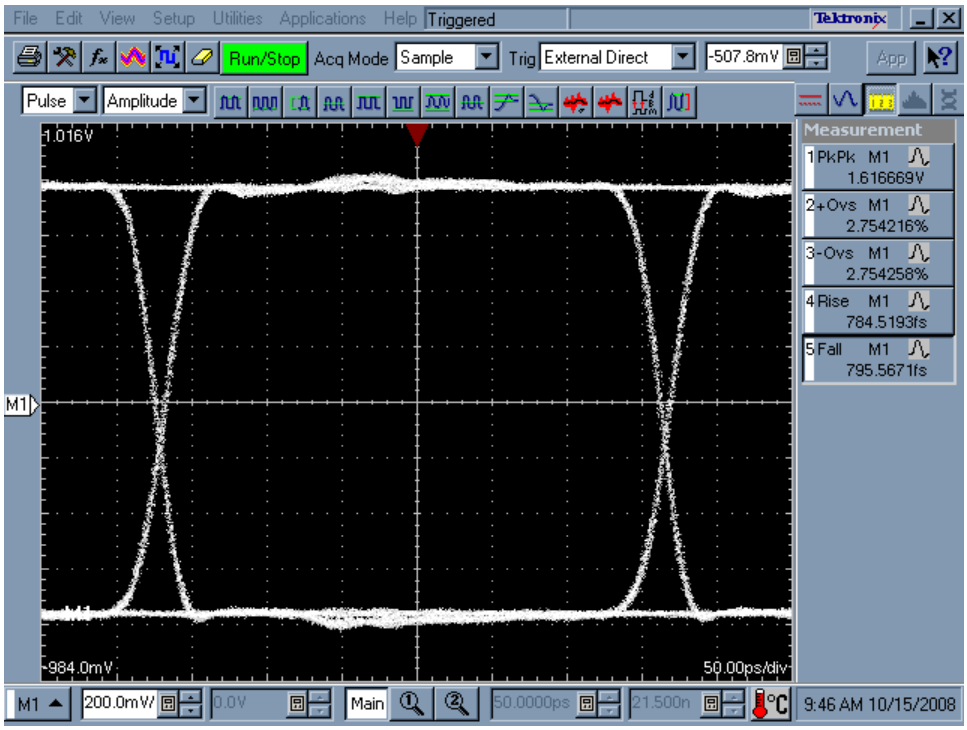

Figure 1. Eye Diagram of a 3 Gbps signal

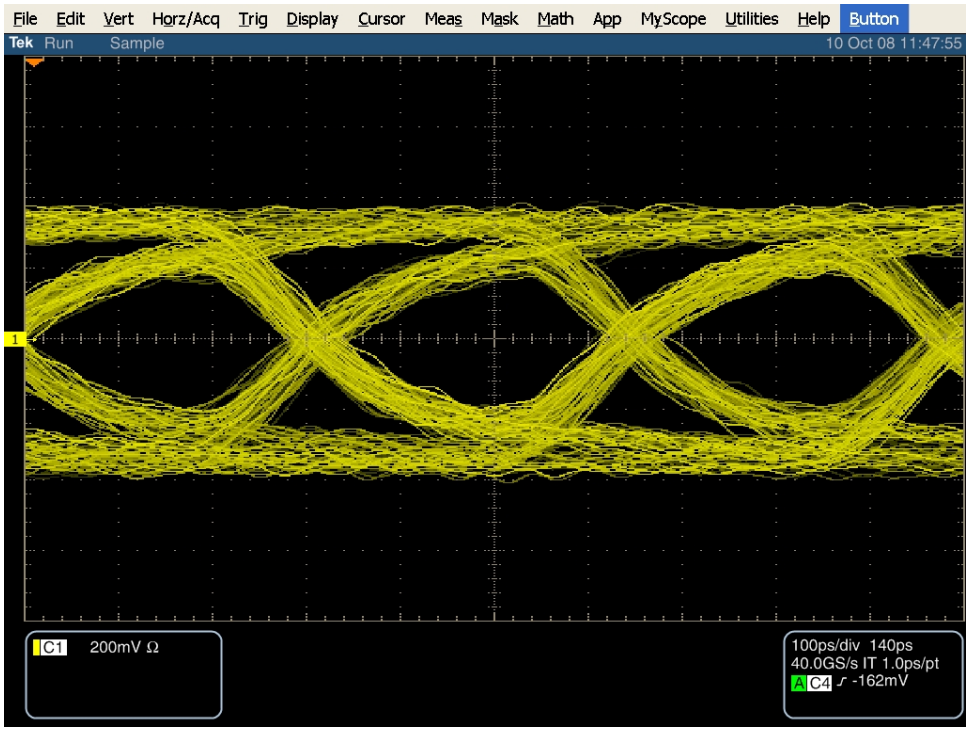

Figure 2. Eye Diagram of a 3 Gbps signal with significant degradation

When moving from an HD-SDI system, running at 1.5 Gbps, to a 3G-SDI system running at 3 Gbps, there are many factors that come into play, conspiring to keep things from working as we would hope. In this paper I will explore three of these factors:

1. **Equalizers and the physical media**
   In broadcast video we are very dependent on the performance of cable equalizers to get our systems to operate correctly. When an SDI signal is sent through a length of cable its characteristics are degraded, and before any processing can be done on that signal, it needs to be restored. Adaptive cable equalizers do a large portion of this processing.

2. **Equipment size**
   The new generations of studios being designed are demanding larger, and larger installations. Not very long ago, a 256x256 router was considered to be a very large router. Today there are several 1K x 1K routers either available or in development. The electrical and physical size of these pieces of equipment have consequences on the signal integrity of the SDI signals that they are handling.

3. **Relaxation of residual jitter specification by SMPTE**
   SMPTE 259M (SD-SDI) and SMPTE 292M (HD-SDI) both specify that the signal being provided by a piece of equipment that claims compliance may have no more than 0.2UI of jitter on it's output. This means that the user is guaranteed that his signal is stable for no less than 80% of the unit interval. Passing this signal through cable, or other processing elements will degrade this.

After having looked at these three areas, I will make suggestions both to the equipment manufacturers and to the users on what things can be done to increase the chances of success when designing for 3 Gbps SDI.

Equalizers

As an electrical signal goes through cable, the cable acts like a low-pass filter. For most of the frequency band of interest to video engineers, the characteristics of this filter are that it attenuates the signal by an amount proportional to $\sqrt{f}$, where f is the frequency of interest. This means that if two signals go through a given length of cable, one of the signals being an HD-SDI signal, and the other being a 3G signal, the 3G signal will be smaller by a factor of 1.4 when compared to the HD-SDI signal. Cable equalizers use adaptive, high pass filters with a response that compliments the $\sqrt{f}$ characteristic of the cable – if they work well, then they eliminate the degradation caused by the cable.

Figure 3 shows the original HD-SDI signal, then in Figure 4 we can see what the eye diagram looks like after the signal has passed through 100m of 1694A coax cable, and then in Figure 5, we see this same HD-SDI signal after cable equalization. You can see that the equalizer restores the original amplitude of the signal.

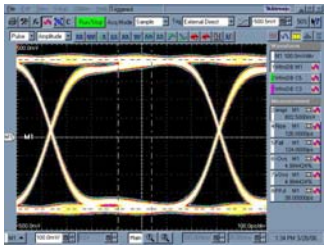

Figure 3. Initial HD-SDI signal

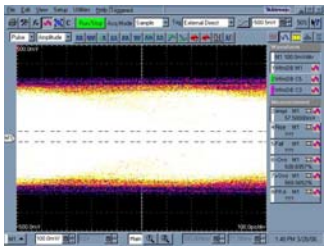

Figure 4. HD-SDI signal after 100m of cable

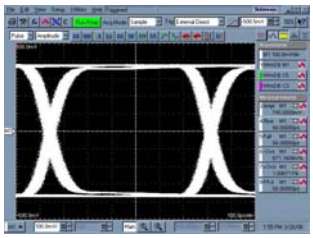

Figure 5. HD-SDI signal after equalization

Although the cable equalizer is able to restore the original amplitude and the rise/fall times of the signal, there is some noise (jitter) added to the signal which can be seen by the 'X' portions of the eye diagram having fatter lines after equalization than they had originally. To prevent this jitter from accumulating too much, another circuit is used in which a PLL locks onto the input signal, and regenerates a clean clock with which the data is reclocked. These circuits (known as reclockers) can generally tolerate up to about 0.6 UI of jitter before they are unable to reliably reclock the input signal and remove accumulated jitter.

Jitter is added as noise, which is then amplified by the high gain stages in the equalizer, the gain of these stages increases with increased cable length (more attenuation), or with increased data rates (also more attenuation). The length of cable that can be used in any particular link, and the maximum datarate are determined by the 0.6 UI input jitter tolerance limit of the reclocker.

Equipment size

In this section I am going to focus on routers. Virtually every piece of equipment within a television broadcast studio is touched by the router, so router performance has a very large impact of the success or failure of a studio installation.

Most routers have an architecture in which the signal sees three cards, and two backplanes as shown in Figure **6.**

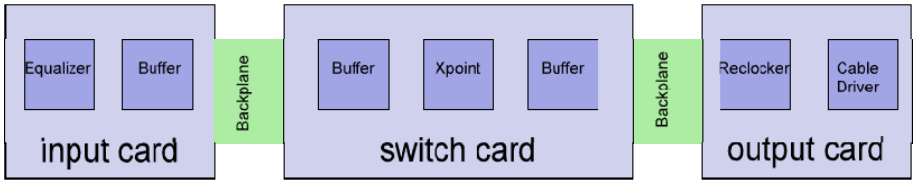

Figure 6. Typical Router Architecture

In general, each channel of the input card consists of a cable equalizer and some circuit which will drive the equalizer output onto the backplane, the switch card consists primarily of backplane receivers and drivers, and the crosspoint switch, and on the output card there is a reclocker, and then a cable driver. Note that since the only reclocker in the system is on the output card, jitter accumulates through the system until it reaches the output card.

As the routers become larger, the backplanes become physically larger, as well as more heavily loaded, both of which contribute to greater amounts of jitter being added to the signal.

Jitter Budget (all at 3 Gbps)
Typical jitter added by 10" of FR4 backplane trace: 0.1 UI
Typical jitter added by a large (144x144) crosspoint switch: 0.05UI
Typical jitter added by backplane drivers 10ps (0.03UI)
Typical jitter added by equalizer:
70m cable: 0.2UI
100m cable: 0.3UI

Looking at this, it is apparent that if the original source equipment has an output jitter of 0.3UI, it is going to be very difficult to design even a small router which is able to receive the signal, switch it, and then reclock and drive the signal without generating errors.

Relaxation of jitter specification by SMPTE 424M

In order to be considered compliant with SMPTE 424M (the 3 Gbps SDI physical specification), a piece of equipment must have output jitter of no more than 0.3UI. The standard for HD-SDI is 0.2UI, and the Unit Interval is twice as large. This means that for a 3 Gbps SDI receiver, the time during which the receiver can count on a stable signal is about 1/3 that of the HD-SDI signal. A footnote for SMPTE 424M indicates that it is strongly recommended that SMPTE 424M

equipment be designed with no more than 0.2UI of output jitter, but the designers of receivers cannot count on a recommendation, they can only rely on the specification. The effect of this is that for many receivers, the maximum length of cable that can be supported will be substantially shorter if the piece of equipment driving that cable has a poor output jitter specification. This places equipment designers in a bind. If they specify supported cable lengths assuming drivers that just meet spec, they will be guaranteed that their system will always work, but less scrupulous manufacturers my specify their receivers based on the assumption that source equipment meets the 0.2UI specification, allowing them to claim longer cable length support for a product which in actual fact comparable. The landscape for the 3 Gbps studio installer is liable to be treacherous indeed.

Strategies for Successful Equipment Design

Suggestion #1 Reclock !

As could be seen in the section on routers, at 3 Gbps, with current state of the art components, there is not much room for error in the jitter budgets before errors start the come into the system. One way that the system could be given more margin is by adding an additional stage of reclocking – this time on the input card, in addition to the reclocker on the output card. This means that there is much more room for jitter accumulation within the system, and that overall system performance is less dependent on cable length or transmitter output jitter. The problem with this is that a reclocker is an expensive component, and one would be required per input channel, having a negative impact on the overall cost of the router – and the specification that it would help with is input jitter tolerance, which is not one of the specs that customers usually look at first – will they be willing to pay for it?

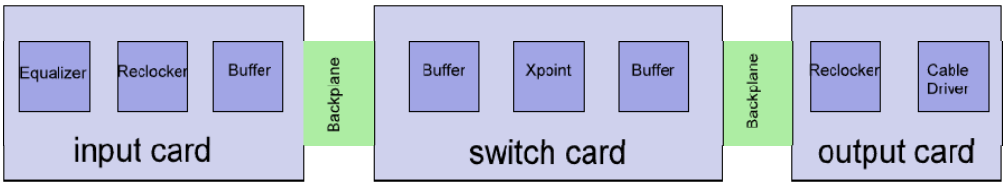

Figure 7. Equalizer architecture with reclocking input card

Suggestion #2 Equalize

Another strategy that the router designer might use is to put FR4 equalizers on the backplane receivers of the crosspoint card and/or the output card. Some of

the National reclocker chips which are intended for large routers have integrated FR4 equalizers (LMH0356) and the financial impact of including this function is minimal.

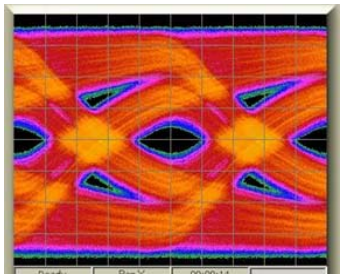

Figure 8. 3 Gbps signal after 1m of backplane trace

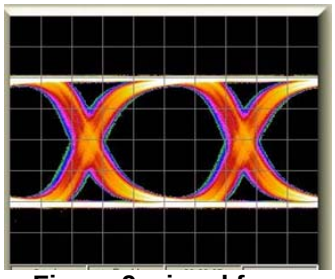

Figure 9. signal from Figure 8 after LMH0356 equalization

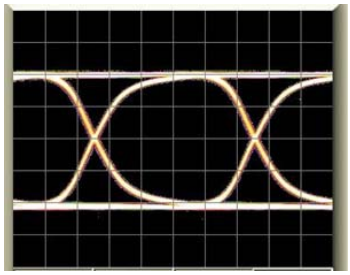

Figure 10. 3 Gbps signal after FR4 equalization and reclocking.

In Figure 8 you can see the eye diagram of a 3 Gbps signal after passing through 1m of backplane trace – and you can see how much the eye has been degraded. The LMH0356 reclocker has an FR4 equalizer built in to it's front end, and by simply enabling this equalizer the eye is restored to that seen in Figure 9. To remove the remaining jitter, the LMH0356 reclocking function is enabled, resulting in the eye diagram of Figure 10.

Suggestion #3 Pay attention to Power

As the sizes of routers increase, so will their power dissipation. Power is a factor both in terms of the cost of operating the system, but also because of the heat which is generated. Most electronic circuits operate better at lower temperatures, so keeping cool is not just a good way of keeping the accountants and environment happy, it also makes for a better performing product. Often although a router may be very large, only a small fraction of the channels may be used at any particular time. If a control system is smart enough, and the hooks are put into the design, parts of the switch that are not being used can be powered down, saving power. Many of today's integrated circuits are being designed with control interfaces where the chip will tell you if its inputs are active – if your serializer is not receiving a clock, then it is pointless to be burning a lot of power on the device, and action can be taken to power it down! Some cable drivers such as the LMH0307 are able to detect the presence of a load connected to their output – and if they detect that there is no load present, they can power down upstream circuitry such as the LMH0356 reclocker.

Suggestion #4 Beat the specs, and brag

Installation design at 3 Gbps is going to be much more difficult than it was for HD-SDI. Installers are going to be forced to pay closer attention to a lot of the equipment specs, and will increasingly be making purchasing decisions based more on performance, and less on other factors. The winners at 3 Gbps will be

the ones with superior performance, and with test data, and spec sheets to prove it.

Strategies for successful studio design.

Suggestion #1 Less jitter is better
Creating viable 3 Gbps SDI installations would have been an easier task had equipment manufacturers been forced into making lower output jitter products, rather than just being encouraged to do so. Look closely at the output jitter specifications of every piece of equipment in the plant – if it is not lower than 0.2UI, then you may want to consider following that box immediately with a good quality reclocking Distribution Amplifier (DA).

Suggestion #2 Pay attention to cable lengths.
Everything is going to be closer to the edge with 3 Gbps than it was at HD-SDI. Longer cable runs will be more likely to generate issues than they were at lower data rates. Be prepared with DAs, or with the prospect of upgrading the equipment at one end of the cable or the other.

Suggestion #3 Verify performance.
Testing parameters such as output jitter or input jitter tolerance is difficult. Since these are still the early days of the 3 Gbps SDI interface, the available equipment is either expensive, inaccurate, or both. Despite this, the key to success will be to understand what the various pieces of equipment do. Some of this can be done with general purpose test equipment. Ask manufacturers for detailed test data, and take the time to understand what it is saying.

Note:
A version of this paper was presented at the **2008 SMPTE Conference**.

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