CLC012,CLC014,DS90CP04,DS90CR481, DS90CR483,DS90CR483A,DS90LT012A

Eye Opening Enhancements extend the reach of high-speed Interfaces

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Technology Edge

Eye Opening Enhancements extend the reach of high-speed Interfaces
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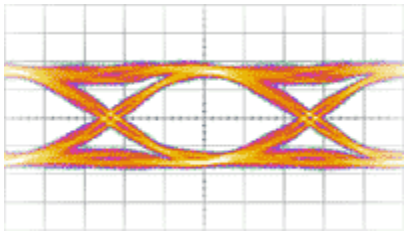

Typically the faster you go, the shorter you go. Data rate is inversely proportional to cable length. However new techniques offered in the latest generation of interface parts provide eye opening enhancements to extend the reach of the interconnect. Prior generations of interface devices focused mainly on level translation only. The current generation of devices uses new techniques of signal conditioning to optimize the signal quality at the receive end. This includes pre-emphasis, encoding, equalization, and termination optimization.

LVDS (Low Voltage Differential Signaling) has become a very popular transmission method when vast amounts of data need to be moved in a short amount of time. SDI (Serial Digital interface) is similar to LVDS in speeds, but utilizes a larger signal swing and drive levels. It is commonly used on interconnects in the tens of meters to hundreds of meters. CML (Current Mode Logic) is the IO commonly deployed on SERDES parts operating in the 1-5+ Gbps line speed range. These eye-opening enhancements are applicable to all three interface technologies. Devices are now available that integrate more digital and special analog functionality to extend the reach by improving the output signal and also using other higher layer enhancements. This article provides a discussion on four such enhancements.

Enhancing signal quality prior to sending it with Pre-emphasis -
Pre-emphasis is a unique signal improving technique that opens the eye pattern at the far end of the cable for point-to-point applications. The reason it is unique is that it does not utilize or burn any bit time, so the bus is still 100% efficient for data transfer. Every bit sent is valid information.

A simple model for the interconnect media between the line driver and receiver is a low pass filter. A pulse that is driven down the media will be distorted by the cable loading. The distortion is a function of cable parameters and most importantly the cable length. This effect tends to limit cable length for LVDS transmission to a few meters and CML backplanes to less than 0.5 meters.

Pre-emphasis adds additional output current during the transition time of the bit. This tends to speed up the edge rate and also provides a bit of over-shoot to the signal at the driver output. This modified waveshape is still loaded by the interconnect, but the end effect is now much different and improved.

Figure 1 illustrates an output signal at the TX with 4 different settings of pre-emphasis super imposed. Note the small amount of overshoot and also the faster edge rate that pre-emphasis provides.

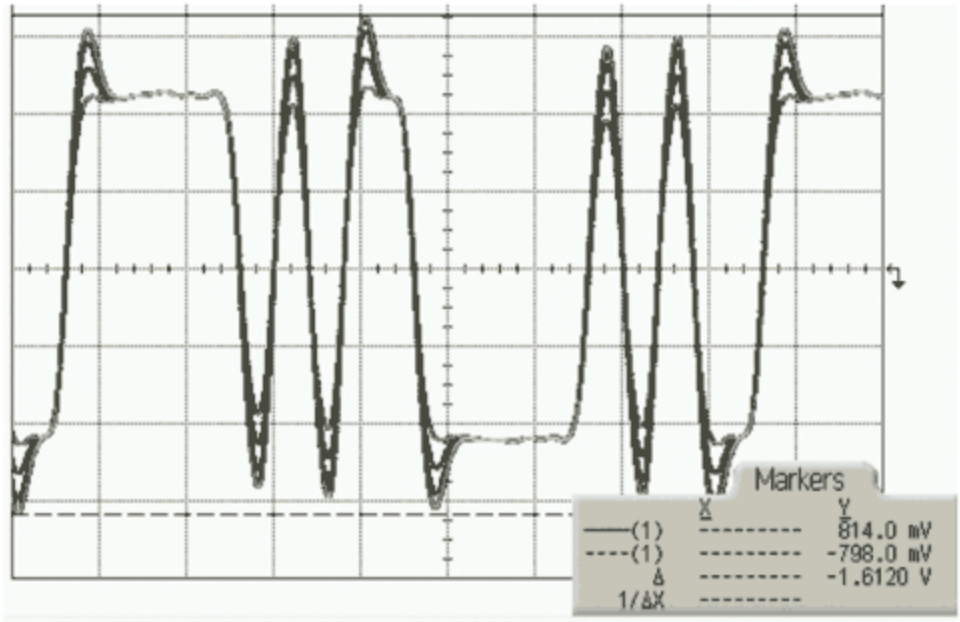

Figure 1 - CML signal at TX output vs. pre-emphasis setting (4 levels)

Figure 2 shows the eye pattern at the receiver input after the backplane loading. Note how the edge rates have degraded, jitter is high and ISI (inter-symbol Interference) effects have closed down the eye. In figure 3 the eye is more open due to the pre-emphasis setting and jitter is greatly reduced. Figure 1,2 and 3 show the CML output of a 2.5 Gbps SERDES. The amount of pre-emphasis is selected via two control pins.

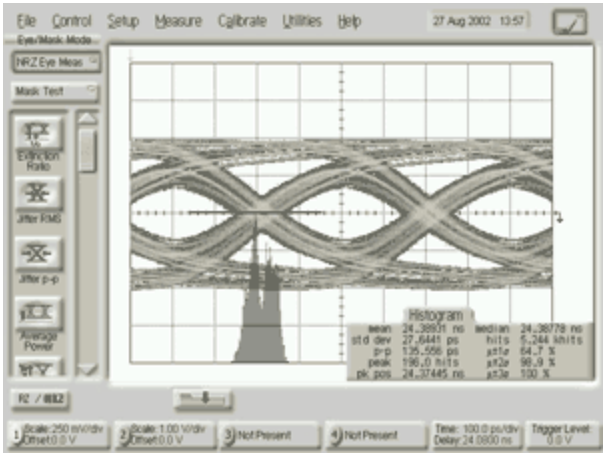

Figure 2 - CML signal without pre-emphasis at the Receiver input

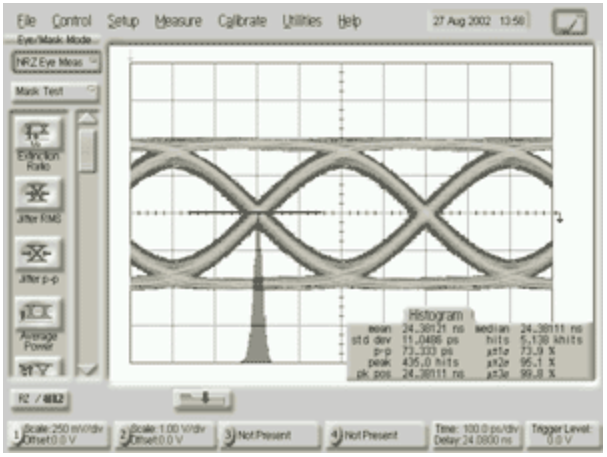

Figure 3- CML signal with pre-emphasis at the Receiver input

Pre-emphasis is also available on the DS90CR481 and DS90CR483 Channel Link transmitters to extend cable lengths. With pre-emphasis, lengths two to four times of standard LVDS transmission are possible. On the

DS90CR481/483, the amount of pre-emphasis current is determined by the RPRE resistor value connected to its respective pin. This single resistor sets the amount of pre-emphasis on all nine LVDS outputs. This allows for the application select the right amount of pre-emphasis for the given cable length.

How much is enough? Too much pre-emphasis can also be of concern. The larger signal will generate more noise, crosstalk, and increase power dissipation. Signal quality measurements are recommended to determine the proper amount of pre-emphasis for the application. Overshoot should not be present in the eye at the receiver input.

Recovering the signal at the receiver with Equalization -
Pre-emphasis alone may not be enough. Equalization may also be used to further open the eye. Equalization can be an analog technique to reverse the low pass effect of the cable with a high pass filter to recover and restore the original signal. While harder to illustrate with scope plots since the recovered signal is internal to the receiver silicon, its net effects are similar to that of pre-emphasis in opening eyes. The goal of the equalizer block is to provide the inverse transfer characteristics of the cable to fully recover the signal. Equalization typically requires a minimum transition density or encoding to operate correctly. This feature is available CLC012 and CLC014 cable equalizers. Figure 4 shows the eye pattern at the far end of the cable operating at 622 Mbps and 200 meters. Note that the eye is completely closed (no opening at all)! The CLC012 recovers the signal and generates the eye pattern that is shown in figure 5.

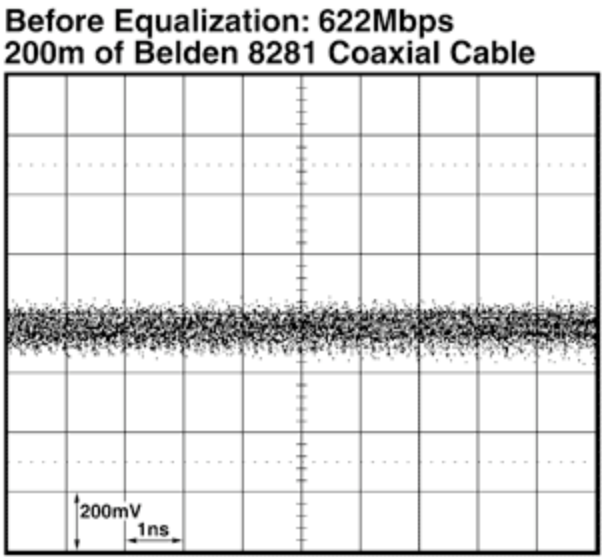

Figure 4 - Completely closed eye pattern at CLC012 receiver inputs

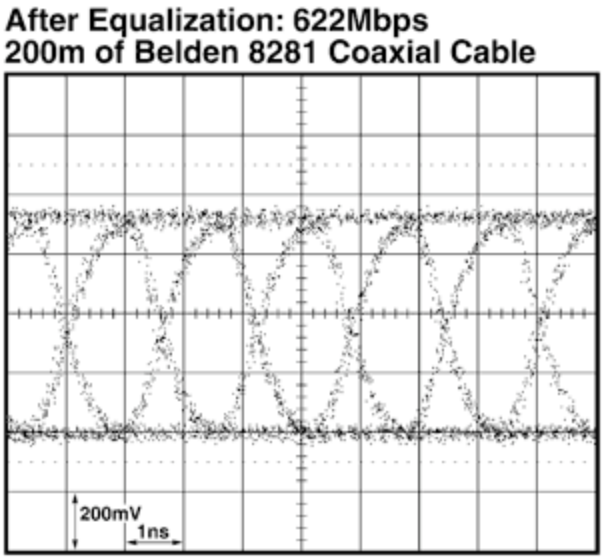

Figure 5 - Recovered Eye Patter at the CLC012 Equalizer Output

Using Encoding to improve signal quality even further -
DC Balancing (Encoding) is yet another way to improve signal quality and can be used with pre-emphasis and equalization. This is more of a digital approach to the cable driving problem. It is targeted specifically at the ISI problem. ISI in short is the distortion of the current bit due to the logic state of the prior bits that preceded it. Let's think about a simple clock signal first. A clock is a periodic signal and it has a 50% duty cycle, therefore it is also DC balanced. The line is HIGH for 50% of the time and LOW for 50% of the time, thus it is balanced. This is the reason that clock lines tend to have cleaner signal quality compared to non-encoded NRZ data lines. It is also this fact that if we send clock and data in parallel, that the cable length is still determined by the bit time of the data (minimum pulse width sent) and not the clock, even though its minimum pulse width is one half of the data pulse

width (note this example assumes single edge clocking of the data).

ISI on the data line is caused by the charging of the line in one direction due to the data pattern sent. If the line is held HIGH or LOW for a very long period of time, the line fully charges and the steady state value tends to be higher than that of a HIGH bit that just switched HIGH. This higher value starting point will create increased jitter as it will take longer for that bit to transition to the threshold compared to a bit that was just driven HIGH. This increased amount of jitter and signal quality impact may limit the application's maximum data rate. Another way to limit ISI is to modify the data such that it does not send long strings of HIGHs or LOWs. DC Balancing is once such way to prevent these long strings of the same logic state.

DC Balancing can be accomplished a number of ways. One such way is to keep track of the data sent and count the number of ones that were sent. Before sending the next set of data, the number of ones are checked again, it the count is still increasing, the data is modified (inverted) and that makes the running ones count decrease. The net effect of this is to keep the charge on the line within a certain bound. The receiving device needs to do two functions, first it must still recover the data, and it must also detect if the data has been modified. If modified data is detected then it needs to correct for it. A simple and efficient way to do this is to assign a data bit to indicate if the "data" was modified or not. With this, the receiver simply monitors that special bit, and decodes the data if it has been modified to maintain balance on the line. DC Balancing is useful with serialized data streams and is available on the 48-bit Channel Link chipset (DS90CR483/484). The transmitter uses frames of serialized data that are 6-bits in length. It appends a bit to the end that indicates if the data is in it original state or has been modified. Thus a 7-bit frame is sent, and the link is 86% efficient. This is quite high, only 14% of the link's bandwidth is lost due to the special information being sent that DC Balances the data. This is also knows as 6b/7b, for 6 bits of information are sent in every 7 bits done the line. The encoding benefit of the Channel Link chipset (DS90CR4xx) is shown graphically in figure 6. The top illustration shows the charge count increasing with a long sequence of ONEs sent. Note that the single ZERO bit does not make a full transition. The lower graphic is also a long string of ONEs sent but with DC Balance. After six ones, the next payload of ONEs is inverted and flagged by the appended DCB bit. Then another six ones are sent followed by the single ZERO data bit. In the top example the line changed to a positive 19 bias, in the bottom example the line was constrained to positive 5 for a similar pattern. With less charge on the line, the ZERO bit was a full transition and width. DC Balance is useful in application pushing extreme lengths or maximum data rates.

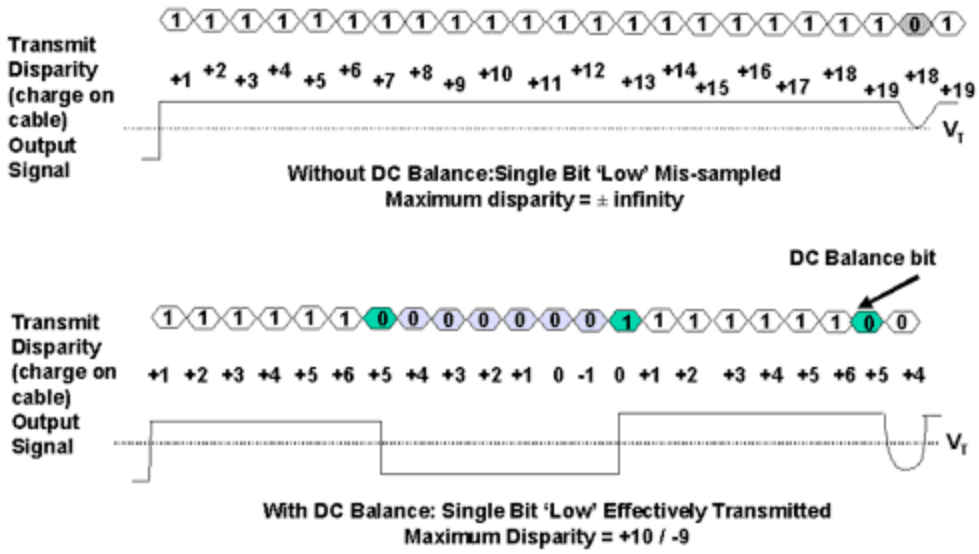

Figure 6 - Channel Link Non DCB vs. DC Balance Encoding

Other schemes accomplish DC Balance with differences in efficiencies. For example, 8b/10b which is very popular in datacom applications is only 80% efficient. As every 10 bits sent, actually only pass 8 bits of

information. The 10-bit codes are special, as they guarantee a certain number of transitions, are DC Balanced, and prevent the occurrence of long transition-less sequences (5 maximum).

Internal Termination reduces stub effects and enhances signal quality

Another problem that can occur and limit high-speed transmission are transmission line reflections from stubs. Even in a point-to-point bus configuration that offers the best signaling environment, a stub may exists and can degrade signal quality. If the distance from the termination resistor to the receiver input is too long, it will act as a stub and signal reflections will occur. To limit this, the termination could be moved on-chip effectively eliminating the stub all together. In general a termination that is matched to the line to within 10% is sufficient, of course the closer match the better. Figure 7 illustrates the comparison of an external termination (with stub) to an internal termination (stub-less). The simulated single-ended waveforms are shown in figure 7. The ringing is a result of the 1.5-inch stub. Internal termination offers the superior signal quality due to the stub-less interconnect. Figure 8 is the same simulation but plotted differentially. The ringing from the stub is of concern for two reasons. It generates noise, and also erodes the differential noise margin. The driver in the simulation is the DS90CP04 which offers LVDS-like signaling at data rates up to 2.5 Gbps.

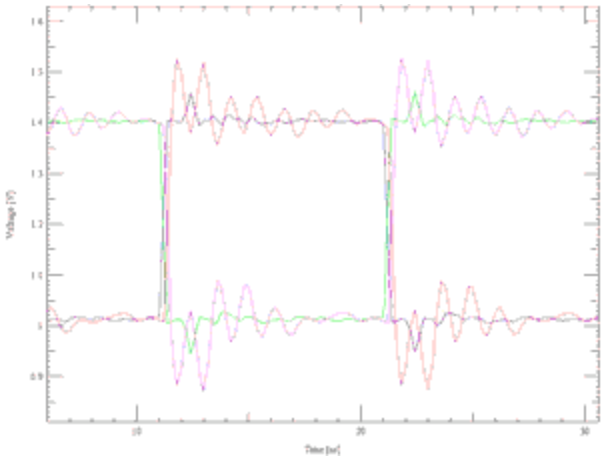

Figure 7 - Stub Comparison - Single Ended View

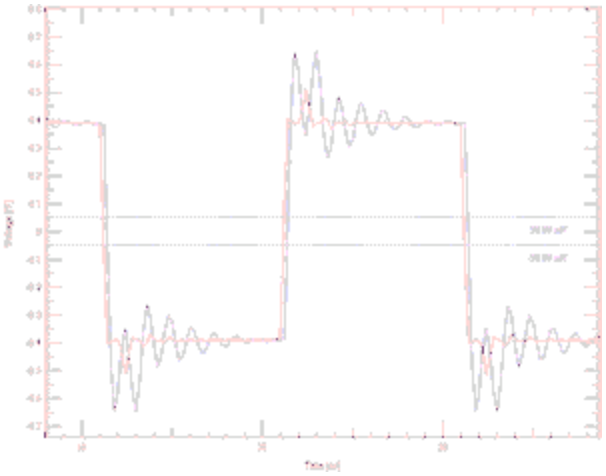

Figure 8 - Stub Comparison - Differential View

New devices offered from National provide internal termination for point-to-point applications. Note that in multidrop or multipoint applications an internal termination is typically not desired, as the driver would see all the receivers in parallel and be overloaded (10 receivers - each with a 100 ohm load would present a 10 ohm load to the driver!).

The DS90LT012A is a single LVDS receiver with internal termination offered in two different extremely small packages (SOT & LLP). This device is intended for applications up to >400 Mbps and is only limited by the speed of its LVCMOS output.

Internal terminations minimize the stub effects greatly, improve the resulting eye pattern and signal fidelity.

Summary

These four enhancements are new ways to extend the reach of high-speed interfaces to greater lengths. Pre-emphasis, encoding and equalization can be used together to provide extremely high throughputs. Termination optimization is also not to be forgotten. These features are now available on the current generation of interface devices and usher in a new era of high-performance robust Interfaces.

Referenced Datasheets
DS90CP04 4x4 Low Power 2.5 Gb/s LVDS Digital Cross-Point Switch
DS90CR481/2 48-Bit LVDS Channel Link Serializer - 65 -112 MHz
DS90CR483/4 48-Bit Channel Link Serializer - 33-112MHz
DS90LT012A 3V LVDS Single CMOS Differential Line Receiver
CLC012 Adaptive Cable Equalizer for ITU-T G.703 Data Recovery
CLC014 Adaptive Cable Equalizer for High-Speed Data Recovery

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