Application Report
SNLA118C–May 2009–Revised April 2013

AN-1972 Board Layout Challenges in Serial Digital Interface

ABSTRACT

This application report provides recommendations to meet board layout challenges in SDI designs, and shows specific layout examples for cable equalizers and cable drivers.

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1 Introduction

Television and cinema have entered the digital age. Video pictures are used to transport at standard definition rate (270Mb/s), upgraded to high definition rate (1.485Gb/s), and are now migrating to the 3Gbit/s rate. The migration to higher speeds enables higher resolution images for entertainment, yet presents challenges to hardware engineers and physical layout designers alike. Texas Instruments offers a family of multi-rate SDI integrated circuits that supports high performance professional video transport over long distances. Careful high speed board designs should be used in order to maintain the superb signal quality offered by these integrated circuits. The SMPTE standards that specify the Serial Digital Interface have defined requirements and challenges for SDI designs. This application note outlines the layout challenges facing hardware engineers, and provides recommendations to deal with these challenges.

2 Trace Width and Board Stack-Up

One of the unique layout challenges encountered in SDI boards is the coexistence of the 75Ω traces for routing digital video signals, and the chip-to-chip routing that runs on 100Ω differential traces to reclockers, SerDes or FPGA's that prefer finer trace widths. Figure 1 is the schematic diagram of the LMH0302 cable driver with its inputs connected to 100Ω traces and its outputs connected to 75Ω traces. Very often, both types of traces are routed on the top layer where the components reside. Trace widths good for 75Ω may be too wide for running 100Ω traces.

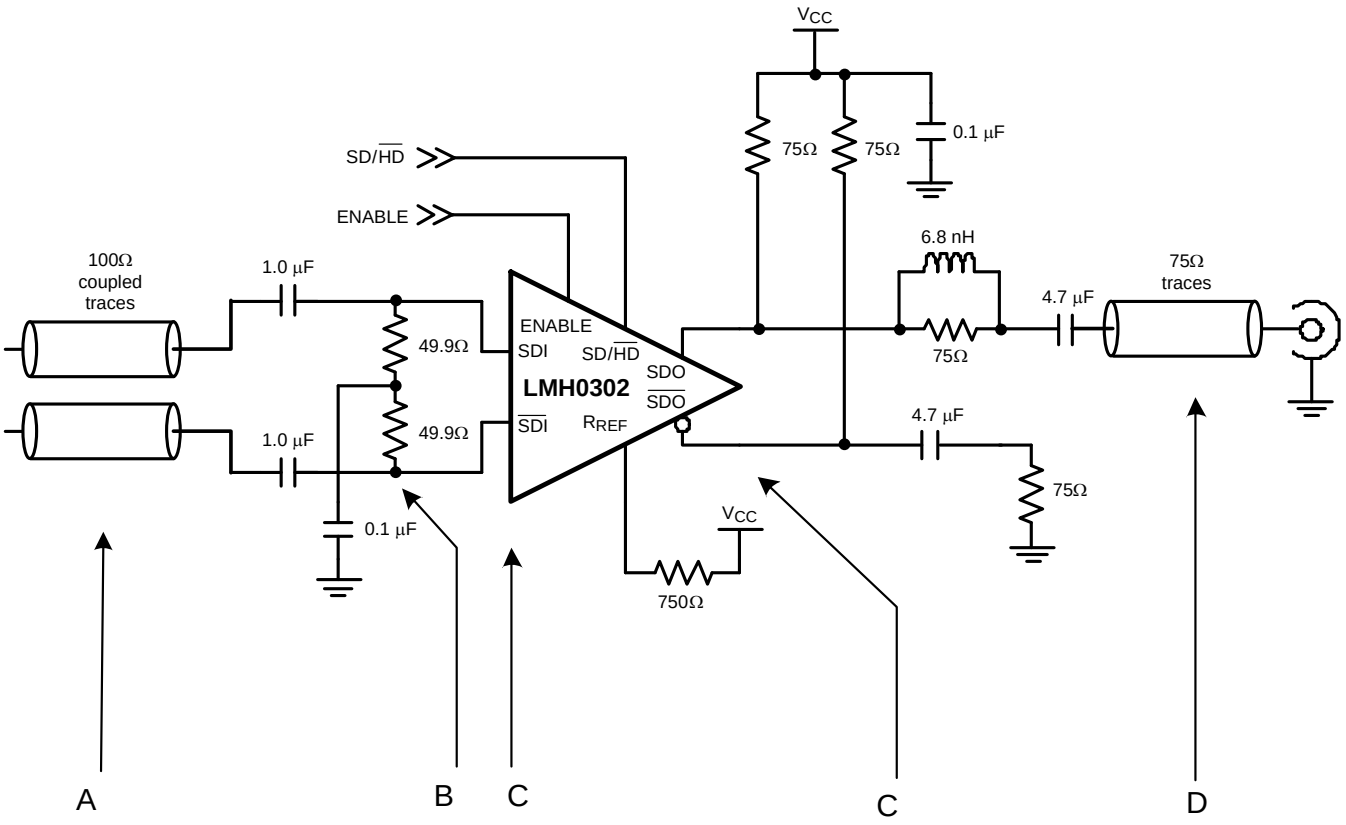

Figure 1. Schematic Diagram of the LMH0302 Cable Driver

What should be the correct trace width? A 6-mil wide microstrip has transmission loss of about 0.3dB/inch at 1.5GHz. For SDI speeds less than 3Gb/s, copper loss is small and is not a big concern in choosing the trace width. Because there are several passive components hanging on the 75Ω trace, its trace width should be comparable to the landing pads of these components in order to minimize the effect of the impedance drop caused by the larger pads. The smallest physical size surface mount components should be used for the same reason. A passive component of 0402-size requires landing pad of about 20mils x 25mils, so a trace width of about 15-25 mils is optimal for the 75Ω traces. If the 75-Ω trace is 20-mil wide,

then a single-ended 50Ω trace would be a very wide trace of 42mils. Fortunately, for a pair of 100Ω differential traces, very tightly coupled 8-mil wide microstrips separated by 6mils can be used with strong mutual coupling to bring the impedance to 100Ω. Figure 2 shows a stack-up example of such an implementation. Unfortunately, it is impossible to maintain uniform spacing when routing the pair of traces in-and-out from the IC, the external termination resistor, or AC coupling capacitors. Branching out the traces to these components breaks the coupling and the impedance increases. Figure 2 illustrates the impedances of the traces, and the effect of branching out at the IC's landing pads, and at the 0402-size resistor.

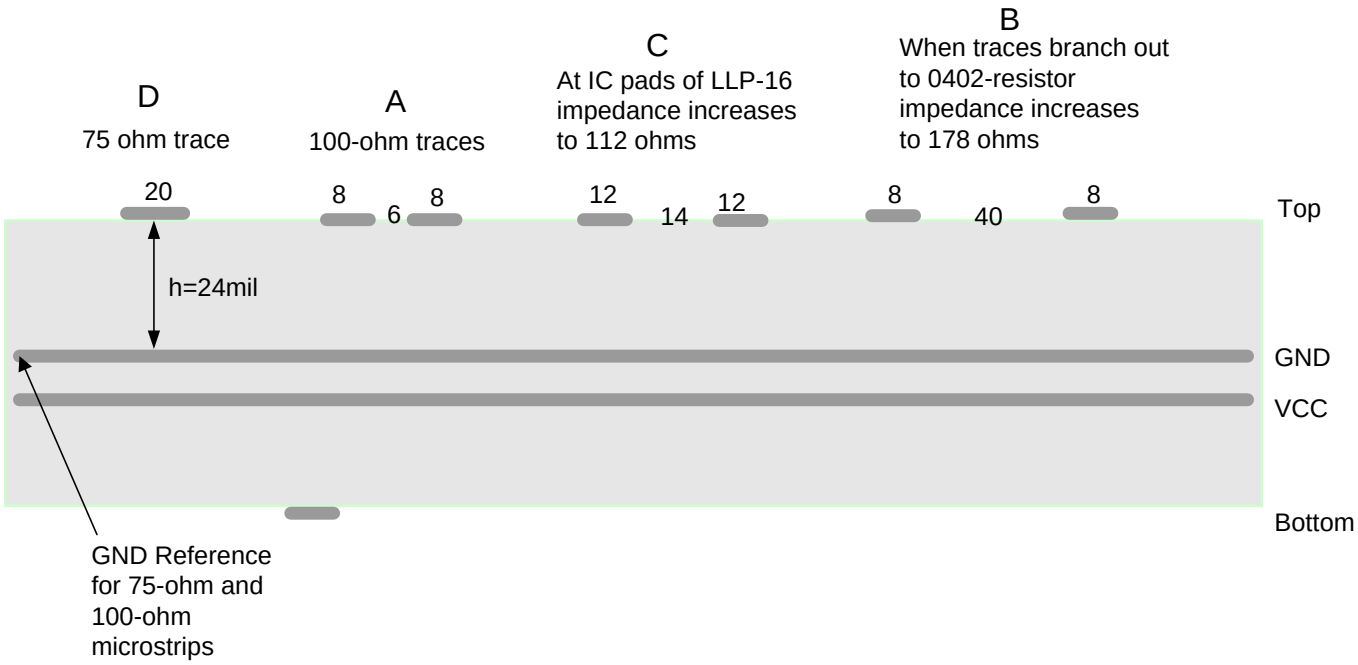

Figure 2. Stack-up example with one ground reference for 75Ω and 100Ω traces

This problem can be solved by using two separate ground references. Figure 3 shows an improved board stack-up, using layer 2 as the ground reference for a pair of 8-mil wide loosely coupled differential traces separated by 10mils, and using part of layer 4 as the ground reference for the 75Ω traces. The two ground references are electrically connected together through some ground stitching plated-through holes. This board stack-up allows the freedom to choose the trace width for the 75Ω traces by adjusting the dielectric distance "h2", and the trace width for the 100Ω traces by adjusting "h1". This arrangement has smaller impedance fluctuations when the loosely coupled 100Ω trace branches in-and-out of components and integrated circuits. As shown in Figure 3, the ground reference for the 75Ω trace is a metal island carved out in the signal layer 4.

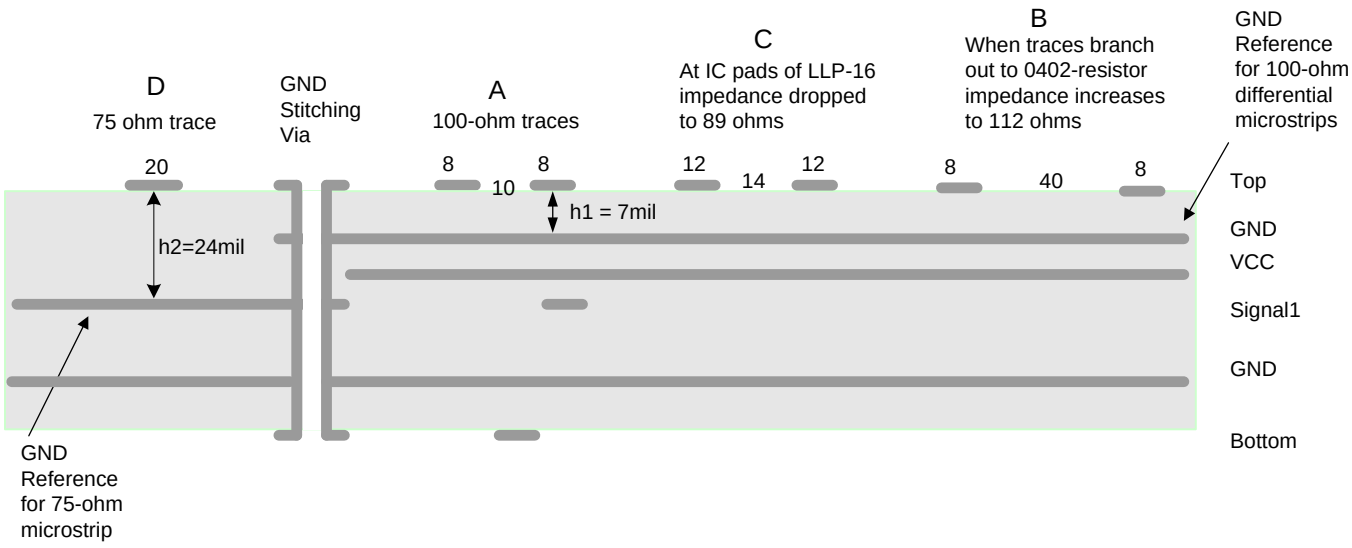

Figure 3. Stack-Up Example With Separate Ground Reference For 75Ω And 100Ω Traces

3 Impact from External Components

In some cases where there is a strong desire to use very fine trace width, the amount of impedance drop caused by the large component landing pads connected with a fine width trace becomes a bigger concern. Figure 4 illustrates an example of such a board stack-up. In this stack-up, 10-mil wide 75Ω traces are reference to layer 4. The 20-mil wide landing pad of an 0402-size resistor introduces excess capacitance and causes the impedance to drop from 75Ω to about 57Ω at the pad. Similarly, a 20-mil pad connected to a pair of 5-mil wide differential microstrips causes the impedance to drop from 100Ω to about 74Ω. To compensate for excessive drop in impedance caused by component pads, it is possible to use a ground relief under the pads to shave off the excess parasitic capacitance and bring the impedance closer to the target values. Figure 4 illustrates this technique by removing the metal in the plane(s) under the component pads.

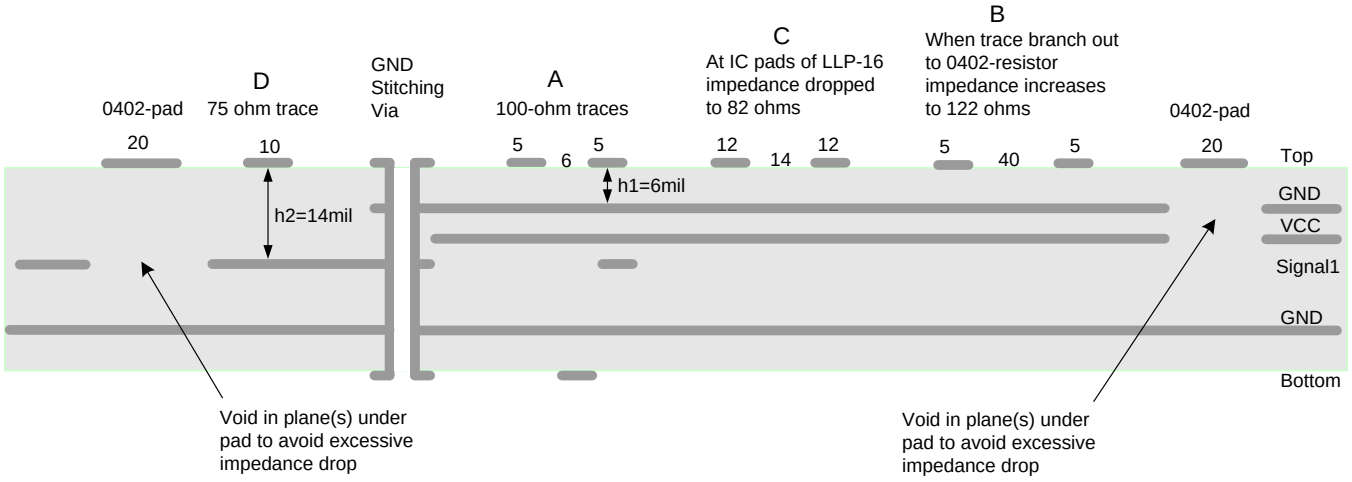

Figure 4. Stack-Up Example With Fine Trace That May Require Ground Relief Under Pads

4 Return Loss Challenge

SMPTE 259M, 292M and 424M standards specify the requirements for the Serial Digital Interface used to transport digital video at SD, HD and 3Gb/s over coaxial cables. One of the requirements is the output signal amplitude of 800mV ±10%. This amplitude tolerance requirement has to be met with an external termination resistor of 75Ω±1%, instead of an integrated termination with wider tolerance. Another requirement is the input return loss (IRL) and the output return loss (ORL), which basically specify how well the input or output port looks like a 75Ω network. Figure 5 shows the SMPTE requirements on return loss specifications along with the input return loss of an SDI port.

The SMPTE return loss specifications require the use of an external impedance balance network, consisting of a parallel combination of an inductor and a 75Ω resistor, for counteracting the capacitance effect from the input or output circuit of an integrated circuit. SMPTE also defines the use of AC coupling for transporting uncompressed bit stream with heavy DC unbalance. This specification requires the use of fairly large AC coupling capacitor (4.7µF) to avoid low frequency DC wander.

These SMPTE requirements mean that there will be several components hanging on the trace between an integrated circuit and its BNC connector. These external components make high speed board layout more challenging. Each component pad is going to introduce some amount of impedance discontinuity that impacts the overall impedance matching to 75Ω, and the locations of these components are also critical in meeting return loss requirements.

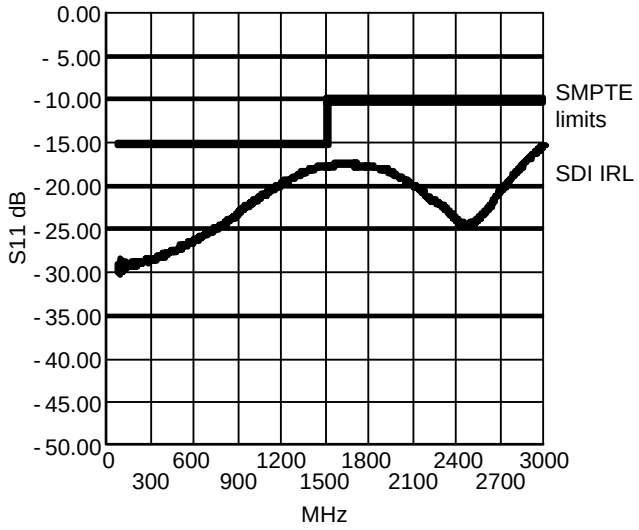

Figure 5. Plot Of Input Return Loss (IRL) of an SDI Port and SMPTE Limits

5 Layout Guidelines

For SDI boards, the data rates are less than 3Gb/s, and signal transition times are above 100 picoseconds. The challenge in SDI board layout is not in speed, but in devising a layout strategy to minimize impedance mismatches from the many external components on the 75Ω SDI port, and a board stack-up that supports both 75Ω and 100Ω traces. We can meet these challenges by following a few simple layout guidelines:

- Set trace impedances to 75Ω±10%, 100Ω±10%
- Use the smallest size surface mount components
- Use the smallest size component pads to minimize impedance discontinuities to the trace impedance
- Select trace widths that minimize the impedance mismatch along the signal path
- Select a board stack-up that support 75Ω single-end trace and 100Ω loosely coupled differential traces
- Use surface mount ceramic capacitors and RF signal inductors
- Place components that impact return loss (termination resistors, impedance balance network) closest to the IC pins
- Maintain symmetry on the complimentary signals

- Route 100Ω traces uniformly (keep trace widths and trace spacing uniform along the trace)
- Avoid sharp bends; use 45-degree or radial bends
- Walk along the signal path, identify geometry changes and estimate their corresponding impedance changes
- Use good signal launch for BNC connectors and maintain 75Ω impedance with well designed connectors' footprints
- Use solid planes. If ground relief is needed to shave off excess parasitic capacitance, use with care; consult a 3D simulation tool to guide layout decisions
- Use the shortest path for V_{CC} and Ground hook-ups; connect pin to planes with vias with no trace

6 Layout Example - LMH0302 Multi-Rate Cable Driver

Figure 6 shows the schematic diagram and Figure 7 shows a conceptual layout diagram of National's LMH0302 3Gb/s/HD/SD SDI cable driver. The stack-up shown in Figure 2 is used in this example. Layer 2 is the ground reference for the 8-mil wide 100Ω differential traces that go to the input pins SDI+ and SDI-. The 100Ω termination resistor R6 is placed closest to the input pins to avoid the capacitive stud effect. An island of metal on layer 4 is used as the ground plane for the 75Ω traces. The two ground references are stitched together using the ground via for the device's DAP connection.

The 75Ω terminations R2 and R3 are placed as close as possible to the driver's output pins SDO+ and SDO-. The impedance matching components L1 and R1 are placed close to the output pin SDO+, where it is most effective in compensating for the capacitance of the driver's output.

This design uses 0402-size components to minimize the impedance change to the 75Ω trace built with 20-mil microstrip referenced to layer 4. The footprint used for the BNC should have good signal launch for maintaining good return loss.

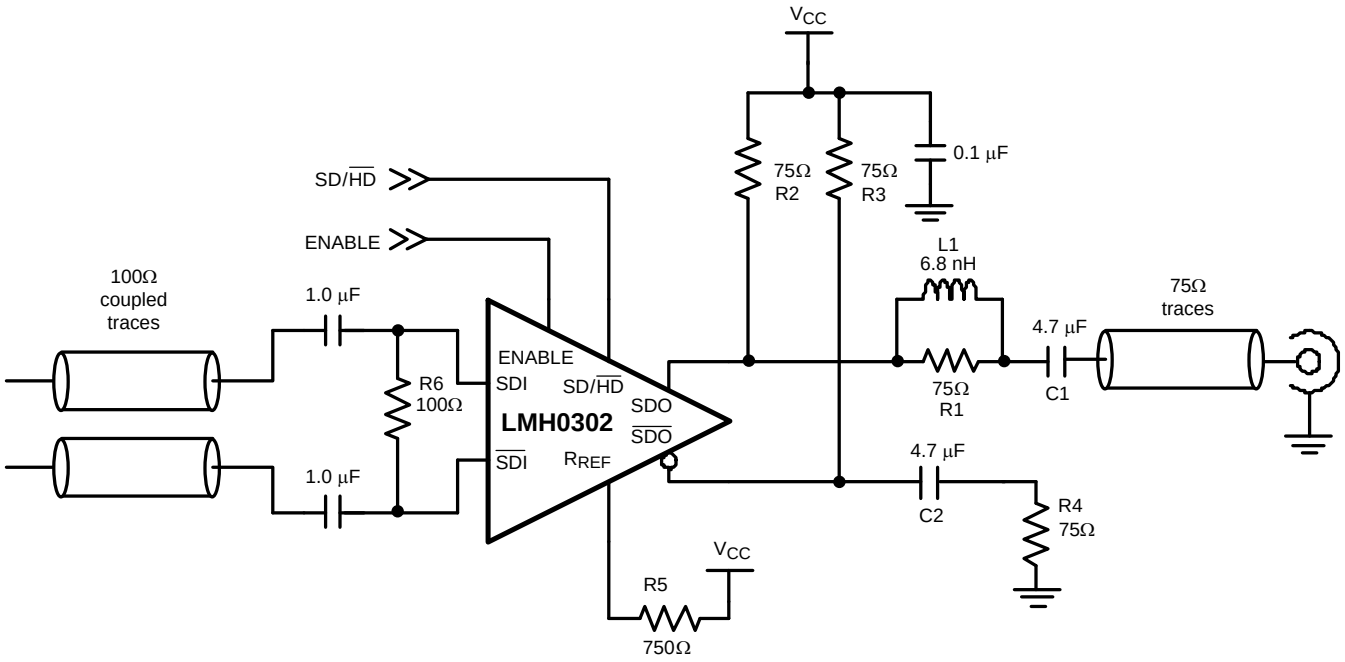

Figure 6. Schematic Diagram of the LMH0302 Cable Driver

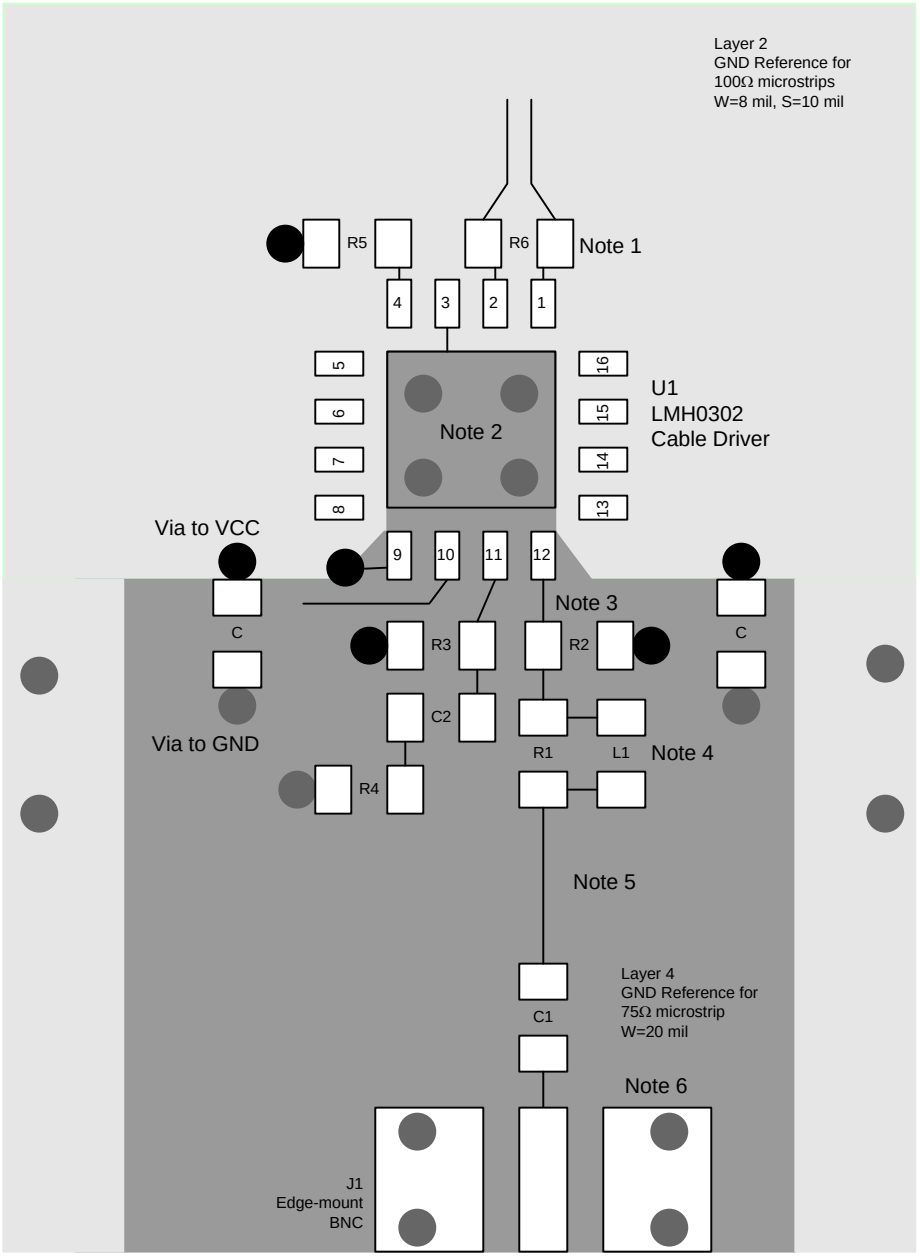

Figure 7. Layout Recommendations For The LMH0302 Cable Driver (Showing Signal Path And Power Hook-Up)

- Note 1 – R6 100Ω receive termination placed close to IC pins. R5 750Ω placed close to IC pin. Use coupled traces with 100Ω differential impedance reference to Layer 2.
- Note 2 – GND stitch for Layer 2 and Layer 4.
- Note 3 – R2, R3 75Ω driver terminations placed close to IC pins.
- Note 4 – L1, R1 impedance matching network placed close to SDO+ pin.
- Note 5 – Use 75Ω controlled impedance trace reference to Layer 4. Use 0402-size components. Use trace width 15-25mil to minimize impedance drop caused by larger component pads.
- Note 6 – Use 75Ω controlled impedance footprint for BNC.

7 Layout Example - LMH0384 Multi-Rate Adaptive Equalizer

Figure 8 shows the schematic diagram and Figure 9 shows a conceptual layout diagram of TI's LMH0384 3Gb/s/HD/SD SDI adaptive cable equalizer. The stack-up shown in Figure 2 is used in this example. Layer 2 is the ground reference for the 8-mil wide 100Ω differential trace that goes to the output pins SDO+ and SDO-. The far-end 100Ω termination resistor R4 is placed closest to the input pins of the receiving integrated circuit (not shown). An island of metal on layer 4 is used as the ground plane for the 75Ω traces. The two ground references are stitched together using the ground via for the device's DAP connection. The AC coupling capacitor C2 is placed closest to the input pin at SDI+. The impedance matching components L1 and R1 are placed as close as possible to the input pin SDI+ through C2. The 75Ω termination resistor R2 is placed after C2 to minimize the effect of the stub.

This design uses 0402-size components to minimize the impedance change to the 75Ω trace built with 20-mil microstrip referenced to layer 4. The footprint used for the BNC should have good signal launch in order to maintain good return loss.

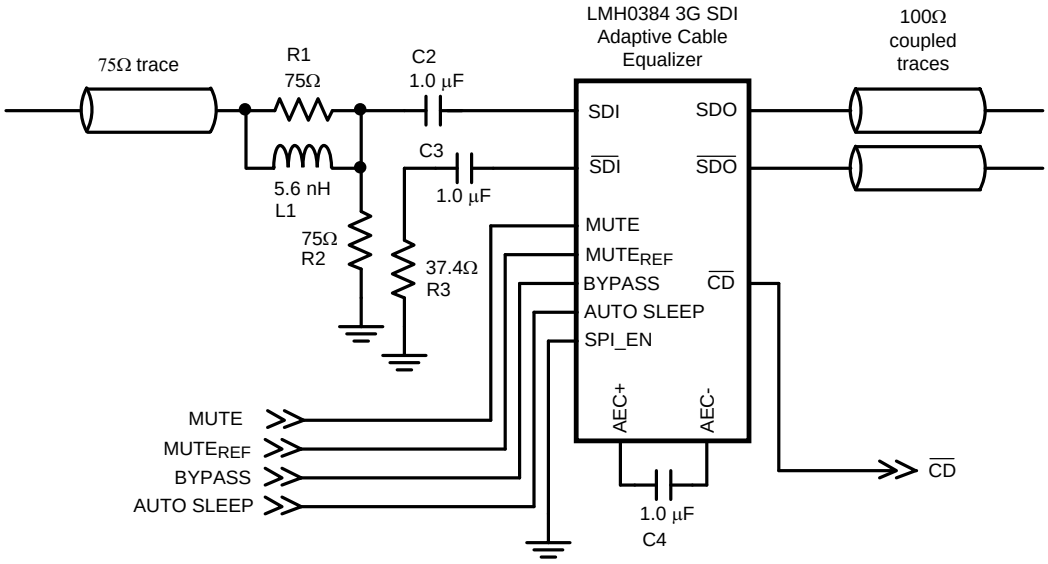

Figure 8. Schematic Diagram of the LMH0384 Adaptive Equalizer

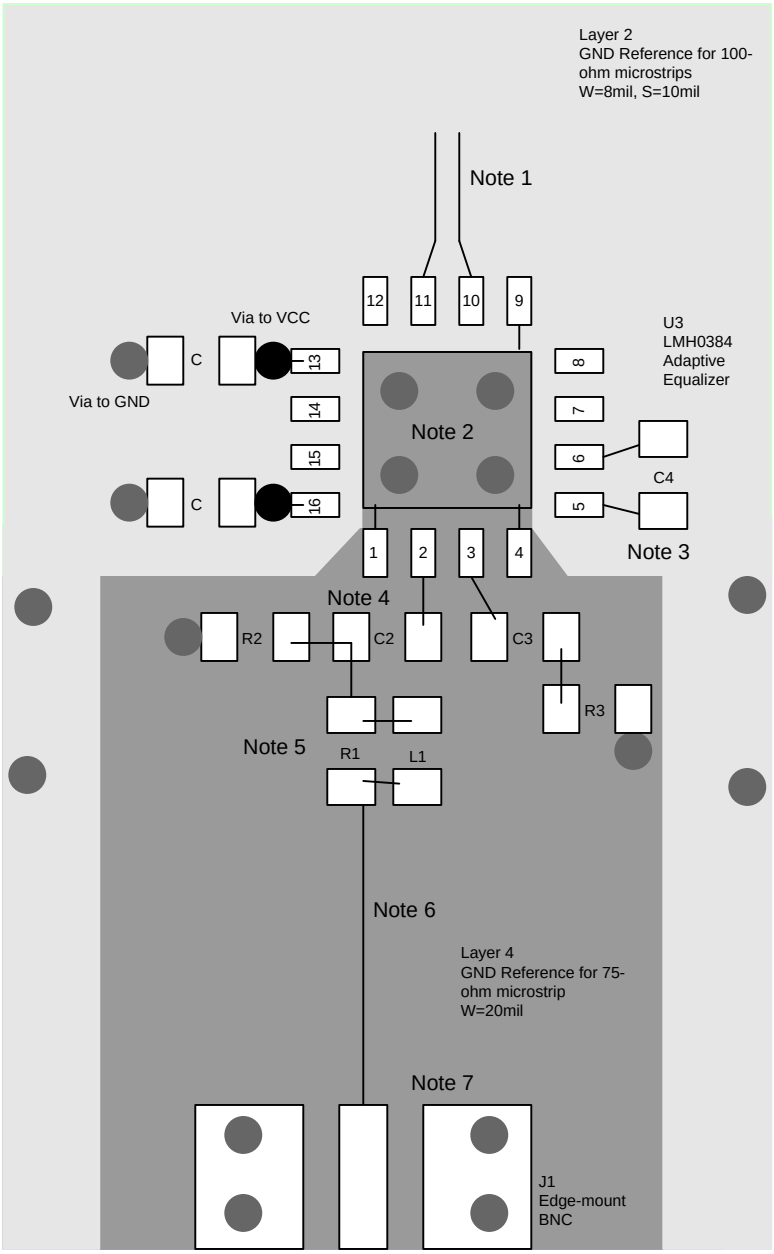

Figure 9. Layout Recommendations For The LMH0384 Adaptive Equalizer (Showing Signal Path And Power Hook-Up)

- Note 1 – Use coupled traces with 100Ω differential impedance reference to Layer 2.
- Note 2 – GND stitch for Layer 2 and Layer 4.
- Note 3 – C4 placed close to pins 5 and 6.
- Note 4 – C2 placed closest to IC input pin. R2 75Ω receive termination placed after C2.
- Note 5 – L1, R1 impedance matching network placed close to SDI+ pin through C2.
- Note 6 – Use 75Ω controlled impedance trace reference to Layer 4. Use 0402-size components. Use trace width 15-25mil to minimize impedance drop caused by larger component pads.
- Note 7 – Use 75Ω controlled impedance footprint for BNC.

8 Conclusion

The challenge in SDI board layout is in devising a layout strategy to minimize impedance mismatches from the many external components on the 75Ω SDI port. Use of 75Ω microstrip with wide trace width comparable to the landing pads of the passive components will achieve the goal of minimum impedance discontinuity. Use of a second ground reference allows the freedom to use finer trace widths for the 100Ω differential traces that route to high pin-count IC's. It is recommended to walk along the signal path, look for impedance change due to the change of layout structures, and devise a way to shave off the excess inductance or capacitance in order to maintain the target characteristic impedance. By following a few simple layout guidelines, it is possible to design a board to meet SDI return loss and keep high signal fidelity.

9 References

1. SMPTE standards are standards published by the Society of Motion Pictures and Television Engineers. Some of these standards are:
   - SMPTE 259M-2006: SDTV Digital Signal/Data – Serial Digital Interface
   - SMPTE 292M-1998: Bit Serial Digital Interface for High Definition Television Systems
   - SMPTE 424M-2006: 3Gb/s Signal/Data Serial Interface
2. *LMH0302 3Gbps HD/SD SDI Cable Driver* (SNLS247), *LMH0384 3 Gbps HD/SD SDI Extended Reach and Configurable Adaptive Cable Equalizer* (SNLS308), and other Texas Instruments SDI integrated circuits can be found at www.ti.com.
3. *Getting Signal Launch Right for High Speed Sub-systems* (SNLA186)

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