Application Report
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AN-1728 IEEE 1588 Precision Time Protocol Time Synchronization Performance

ABSTRACT

This application report presents specific time synchronization results from the precision PHYTER. Histograms and oscilloscope plots of these synchronization results are provided, showing the relationship between the slave clock and the master clock.

Contents

List of Figures

List of Tables

1 Introduction

The purpose of the IEEE 1588 Precision Time Protocol (PTP) is to synchronize the time between different nodes on an Ethernet network. Many applications in factory automation, test and measurement, and telecommunications require very close time synchronization. This requirement is often well beyond what can be provided by a standard software solution. The Precision PHYTER solution provides exceptionally tight time synchronization that meets these application needs and is easily added to existing products.

This application report is applicable to the following product: DP83640.

2 Background

Network Time Protocol (NTP) has been the traditional way to synchronization time over Ethernet networks. NTP allows time synchronization up to 100 milliseconds. The IEEE 1588 PTP is required to achieve tighter synchronization. In software PTP applications, single link synchronization in the range of 100 microseconds can be reached. As can be seen in Figure 1, hardware assistance is required to achieve time synchronization in the nanosecond region.

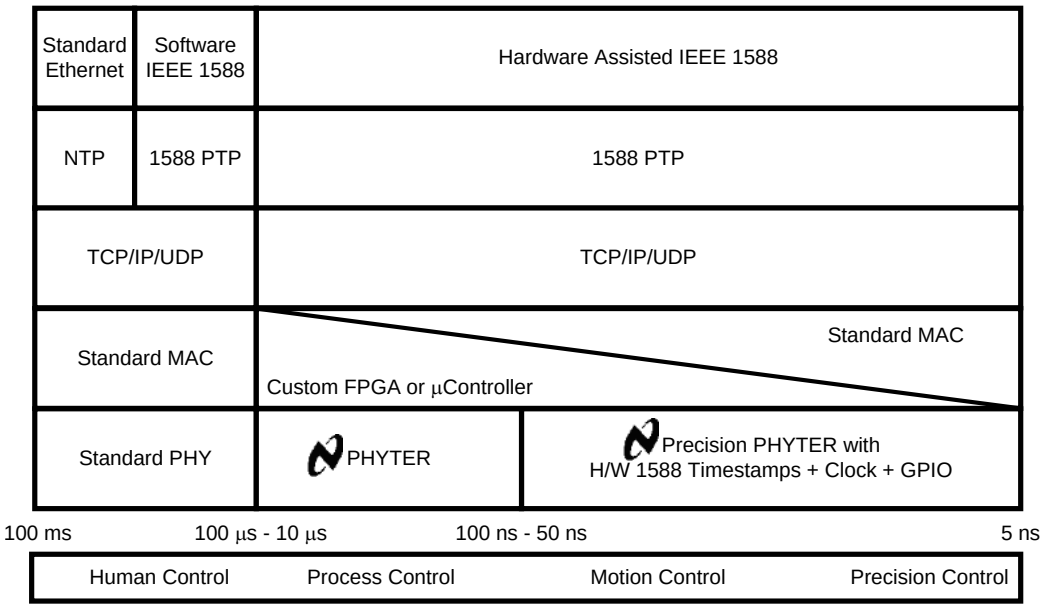

Figure 1. Implementation Choices to Achieve Better Time Synchronization

Every component that handles the PTP packets after they are received on the wire will increase the synchronization error. Software adds the most error since both processor load and the delay associated with handling interrupts impact how quickly a synchronization request is processed. Fortunately, only certain PTP actions are time critical. The most time critical PTP actions are recording timestamps of PTP packets, adjusting and maintaining the synchronized local clock, and using synchronized I/Os. By placing these components in the Ethernet PHY as shown in Figure 2, the DP83640 precision PHYTER accesses PTP packets as soon as they are available from the wire. Therefore, the precision PHYTER is the key component for reaching time synchronization of less than 10 nanoseconds. As an additional benefit, this solution can be added to an existing product design by simply replacing the Ethernet PHY and adding IEEE 1588 PTP software, avoiding the complications of moving to a new processor family or developing an ancillary FPGA.

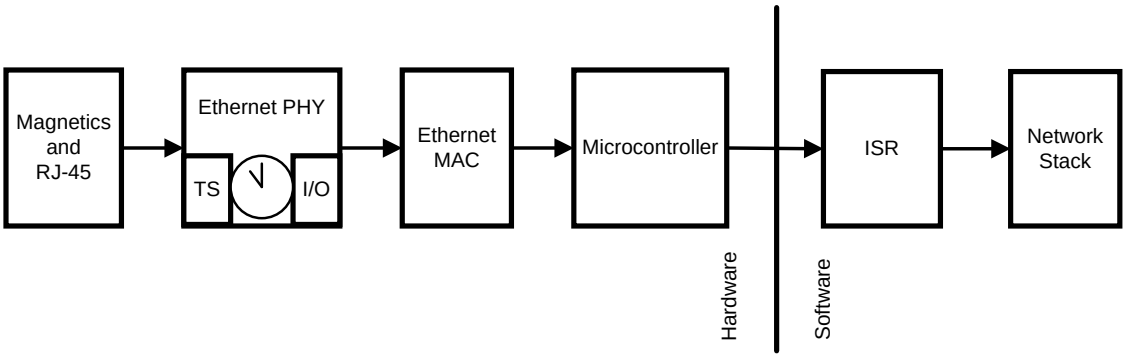

Figure 2. The Precision PHYTER IEEE 1588 Time Synchronization Advantage

3 Testing Time Synchronization Theory

It is difficult to assess the level of time synchronization that a system is capable of achieving because there is more than one way to test the quality of the time synchronization. Since each approach provides different information and has different considerations, this application report provides synchronization data taken under different test conditions. There are three approaches to testing time synchronization: software testing, pulse per second signal comparison, and output clock comparison.

Software testing relies on the results reported by the PTP stack to show the quality of the time synchronization. This means that the software results are subject to the same limitations as the PTP algorithm itself. The primary limitation of the PTP algorithm is that it cannot correct for differences in the length of the transmit path and the receive path. Another consideration when analyzing software results is that the reported error is always taken just before the time synchronization. Since the process is reporting an error that is essentially due to the drift between two clocks, the software error represents a worst case picture of the average time synchronization.

The most common way to analyze time synchronization comes from looking at the pulse per second (PPS) signal. Sending out a pulse at every second transition produces a PPS signal. For many older systems, the PPS signal is the only way to measure the success of time synchronization. The primary disadvantage to this measurement is that this effectively samples the error every second. Since there is not necessarily a correlation between the second transition and the clock synch update, it is difficult to achieve dependable results. Another issue with the PPS measurement is that the PPS signal is typically generated from a digital output that will add additional error to the synchronization results. That additional error will only impact digital inputs and outputs, but not the synchronized clock itself and, thus, should not be included in the synchronization measurement.

The most accurate method to measure clock synchronization is set both the master and slave to generate a clock output at a known frequency and then compare those two clock signals. This provides the error at many more times a second, providing a more accurate view of the time synchronization. As an additional benefit, the clock output can be handled through an analog output that will not add additional synchronization error.

4 Software Reported Synchronization Test Results

4.1 Software Reported Test Setup

The software test setup relies on an FPGA card that emulates an Ethernet MAC to allow the control software to interface with the Ethernet PHY hardware. The software connects to the MAC emulator through a USB connection. The PTP packets and PHY controls are created by the MACs and sent to the Ethernet PHYs. The software portion of the PTP protocol is handled by the computer while the hardware portion of the PTP protocol remains in the DP83640 on the PHY board. This setup is illustrated in Figure 3.

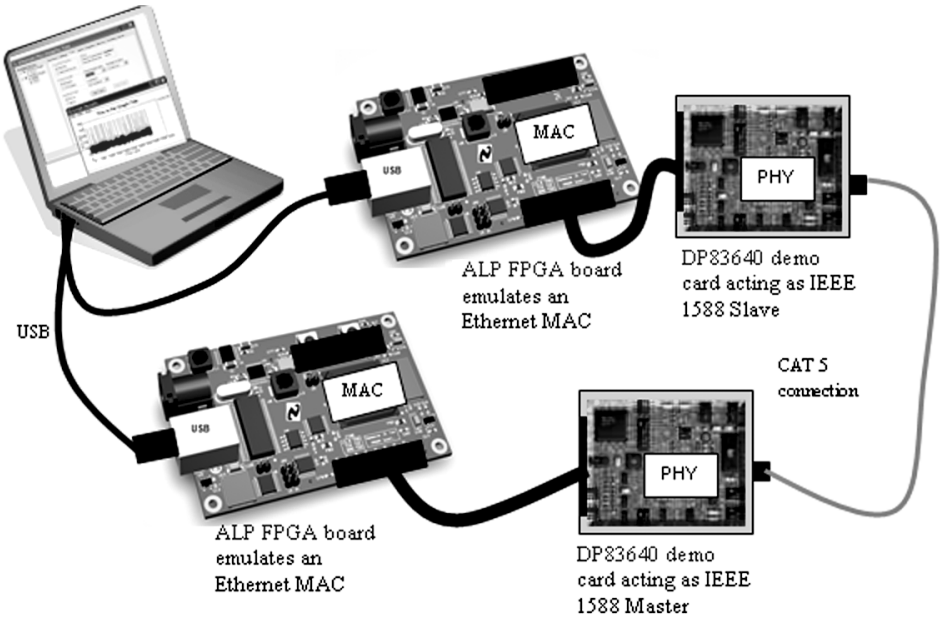

Figure 3. Software Synchronization Test Setup

4.2 Software Reported Test Conditions

Table 1 summarizes the conditions for the software test setup.

Table 1. Test Conditions

Operating Voltage	3.3 V
Temperature	25 °C
Reference Frequency Source	On-board 25 MHz crystal
IEEE 1588 PTP Synchronization Interval	1 second

4.3 Software Reported Test Results

Table 2. Synchronized to Master using IEEE 1588 PTP

	Mean	Standard Deviation	No of Samples
Software Reported Test Results	1.59 ns	6.5 ns	500 samples

Figure 4 represents a typical plot of the clock synchronization error, as reported by the software, between the master and slave nodes when they are time synchronized using the IEEE 1588 PTP protocol. The center line shows the average offset between the two clocks. The top and bottom lines graph the standard deviation around that average offset. The varying line shows the instantaneous offset that is calculated before each synchronization adjustment to the local slave clock. In Figure 4, the effects of the PTP synchronization algorithm can easily be seen in the stability and accuracy of the average offset and the tracking of the instantaneous offset per synchronization cycle.

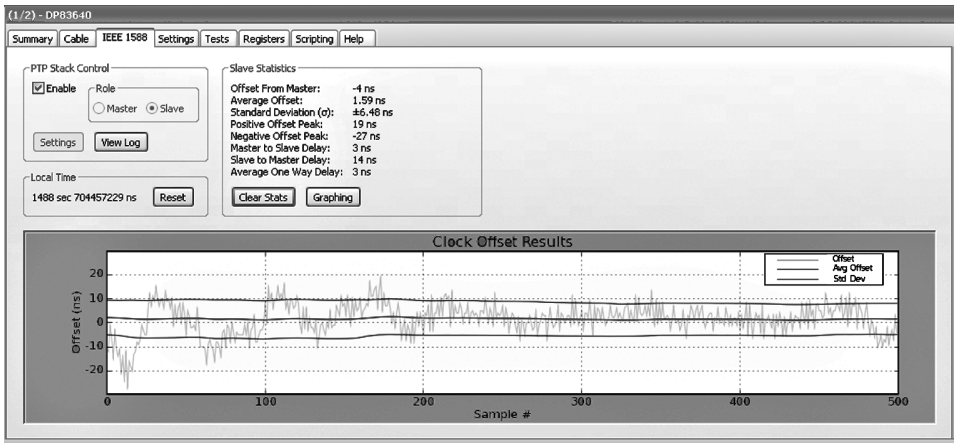

Figure 4. Synchronized to Master Using IEEE 1588 – Software Test Results

5 Pulse Per Second Synchronization Test Results

5.1 PPS Test Setup

Testing the PPS signal time synchronization was achieved by analyzing the PPS signals from both the master and slave devices with a Tektronix TDS784C oscilloscope. The test setup is represented in Figure 5.

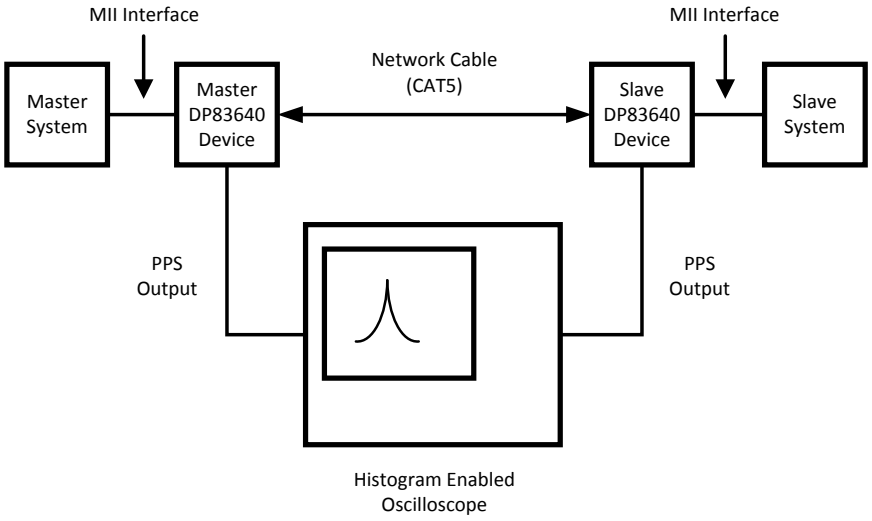

Figure 5. Pulse Per Second Output Synchronization Test Setup

5.2 PPS Test Conditions

Table 3 summarizes the conditions for the PPS test setup.

Table 3. Test Conditions

Operating Voltage	3.3 V
Temperature	25 °C
Reference Frequency Source	On-board 25 MHz crystal
IEEE 1588 PTP Synchronization Interval	1 second

5.3 PPS Test Results

Table 4. Synchronized to Master Using IEEE 1588 PTP

	Mean	Standard Deviation	No of Samples
PPS Synchronization	-869 ps	7.87 ns	1000 samples

Figure 6 represents a typical histogram plot of the PPS output signal comparison between the master and slave nodes when they are time synchronized using the IEEE 1588 PTP protocol. In Figure 6, the clock to clock synchronization is within a 7.9 nanosecond standard deviation and a mean difference of only –869 picoseconds. This performance represents a significant advantage over other commercially available time synchronization components.

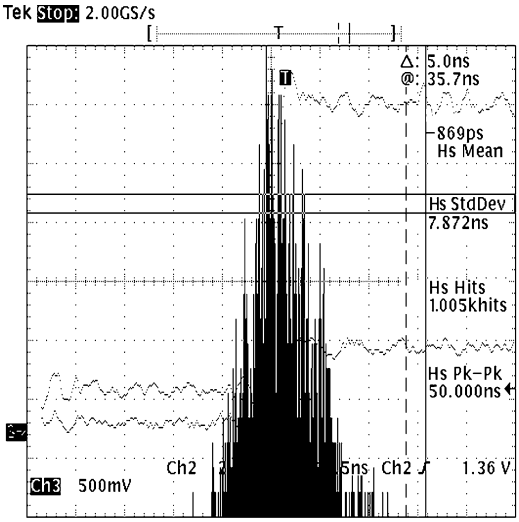

Figure 6. Synchronized to Master Using IEEE 1588 – PPS Jitter Histogram

6 Clock Synchronization Test Results

6.1 Clock Test Setup

Testing the PPS signal time synchronization was achieved by analyzing the clock output signals from both the master and slave devices with a Tektronix TDS784C oscilloscope. Both devices were set to output a 10 MHz clock signal for testing purposes. The test setup is represented in Figure 7.

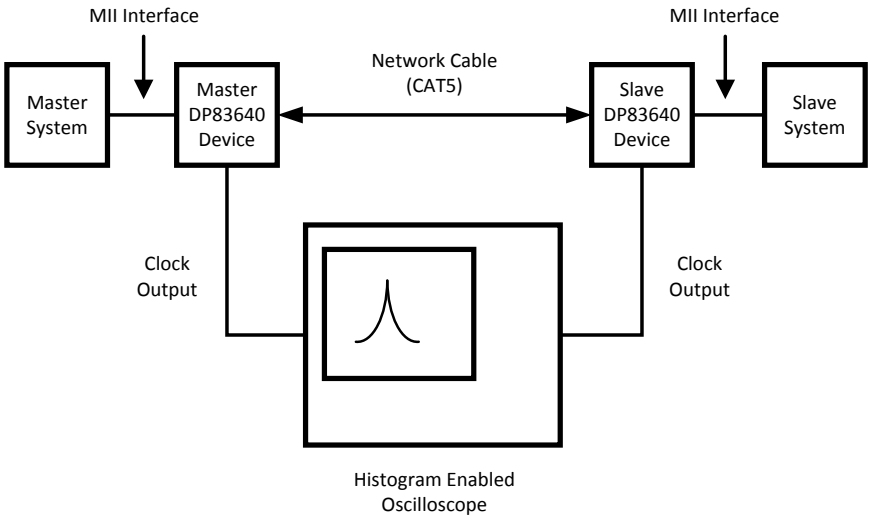

Figure 7. Clock Output Synchronization Test Setup

6.2 Clock Test Conditions

Table 5 summarizes the conditions for the clock synchronization test setup.

Table 5. Test Conditions

Operating Voltage	3.3 V
Temperature	25 °C
Reference Frequency Source	On-board 25 MHz crystal
Clock Output Frequency	10 MHz
IEEE 1588 PTP Synchronization Interval	1 second

6.3 Clock Test Results

Table 6. Synchronized to Master using IEEE 1588 PTP

	Mean	1-σ Standard Deviation	No of Samples
PPS Synchronization	-226 ps	2.655 ns	1100 samples

Figure 8 represents a typical histogram plot of the time difference between the clock output signals of the master and slave nodes when they are time synchronized using the IEEE 1588 PTP protocol. In Figure 8, the clock to clock synchronization is within a 2.7 nanosecond standard deviation and a mean difference of only –226 picoseconds. This level of synchronization can easily support even very demanding applications.

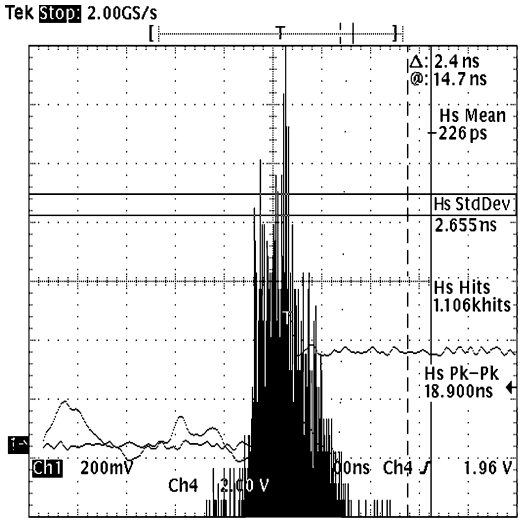

Figure 8. Synchronized to Master Using IEEE 1588 - Clock Output Jitter Histogram

Another way to see the relationship between the master and slave clock outputs is to look at the two clock outputs over time. The following scope plot taken from the same test setup shows this relationship. The oscilloscope is set to infinite persistence, showing the peak to peak jitter of the slave signal. The master clock output is shown on the top and the slave clock output is shown on the bottom. As can be seen from Figure 9, the two clocks are both phase and frequency aligned. The peak to peak synchronization jitter can be seen as the 11 ns delta measurement in the upper right hand corner. This scope capture shows how remarkably stable and time synchronized two clocks can be with IEEE 1588 PTP and the precision PHYTER solution.

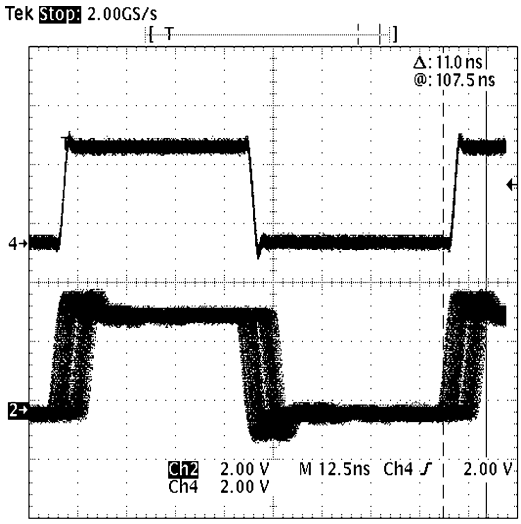

Figure 9. Synchronized to Master Using IEEE 1588 - Clock Output Signals

7 Summary

There are many applications for time synchronized Ethernet that require closer synchronization than what can be achieved with software only implementations of time synchronization protocols. National Semiconductor's DP83640 precision PHYTER provides an easy to implement method for adding high precision time synchronization to Ethernet applications. The provided test results clearly show that the precision PHYTER solution provides very precise and accurate time synchronization of less than 10

nanoseconds standard deviation over a single link. This precision allows a hardware developer to develop a very capable, Ethernet-based solution for any application with strict time synchronization requirements. The results from software analysis, PPS signal analysis, and synchronized clock output analysis provide a very good representation of the capabilities of the DP83640 device to support application development and system design.

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