Application Report
SNLA085A–August 2006–Revised April 2013

AN-1508 DP83849 Cable Diagnostics

ABSTRACT

This application report describes the features incorporated in the DP83849 for detecting cabling faults and monitoring link status in a Twisted Pair cabling environment.

Contents

List of Figures

List of Tables

1 Introduction

In today's increasingly complex network installations, detection of link and cabling problems can be a significant issue, affecting network performance and requiring significant time and effort to find and correct problems. The DP83849 Dual Ethernet Transceiver implements a suite of features that provide extensive link and cable diagnostic features without the need for additional hardware. These features allow for significant in-system diagnostic capabilities, and even allow for the ability to detect or predict potential cabling issues prior to catastrophic failure.

Product Applicability:

DP83849C

DP83849I

DP83849ID

DP83849IF

1.1 Categories of Link Diagnostics

For the purposes of this application report, the types of link diagnostics are divided into three areas:

- Linked Cable Status - Provides current status for a valid link over Twisted Pair cabling
- Link Quality Monitor - Provides a mechanism to detect and warn the system of changing or deteriorating link conditions
- TDR (Time Domain Reflectometry) Cable Diagnostics - Provides a mechanism for analyzing attached cabling to determine common cable faults and to detect cable length or distance to a fault.

2 Linked Cable Status

In an active connection with a valid link status, the following diagnostic capabilities are available in the DP83849:

- Polarity reversal detection
- Cable swap (MDI vs. MDIX) detection
- Frequency offset relative to link partner
- 100Mb Cable Length Estimation
- Cable Signal Quality Estimation

2.1 Polarity Reversal

The DP83849 detects polarity reversal if it observes negative link pulses. Reverse polarity indicates the positive and negative conductors in the receive pair are swapped. Since polarity is corrected by the receiver, this does not necessarily indicate a functional problem in the cable. The Polarity indication is available in bit 12 of the PHYSTS register (or bit 4 of the 10BTSCR register).

Since the polarity indication is dependent on link pulses from the link partner, polarity indication is valid in all 10Mb modes of operation. Polarity reversal indication is not applicable in 100Mb modes of operation. Since the polarity of the receive pair does not affect 100Mb operation, no correction is necessary.

2.2 Cable Swap Indication

As part of Auto-Negotiation, the DP83849 has the ability (using Auto-MDIX) to automatically detect a cable with swapped MDI pairs and select the appropriate pairs for transmitting and receiving data. Normal operation is termed MDI, while crossed operation is MDIX. The MDIX status can be read from bit 14 of the PHYSTS register. Since the cable swap is corrected by the receiver, it does not indicate a functional problem in the cable. In addition, if both partners connected to the cable are Auto-MDIX capable, both could resolve to an MDI-X condition, even if the cable pairs are not swapped.

2.3 Frequency Offset Relative to Link Partner

As part of the 100Mb clock recovery process, the DSP implementation provides a frequency control parameter. This value may be used to indicate the frequency offset of the device relative to the link partner. This operation is only available in 100Mb operation with a valid link status. The frequency offset can be determined using the FREQ100 register. Two different versions of the Frequency Offset may be monitored. The first is the long-term Frequency Offset between the link partner's transmit clock and DUT's recovered clock. The frequency offset remains fairly stable in a valid linked state. The second is the current Frequency Control value, which includes short-term phase adjustments and the frequency offset value. Frequency control value can provide information on the amount of jitter in the system.

Figure 1 provides an example comparing the distribution of Frequency Offset and Frequency Control values over a long period of time. The Frequency Offset value has much less variation than the Frequency Control value.

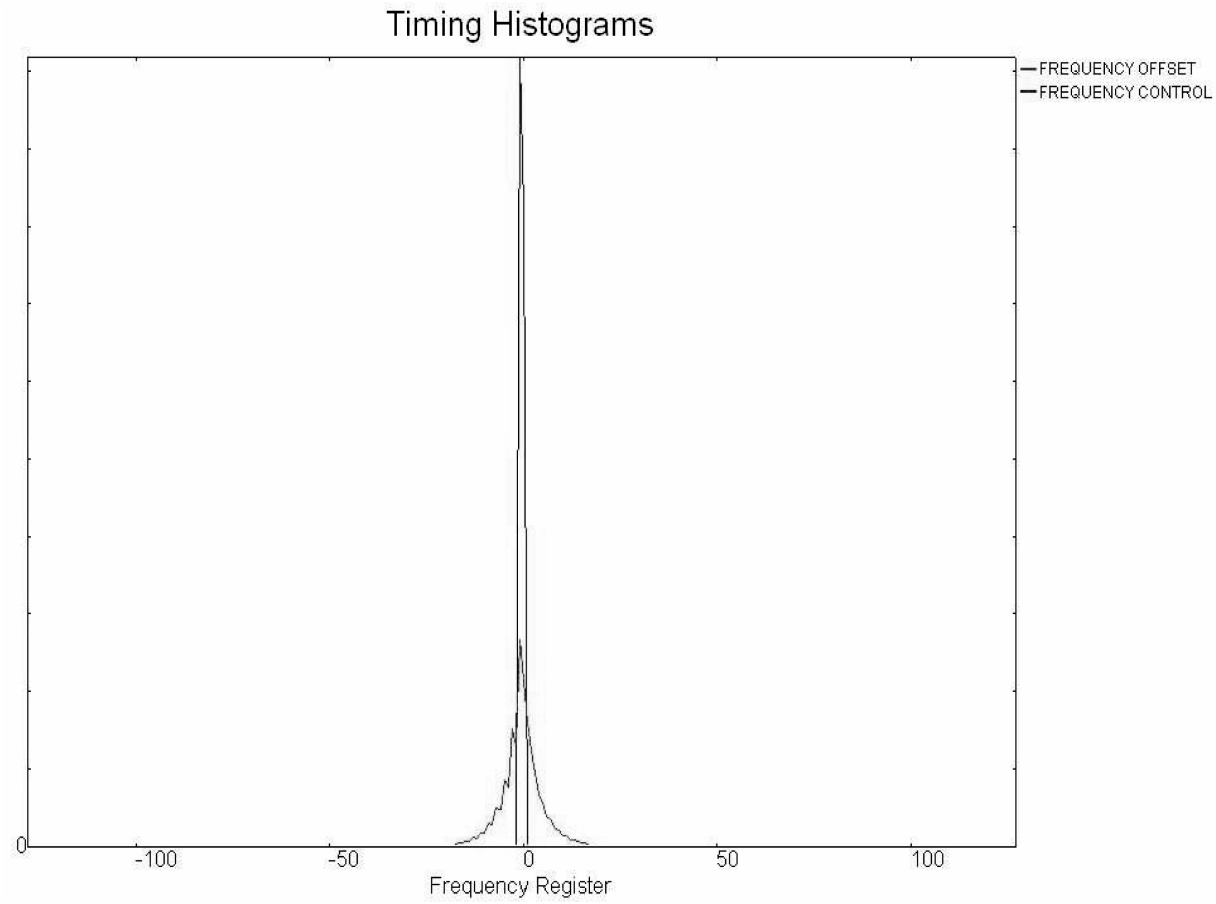

Figure 1. Frequency Control/Offset Histograms

2.4 100MB Electrical Cable Length

The DP83849 provides a method of computing cable length based on electrical characteristics of the 100Mb Link. This essentially provides an equivalent cable length rather than a measurement of the physical cable length. The electrical cable length estimation is only available in 100Mb mode of operation with a valid Link status. The cable length estimation is reported in meters and is available in the LEN100_DET register.

100MB cable length is a linear function of the Analog (AEQ) and Digital (DEQ) equalization coefficient values in the linked state.

if (AEQ == 0) Length = (A_1 × DEQ) + B_1

if (AEQ == 1) Length = (A_2 × DEQ) + B_2

and so on ...

The algorithm for computing the electrical cable length is depicted above. The constants {A1, A2, ... } & {B1, B2, ... } are determined by statistical study of various typical case cables. The computation is completely handled in hardware. The resultant cable length is available using a simple register read.

Electrical cable length readings can vary slightly depending on the cabling, noise, jitter, and so on. Table 1 shows the observed range in typical cables. TDR measurements using DP83849 (described in Section 4) are also shown.

Table 1. Electrical/TDR Cable Length Reading (Typical Cables)

Physical Cable Length (m)	Electrical Cable Length (m)		TDR Measurements (m)	
	Min	Max	TX Pair	RX Pair
1	1	2	1.08	1.08
10	9	10	10.37	10.8
20	19	22	19.87	19.87
30	28	32	31.32	32.18
50	48	51	52.49	53.57
100	105	110	101.09	100.01
130	133	139	129.82	133.92

While not as accurate as TDR based measurements, DP83849's electrical cable length measurements are relatively consistent for typical CAT5 cables, usually within +/- 10m. Based on additional statistical studies, software could be used to convert the reported cable length to match cabling with different characteristics than typical Cat5 cables.

2.5 Cable Signal Quality Estimation - Signal to Noise Ratio (SNR)

The Cable Signal Quality Estimator accounts for the error in the signal recovery algorithm of the DSP and can be used to generate an approximate Signal-to-Noise Ratio/Bit Error Rate for the 100Mb receiver. 100Base-T uses 3-level MLT3 signaling. Scrambled Data (on an average) would comprise of 25% '-1', 50% '0' and 25% '1'. An example of the DSP Receiver histogram in the linked state is shown in Figure 2.

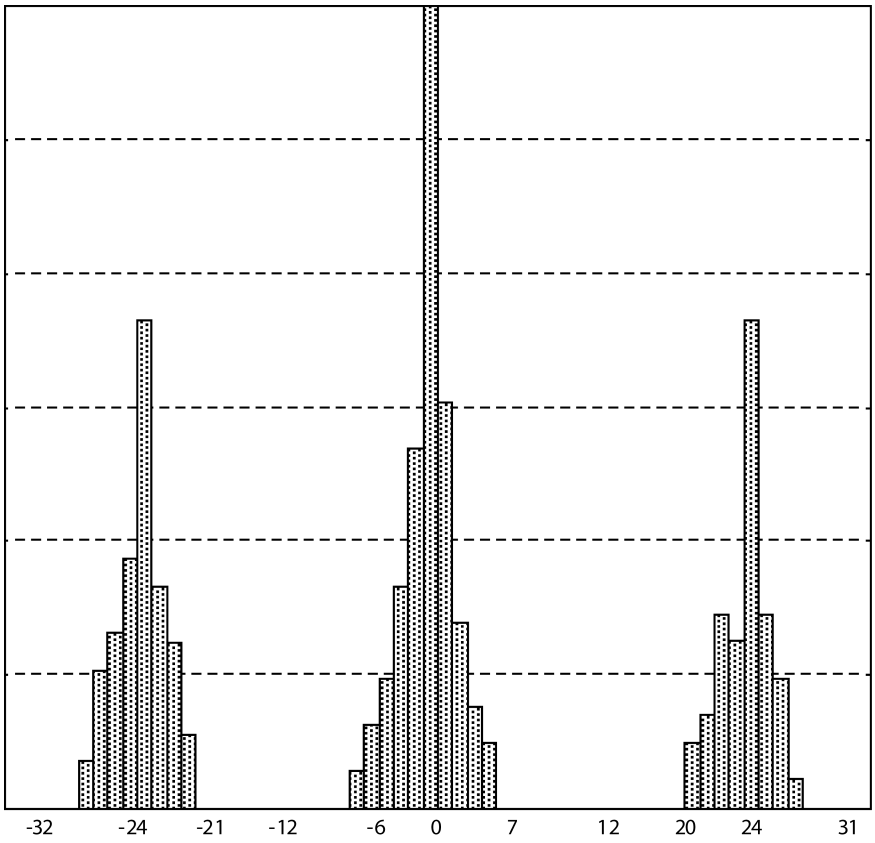

Figure 2. Example Receiver Histogram for Variance calculation

Each data output of the DSP Receiver, sampled every 8ns, includes a data value and an error value relative to the ideal value. The SNR estimation algorithm computes the statistical variance associated with the three data {-1, 0, 1} values over a long period of time (Var_Timer) which is programmable to take a value from the set of {2, 4, 6, 8} ms. The three variance values combine to give the effective variance of the received data. This variance sum is used to compute the SNR by software using the following equation:

$$SNR(dB) = 10\log_{10}((288 \times Symbol\_Count) / Variance) \quad (1)$$

where *Symbol_Count* is the number of data symbols captured during the measurement time:

$$Symbol\_Count = (Var\_Timer\ (ms) \times 2^{17} symbols/ms) \quad (2)$$

The *Var_Timer* can be set using the Variance Control Register (VAR_CTRL). The variance sum is available to software through the Variance Data registers (VAR_DATA). The Variance sum is continuously computed by asserting Var_Enable, such that a new value will be available every {2, 4, 6, 8}ms, depending on the setting of the Var_Timer. Software can poll this process regularly to track the signal quality over time.

Variance Computation can be disabled by deasserting Var_Enable.

Table 2 provides example SNR estimation values for different lengths of typical Cat5 cabling.

Table 2. Signal to Noise Ratio (SNR) for Typical Cable

Physical Cable Length (m)	Observed SNR Range (dB)	Approx. Bit Error Rate
1	27 - 28	10^{-18}
10	26 - 27	10^{-17}
25	25 - 27	10^{-16}
50	24 - 26	10^{-15}
75	23 - 25	10^{-14}
100	22 - 23	10^{-13}
125	21 - 22	10^{-12}

3 Link Quality Monitor

The Link Quality Monitor allows a method to generate an alarm when the DSP adaption resolves to a set of values outside the normal and expected range. This could occur due to changes in the received signal which could indicate a potential problem with cabling, connectors or terminations. Software can program thresholds for the following DSP parameters to be used to interrupt the system:

- Digital Equalizer Post-Cursor Coefficient (DEQ C1)
- Digital Adaptive Gain Control (DAGC)
- Digital Base-Line Wander Control (DBLW)
- Recovered Clock Long-Term Frequency Offset (FREQ)
- Recovered Clock Frequency Control (FC)

Software is expected to read initial adapted values and then program the thresholds based on an expected valid range. This mechanism takes advantage of the fact that the DSP adaption should remain in a relatively small range once a valid link has been established. In this way the system can be tuned to be sensitive or tolerant to parameter changes as desired.

3.1 Link Quality Monitor Control and Status

Link Quality Monitor is controlled through the Link Quality Monitor Register (LQMR) and the Link Quality Data Register (LQDR). The LQMR register includes a global enable to enable the Link Quality Monitor function. In addition, it provides warning status from both high and low thresholds for each of the monitored parameters. Note that individual low or high parameter threshold comparisons can be disabled by setting to the minimum or maximum values.

To allow the Link Quality Monitor to interrupt the system, the Interrupt must be enabled through the interrupt control registers, MICR and MISR.

The Link Quality Monitor may also be used to automatically reset the DSP and restart adaption. Separate enable bits in the LQMR allow for automatic reset based on each of the five parameter values. If enabled, a violation of one of the thresholds will result in a reset of the current link status. In an Auto-Negotiated mode, this will restart Auto-Negotiation. In a forced 100Mb mode, this will force a restart of the DSP adaption process.

3.2 Checking Current Parameter Values

It is recommended that prior to setting threshold values, software check current adapted values. The thresholds may then be set relative to the adapted values. The current adapted values can be read using the LQDR register by setting the Sample_Param bit.

For example, to read the DBLW current value:

1. Write 2400h to LQDR to set the Sample_Param bit and set the LQ_Param_Sel[2:0] to 010.
2. Read LQDR. Current DBLW value is returned in the low 8 bits.

3.3 Threshold Control

The LQDR register also provides a method of programming high and low thresholds for each of the four parameters that can be monitored. The register implements an indirect read/write mechanism. Writes are accomplished by writing data, address, and a write strobe to the register. Reads are accomplished by writing the address to the register, and reading back the value of the selected threshold. Setting thresholds to the maximum or minimum values will disable the threshold comparison since values have to exceed the threshold to generate a warning condition. Warnings are not generated if the parameter is equal to the threshold. By default, all thresholds are disabled by setting to the min or max values. Table 3 shows the four parameters and range of values.

Note that values are signed 2s-complement values except for DAGC, which is always positive. For example, to set the DBLW Low threshold to -38:

1. Write 14DAh to LQDR to set the Write_LQ_Thr bit, select the DBLW Low Threshold, and write data of -38 (0xDA).
2. Write 8000 to LQMR to enable the Link Quality Monitor (if not already enabled)

Table 3. Link Quality Monitor Allowed Parameter Ranges

Parameter	Minimum Value	Maximum Value	Min (2-s comp)	Max (2-s comp)
DEQ C1	-128	+127	0x80	0x7F
DAGC	0	+255	0x00	0xFF
DBLW	-128	+127	0x80	0x7F
Freq Offset	-128	+127	0x80	0x7F
Freq Control	-128	+127	0x80	0x7F

3.4 Link Quality Monitor Implementation

Most parameters should be set based on the baseline value. Once link is established, the baseline values may be read as described previously in Section 3.2. These values can be used to set the expected threshold values. Each parameter will have a different expected range. This section provides some guidelines which can be used to determine appropriate settings.

DEQ C1 and DAGC adaptation heavily depend on linked cable length. Once link is established, the DEQ C1 and DAGC values will remain within a relatively small range of values.

DBLW variation depends on packet data being received. A baseline value is not significant, so the DBLW value should be programmed as a +/- range from zero.

Frequency offset should exhibit a relatively tight range for +/-50ppm variation in system clock frequencies. Since the frequency is in steps of approximately 5.1562ppm, the values of +/- 20 for Freq Offset allow for just over 100ppm in link partner plus receiver frequency offset. Tighter threshold values could be set, using the baseline value, in order to detect drift in frequency offset. This may be especially useful for real-time systems that may need to detect changes in the base frequencies.

Since Frequency Control varies relative to the Frequency Offset, it should be programmed as a range from the Frequency Offset. The range is dependent on the expected variation and amount of noise or jitter tolerance desired.

An example of recommended guard-band ranges are shown in Table 4. Some level of system evaluation should be done to select and validate threshold settings appropriate for expected operating conditions.

Table 4. Link Quality Monitor Example Parameter Ranges

Parameter	Baseline Value	Recommended Range	
DEQ C1	c1	c1 - 10	c1 + 10
DAGC	dagc	dagc -15	dagc + 15
DBLW	none	-40	40
Freq Offset	none or Freq Offset	-20 or Freq Offset - 10	20 or Freq Offset + 10
Freq Control	Freq Offset	Freq Offset - 30	Freq Offset + 30

4 TDR Cable Diagnostics

The PHYTER Dual implements a Time Domain Reflectometry (TDR) method of cable length measurement and evaluation which can be used to evaluate a connected twisted pair cable. The TDR implementation involves sending a pulse out on either the Transmit or Receive conductor pair and observing the results on either pair. By observing the types and strength of reflections on each pair, software can determine the following:

- Cable short
- Cable open
- Distance to fault
- Identify which pair (TX/RX) has a fault
- Pair skew

The TDR cable diagnostics works best in certain conditions. For example, an unterminated or open cable provides a good reflection for measuring cable length, while a cable with an ideal termination at an unpowered partner may provide no reflection at all.

The TDR cable diagnostics only works for twisted pair (copper) connections and is not supported over Fiber connections.

4.1 TDR Pulse Generator

The TDR implementation can send two types of TDR pulses. The first option is to send 50ns or 100ns wide link pulses from the 10Mb Common Driver. The second option is to send pulses from the 100Mb Common Driver in 8ns increments up to 56ns in width. The 100Mb pulses will alternate between positive and negative pulses. The shorter pulses provide better ability to measure short cable lengths, especially since they will limit overlap between the transmitted pulse and a reflected pulse. The longer pulses provide better measurements of long cable lengths.

In addition, if the pulse width is programmed to 0, no pulse will be sent, but the monitor circuit will still be activated. This allows sampling of background data to provide a baseline for analysis. It may also be used to verify that no partner is active on the link.

4.2 TDR Pulse Monitor

The TDR function monitors data from the Analog to Digital Converter (ADC) to detect both peak values and values above a programmable threshold. It can be programmed to detect maximum or minimum values. In addition, it records the time, in 8ns intervals, at which the peak or threshold value first occurs.

The TDR monitor implements a timer that starts when the pulse is transmitted. A window may be enabled to qualify incoming data to look for response only in a desired range. This is especially useful for eliminating the transmitted pulse, but also may be used to look for multiple reflections.

4.3 Shaping of Received Pulse

Software may wish to use the Gain and Equalization functions in the receiver to shape the incoming signal to improve signal response. The Test controls in the DSP allow for loading and freezing values for the Analog Gain Control (AAGC) and Analog Equalizer (AEQ). For example, setting the AAGC to a lower value could be used to reduce the incoming signal to prevent clipping on the ADC outputs. This allows a more accurate determination of the peak time.

Software may also program the device to use the DSP data and therefore the Equalization and Gain controls in the DSP. Note that using the DSP introduces an additional 6 clock delay as reported in the time measurements.

4.4 TDR Control Interface

The TDR Control interface is implemented in the register block (TDR_CTRL and TDR_WIN registers) and implements the basic controls in Table 5.

Table 5. TDR Control Interface

TDR Register Controls	Description
TDR Enable	Enables the TDR function. This bypasses normal operation and gives control of the 10Mb and 100Mb Transmitters to the TDR function.
TDR Send Pulse	Sends the TDR pulse and starts the TDR Monitor. Transmit Mode Enables use of 10Mb Link pulses from the 10Mb Common Driver or data pulses from the 100Mb Common Driver
Transmit Pulse Width	Allows sending of 0 to 7 clock width pulses. Actual pulses are dependent on the transmit mode. If Pulse Width is set to 0, then no pulse will be sent.
Transmit Channel Select	The transmitter can send pulses down either the transmit pair or the receive pair. Default value is to select the transmit pair.
Min/Max Mode Select	Controls TDR Monitor operation. In default mode, the monitor will detect maximum (positive) values. In Min mode, the monitor will detect minimum (negative) values.
Receive Data Select	Selects between ADC data and DSP processed data. The DSP processed data incurs an additional 6 clock delay for the DSP datapath.
Receive Channel Select	The receiver can monitor either the transmit pair or the receive pair. Default value is to select the transmit pair.
Receive Window	The receiver can monitor receive data within a programmable window. The window is controlled by two register values. The Start window indicates the first clock to start sampling. The Stop window indicates the last clock to sample. By default, the full window is enabled, with Start set to 0 and Stop set to 255. The window range is in 8ns clock increments, so the maximum window size is 2048ns.

4.5 TDR Monitor Results

The TDR function monitors data from the Analog to Digital Converter (ADC) to detect both peak values and values above a programmable threshold. It can be programmed to detect maximum or minimum values. In addition, it records the time, in 8ns intervals, at which the peak or threshold value first occurs. The results of a TDR peak and threshold measurement are available in the TDR_PEAK and TDR_THR registers respectively. The threshold measurement may be a more accurate method of measuring the length for longer cables by providing a better indication of the start of the received pulse, rather than the peak value.

4.5.1 Length Detection or Distance to Fault

The cable length or the distance to a cabling fault can be determined from the time to the reflected pulse. Since the reflected pulse has traveled down the cable and back, the actual length is 1/2 of the distance traveled by the signal. The length is dependent on the NVP or Nominal Velocity of Propagation for the cable in use. The NVP is often expressed as a percentage of the speed of light, for example .72c (where, $c = 3 \times 10_8$m/s). For an NVP of .72c, the distance may be computed from the delay using the following formula:

$$\text{Length} = \text{Delay(s)} \times (.72c) / 2 = \text{Delay(ns)} \times 0.72 \times 0.15 \quad (3)$$

or as a function of the TDR_PEAK time measurement:

$$\text{Length} = \text{TDR\_Peak\_Time} \times 8\text{ns} \times 0.72 \times 0.15 = \text{TDR\_Peak\_Time} \times 1.2 \times 0.72 \quad (4)$$

These equations can be easily modified to support a different velocity of propagation.

4.6 Examples of Cable Connections

The following are examples of some typical cable connections or faults, and the resulting waveforms.

4.6.1 Open Circuit

An open circuit (Figure 3) is a relatively easy measurement. Open circuit response provides a strong positive reflection. No response should be seen on the opposite pair. An unterminated cable will exhibit an open circuit response off of both the transmit and receive pairs.

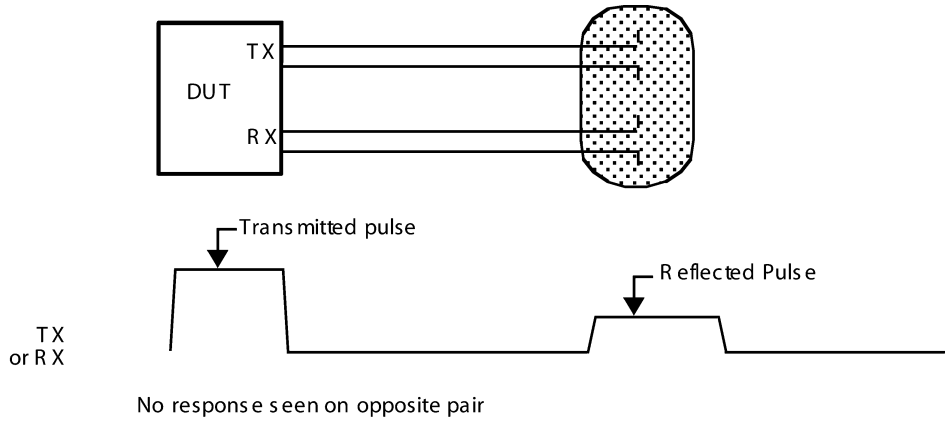

Figure 3. Open Circuit

4.6.2 Short Circuit Within a Single Pair

A short circuit within a single pair (Figure 4), that is, TX+ shorted to TX-, results in an easily identifiable response. The response is a returned signal which is the inverse of the transmitted pulse. No response should be seen on the opposite pair. This type of wiring problem should be detectable whether the cable is unterminated or terminated at an inactive partner.

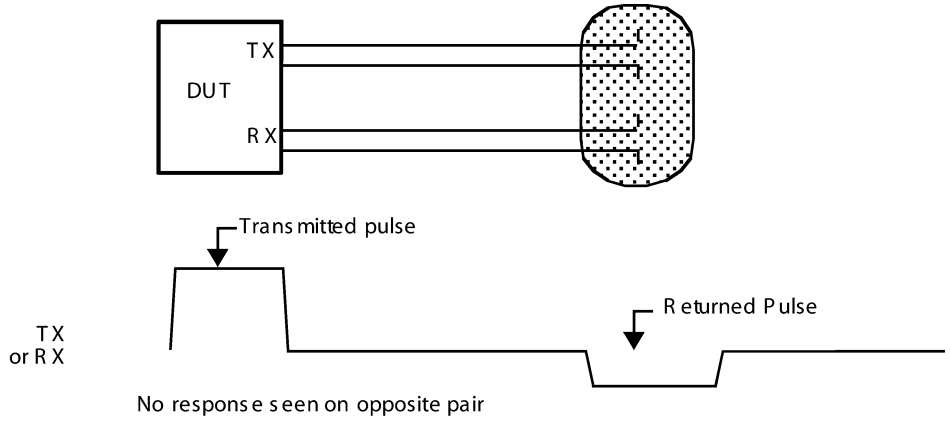

Figure 4. Short Circuit Within a Single Pair

A short circuit between conductors in opposite pairs is not as identifiable, although the response definitely is identifiable as a wiring problem. The response may include multiple responses/reflections, but definitely includes a returned pulse on the opposite pair. Due to crosstalk between conductors, the original pulse and returned pulse can induce additional response pulses. In addition, whether the cable is unterminated or terminated at a partner could also affect the types of responses seen. The measurement of a significant return on the receive pair is enough to diagnose a wiring problem, which is the main concern.

4.6.3 Termination at Inactive or Unpowered Partner

A good termination to an inactive or unpowered partner (Figure 5) should result in a very minimal returned signal, especially at long cable lengths. If the termination is close to ideal, the response may be undetectable. If the termination is not very ideal, the some reflection will be detectable, although it should still be smaller than the response from an open or short circuit. Dependent on the termination and whether the partner is powered or not, there may also be a small response on the opposite pair. For short cable lengths, the response may be large enough to make cable length measurements.

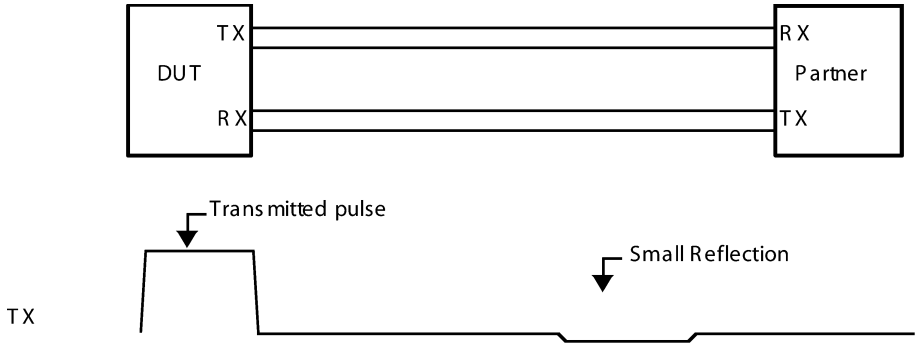

Figure 5. Termination at Inactive Partner

4.6.4 Cross-Wired Circuits

A cross-wired circuit (Figure 6 and Figure 7) can occur if a connector is wired incorrectly or a cable is spliced incorrectly. The basic result of the mis-wiring is a returned pulse on the opposite pair. In addition, the location of the mis-wiring within the cable can result in significant crosstalk, causing additional responses. It is difficult to identify the exact wiring condition, but the return on the receive pair is enough to diagnose a wiring problem.

This type of wiring failure is best detected if the cable is terminated at an inactive partner. The response may look like the basic unterminated case if the cross-wiring is done at the far-end connector. If the cross-wiring is at the near end connector, then significant cross-talk may occur (especially for long cables), and still allow for detection of a cabling problem.

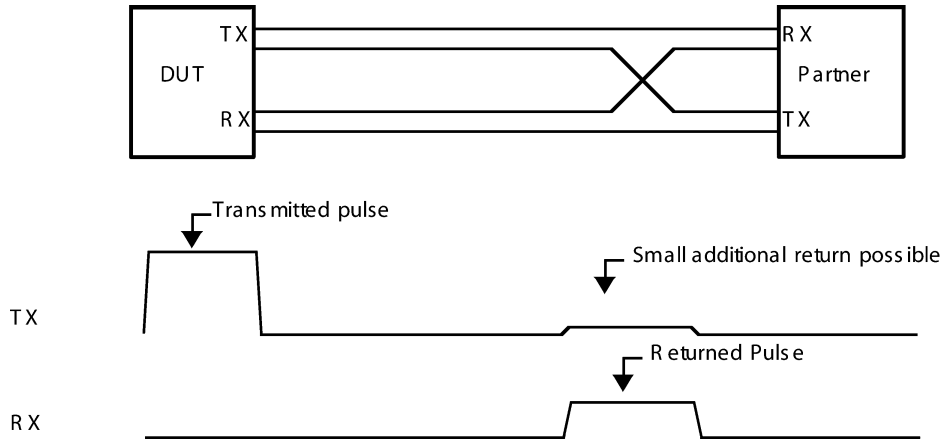

Figure 6. TX-/RX+ Cross-Wired Circuit (into Inactive or Unpowered Partner)

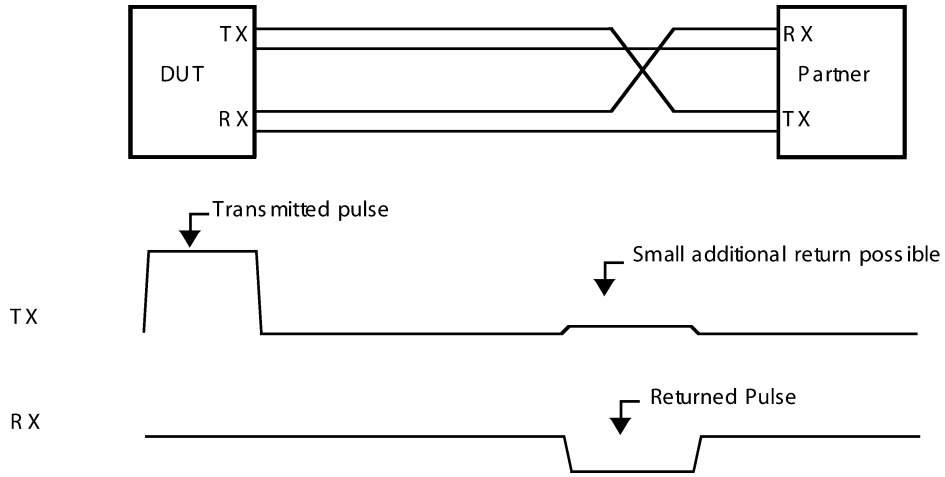

Figure 7. TX+/RX+ Cross-Wired Circuit (into Inactive or Unpowered Partner)

4.7 Checking for an Active Partner

Before making TDR measurements, it may be necessary to check for an active partner. If a partner is active, sending link pulses or data, then it may be difficult or impossible to use the TDR function to detect faults or measure cable length. Software may attempt to determine if a partner is active in a couple of ways.

4.7.1 Use of Energy Detect

The Energy Detect mechanism can be used to monitor the Transmit or Receive pairs for activity. Software may control which pair is monitored by setting the MDIX control to MDI for Transmit and MDIX for Receive. Auto-MDIX should be disabled to allow separate analysis of Transmit and Receive pairs. The device may be programmed to manually drop to a powered-down state. The Energy Detect status bits can then be monitored to detect activity. If activity is present on a pair then it may not be possible to make TDR measurements on that pair. If one pair shows activity, it may still be possible to make measurements on the other pair.

4.7.2 Use of Zero Length TDR pulse

The TDR mechanism allows for sending a pulse of 0 length, which provides a method to measure baseline activity. This can be used to check for constant signaling such as 100Mb Idles or packet data. It is not very effective at checking for link pulses, since the spacing between link pulses is much greater than the TDR sampling time. If the Energy Detect mechanism indicates activity, the TDR method can be used to determine if the activity is Link Pulses or constant signaling such as 100Mb Idles. TDR will always detect activity for 100Mb Idles or packet data, but only infrequently detect activity for Link Pulses. If the activity is Link Pulses only, it may still be possible to make TDR measurements by making multiple runs and averaging the results or throwing out spurious results.

The Zero Length TDR pulse may also be used to determine the DC Offset in the recovered signal. If no activity is present, the response should be a constant value with possibly one or two count variation due to noise. Both threshold settings and peak measurements may be modified by the DC offset to improve the accuracy of the TDR measurements.

4.8 Digital Scope Implementation

The TDR mechanism can be used to generate a summary waveform which is equivalent to a digital scope view of the response. Setting the window size to a single datapoint, the exact amplitude at that point can be measured and recorded. By making measurements at each datapoint, a representation of the full waveform can be generated. Software may take multiple measurements at each datapoint to average the results to eliminate effects of noise or other effects unrelated to the transmitted pulse. Taking this amount of data requires a significant amount of time, but should yield a very good picture of the cable response.

Figure 8 shows example plots showing the response for an open circuit connection using two different pulse types.

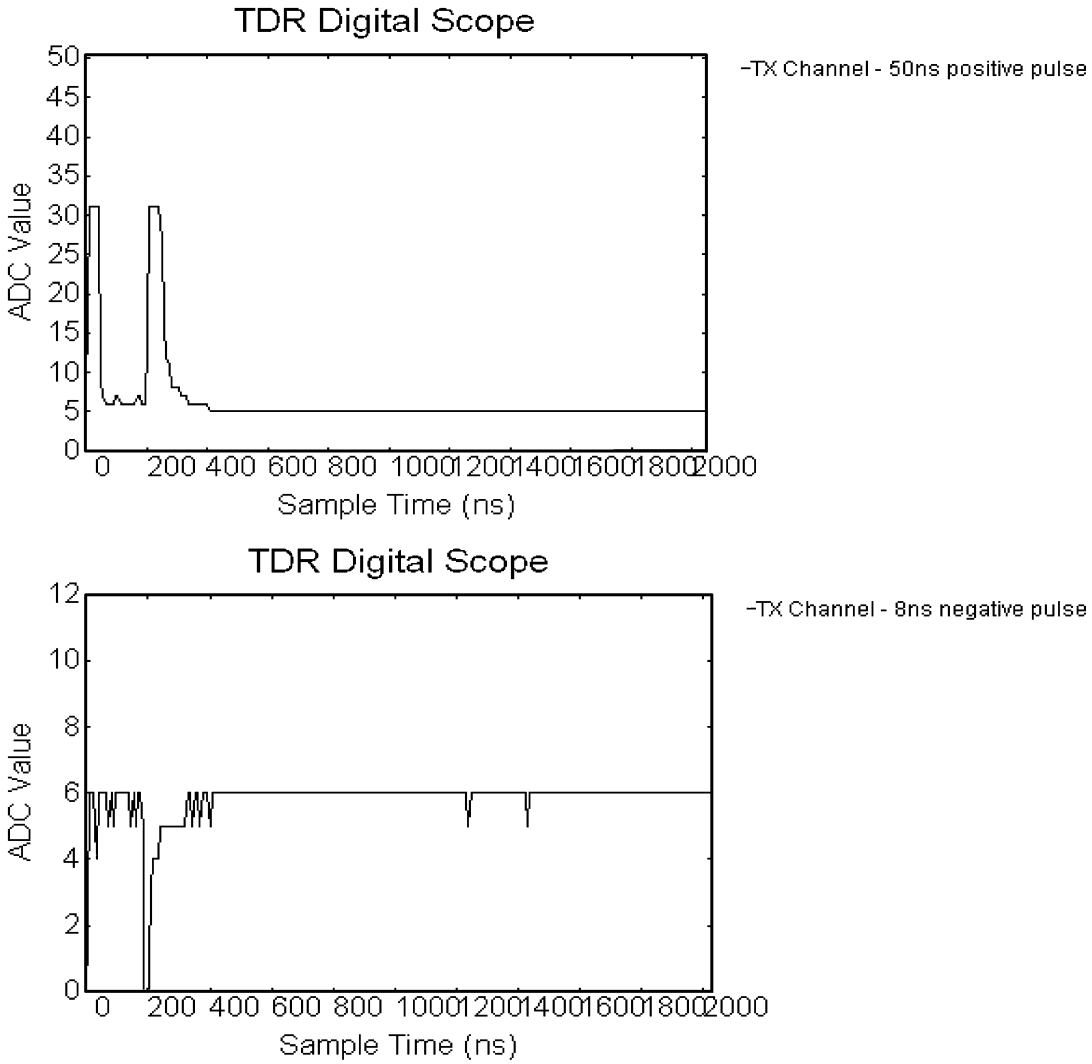

Figure 8. Far-end Cable Open Response

5 Integrity Utility

The Integrity Utility was developed to provide a simple to use and robust application that allows interaction with Ethernet Media Access Control (MAC) and Physical Layer (PHY) devices. The application has full support for the cable diagnostics features available in DP83849 Dual Port 10/100 Ethernet Transceiver.

5.1 Operating System Support

Integrity Utility supports the following operating systems:

- Microsoft Windows 2000
- Microsoft Windows XP

5.2 Summary Tab

The Summary tab (Figure 9) shows the state of the selected Phy port. It has sections that describe the device's characteristics, link state information and local and remote link partner auto-negotiation capabilities.

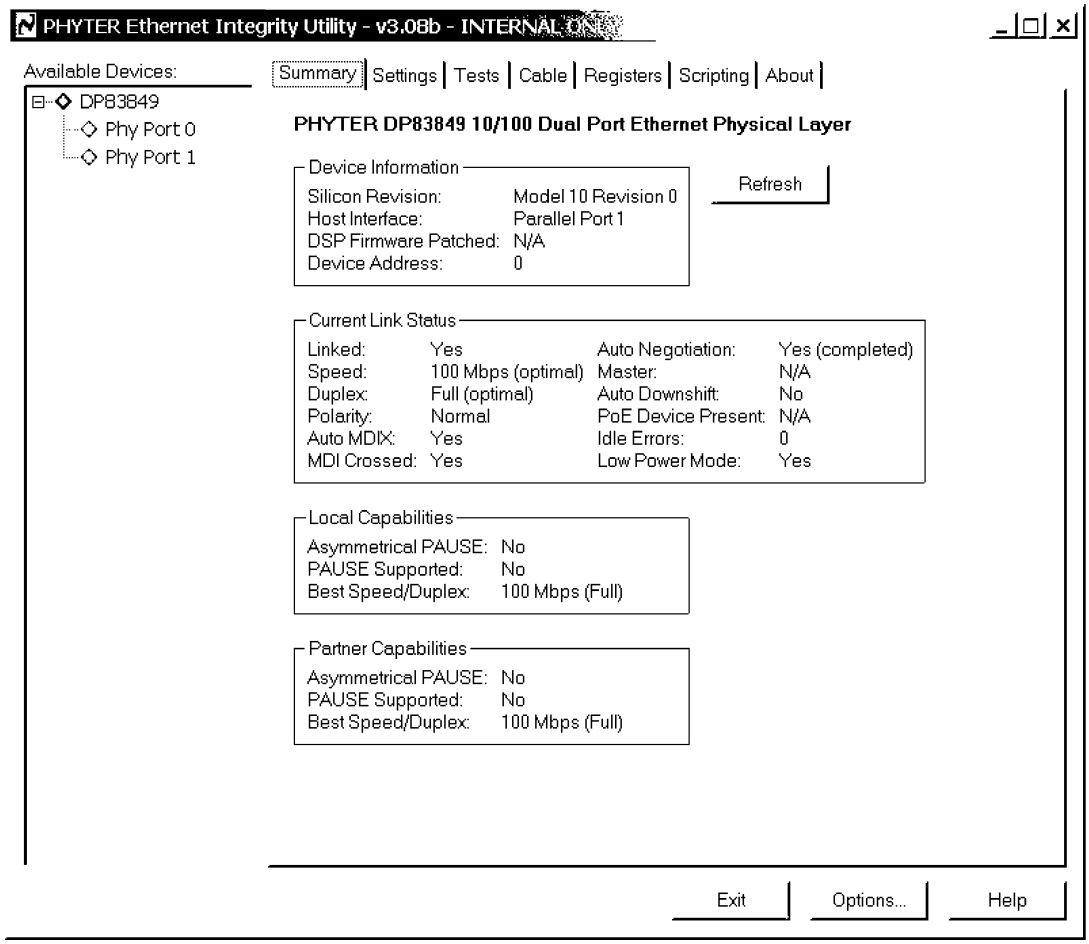

Figure 9. Integrity Utility-Summary Tab

5.3 Settings Tab

The Settings tab (Figure 10) provides a method of changing a port's link configuration. Interface to display registers, reset device, alter linked behavior, speed, duplex settings, MDI/MDIX selection and Energy detect on/off are provided.

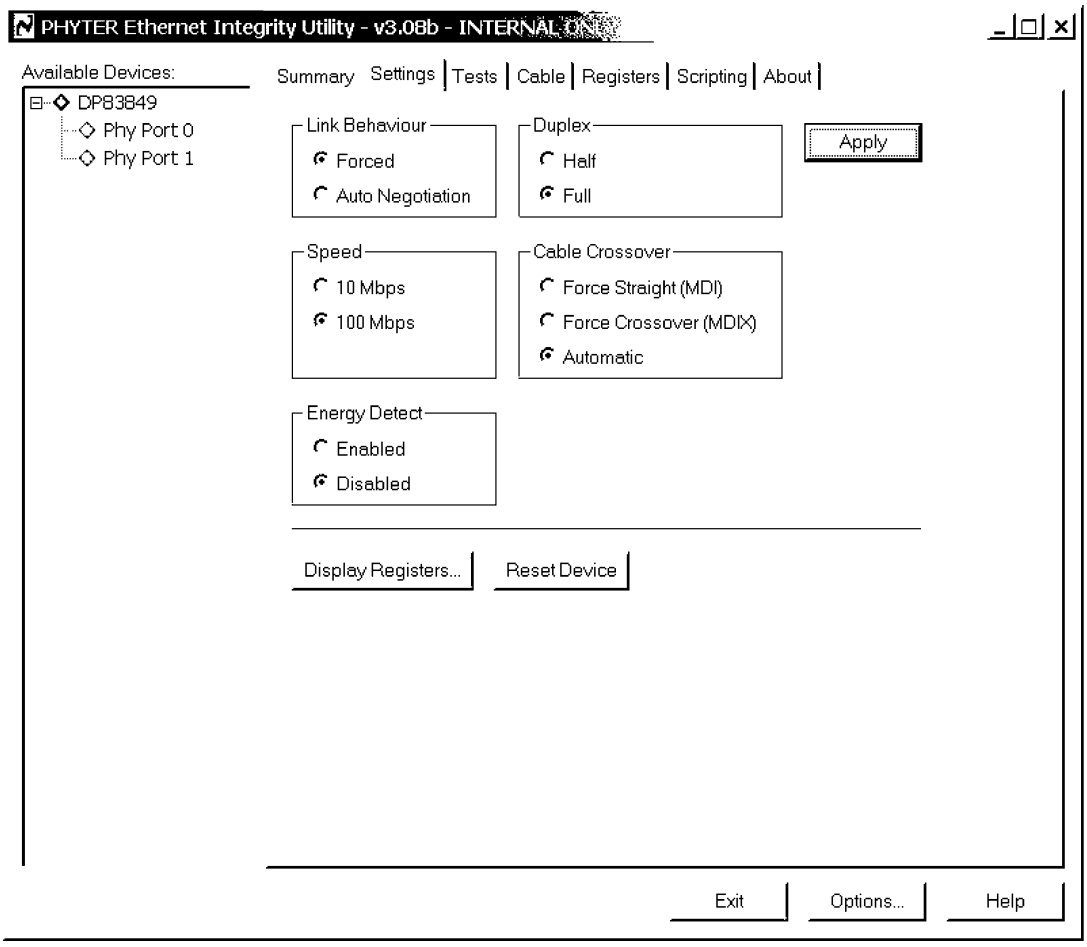

Figure 10. Integrity Utility-Settings Tab

5.4 Cable Diagnostics Tab

The Cable diagnostics tab (Figure 11) provides the interface to initiate cable diagnostics for DP83849 10/100 Dual Ethernet Phy. Polarity and MDI/MDIX status, electrical cable length estimate, frequency offset/Jitter and receive SNR can be read directly. Interface for TDR cable diagnostics for open/short, distance to fault, and so on, is provided. Link Quality Monitor interface allows setting of thresholds for various DSP parameters and observing alarm conditions.

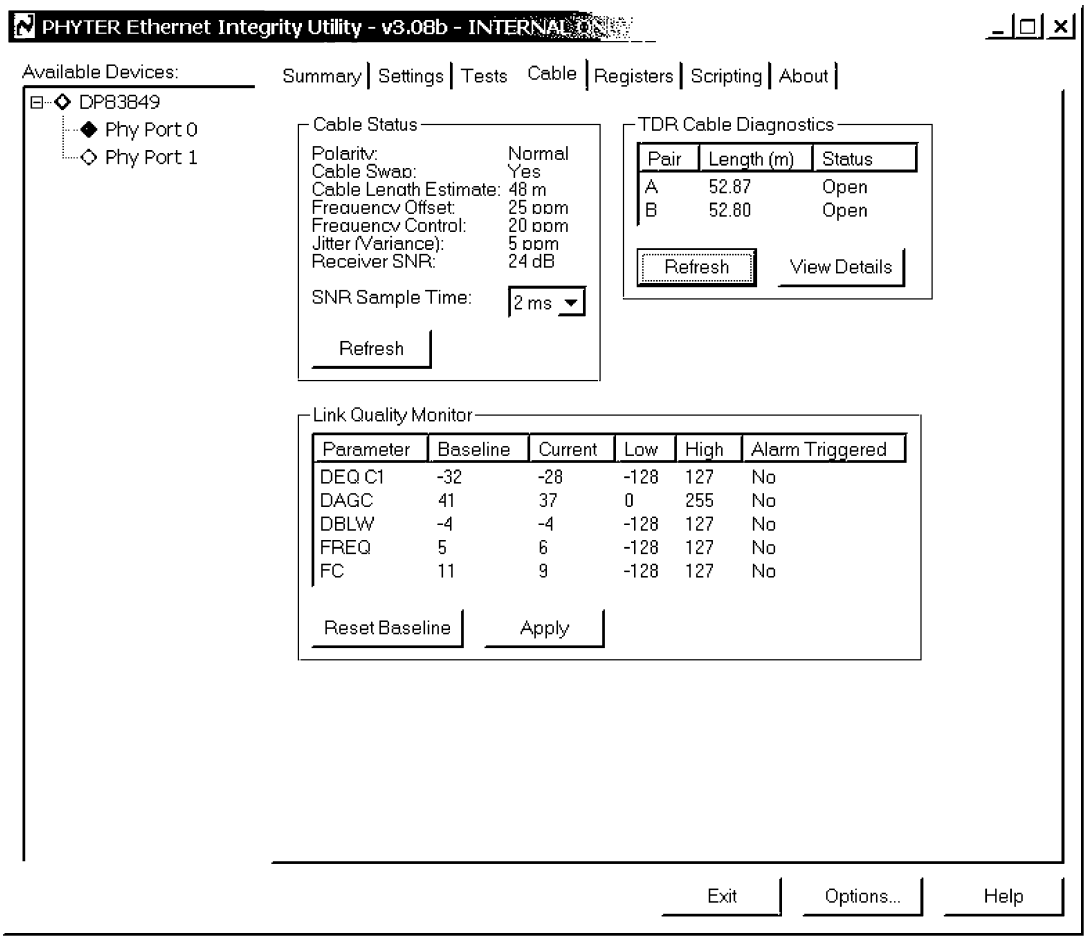

Figure 11. Integrity Utility-Cable Tab

5.5 Registers Tab

This Registers tab (Figure 12) provides a central location to view and modify the Phy base registers. It presents the selected register's individual bit values with a short description for each bit. The displayed register values are only updated after selecting the "Refresh" button or after modifying a register's value.

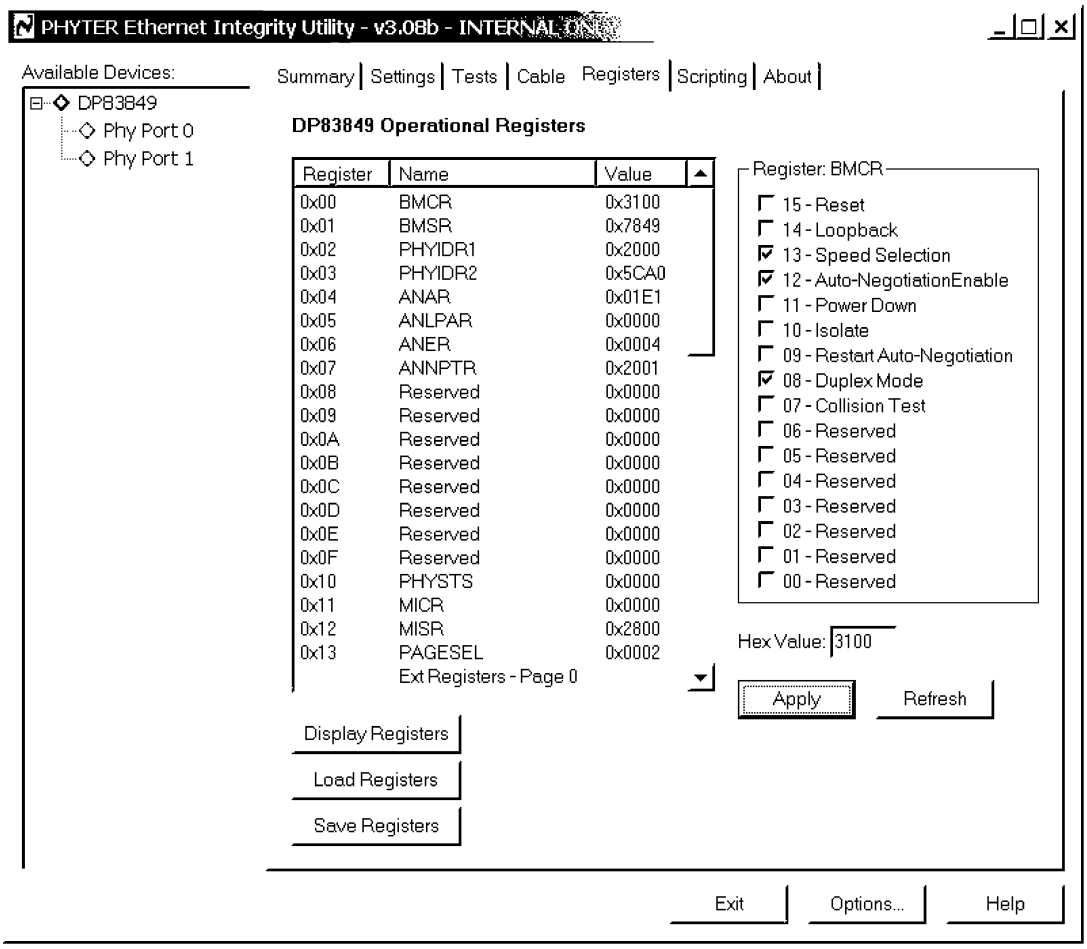

Figure 12. Integrity Utility-Registers Tab

5.6 Scripting Tab

The Scripting tab (Figure 13) provides a Python interpreter command prompt. The GUI application uses the Texas Instruments Ethernet Library to interact with the underlying DP83849 devices. Custom Python scripts can be developed that provide additional functionality not found in the GUI application.

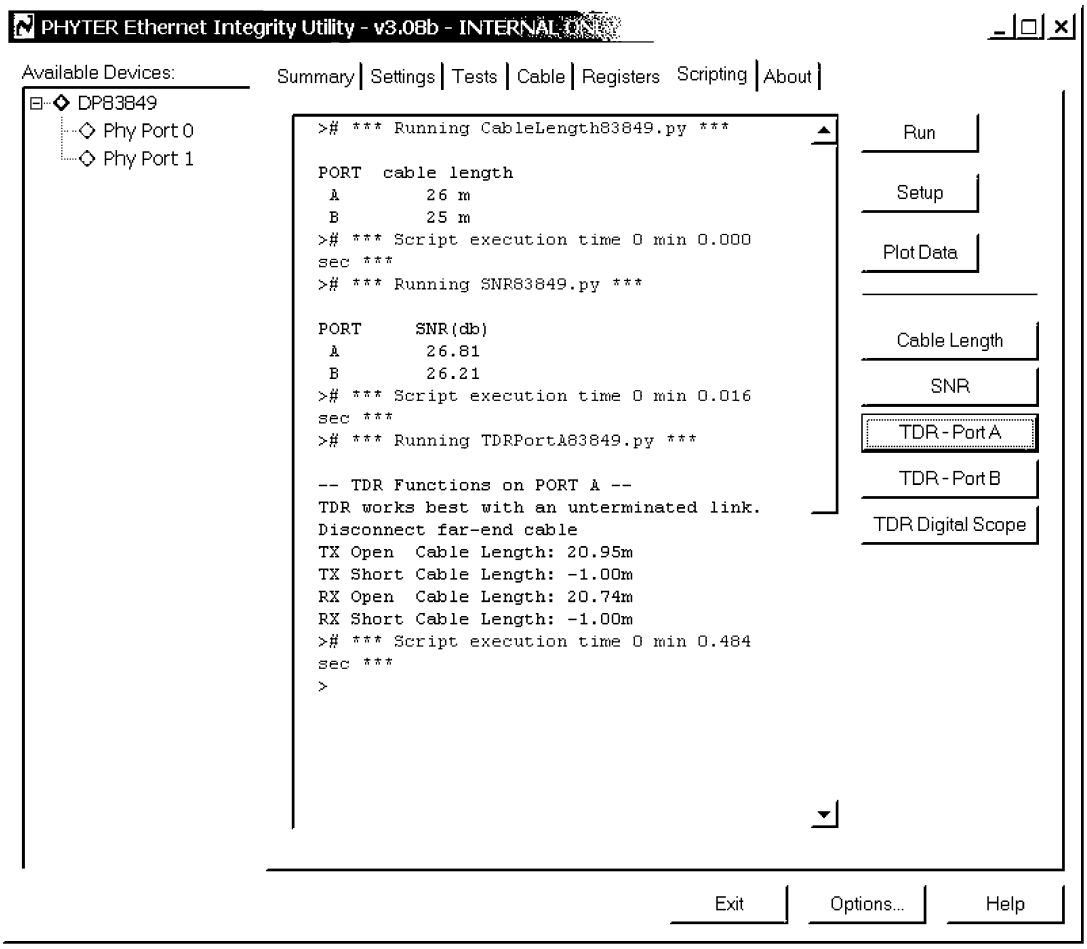

Figure 13. Integrity Utility-Scripting Tab

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