Functional Safety Information

LMT86-Q1 Functional Safety FIT Rate, FMD and Pin FMA

ABSTRACT

This document provides important information on the LMT86-Q1 (SC70 package) that can aid in functional safety system designs. This document discusses:

- The failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards in combination with expert judgement
- The component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

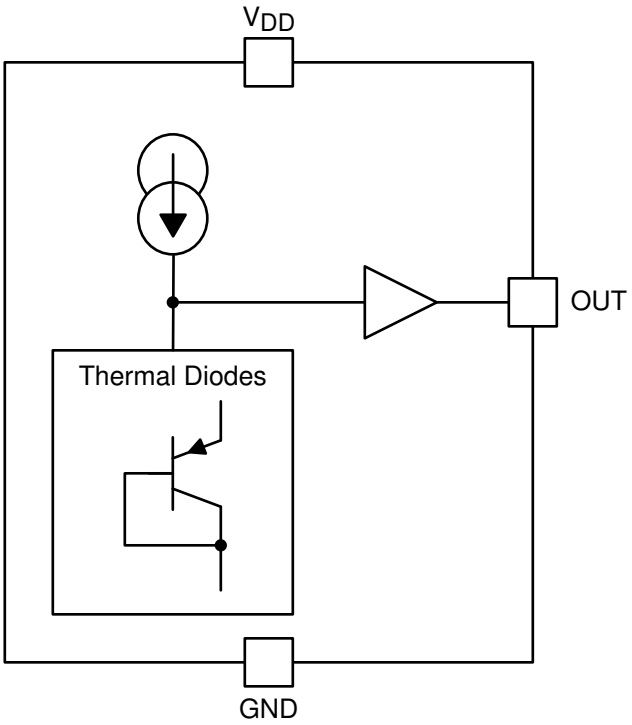

Figure 1-1. Functional Block Diagram

The LMT86-Q1 was developed using a quality-managed development process, but was not developed in accordance with the ISO 26262 standards.

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1 Failure In Time (FIT) Rates

This section provides Failure In Time (FIT) rates for LMT86-Q1 based on two different industry-wide used reliability standard. Table 1-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11.

Table 1-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Per 10^9 Hours)
Total Component FIT Rate	4
Die FIT Rate	2
Package FIT Rate	2

The failure rate and mission profile information in Table 1-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1.0mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

2 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMT86-Q1 in Table 2-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgments.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 2-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (HIZ)	15%
VOUT short to VDD	20%
VOUT short to GND	20%
VOUT not in specification	45%

3 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMT86-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 3-2)
- Pin open-circuited (see Table 3-3)
- Pin short-circuited to an adjacent pin (see Table 3-4)
- Pin short-circuited to supply (see Table 3-5)

Table 3-2 through Table 3-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 3-1.

Table 3-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.

Table 3-1. TI Classification of Failure Effects (continued)

Class	Failure Effects
D	No device damage, no impact to functionality or performance.

Figure 3-1 shows the SC70 package pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMT86-Q1 data sheet.

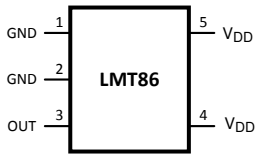

Figure 3-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Bypass capacitor on the input voltage pin of 0.01 µF.
- Series resistors are sized to limit the input currents to the analog inputs to < 5 mA.
- Capacitive loading on output pin is limited to 1100 pF.

Table 3-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	No effect. Normal operation.	D
GND	2	No effect. Normal operation.	D
OUT	3	Output stuck low. No analog output present on device.	B
VDD	4	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
VDD	5	Expected analog output from device can be altered.	B

Table 3-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Expected analog output from device can be altered.	B
GND	2	Device functionality undetermined. Device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
OUT	3	No effect. Normal operation.	D
VDD	4	Expected analog output from device can be altered.	B
VDD	5	Expected analog output from device can be altered.	B

Table 3-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	GND	No effect. Normal operation.	D
GND	2	OUT	Device functionality undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
OUT	3	GND	Output stuck low. No analog output present on device.	B
VDD	4	VDD	No effect. Normal operation.	D
VDD	5	VDD	No effect. Normal operation.	D

Table 3-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Expected analog output from device can be altered.	B
GND	2	Device functionality undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
OUT	3	Output stuck high.	B
VDD	4	No effect. Normal operation.	D
VDD	5	No effect. Normal operation.	D

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2020) to Revision A (October 2021)	Page
• Added *Pin Failure Mode Analysis (Pin FMA)* section	2

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