UCD3138128A Migration Guide

User's Guide

Literature Number: SNIU030
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Introduction

This application note describes the significant differences between Texas Instruments' UCD3138128 and UCD3138128A Digital Power Controllers to assist customers in migrating applications. While the main focus of this document is migration from UCD3138128 to UCD3138128A, this document is also useful if you are considering migrating in the reverse direction. Functions that are identical in both devices are not included in this document. All efforts have been made to provide a comprehensive list of the differences between the two devices in the UCD3138 family.

The UCD3138128A device is the newest member of the UCD3138 integrated digital power controller family. This device has the following enhancements from the UCD3138128:

- The General Purpose ADC has been improved for better accuracy and performance at extreme cold temperatures (–40°C)
- The UART peripheral has been modified to include a hardware based auto-baud rate adjustment feature
- A new, Synchronous Rectifier Dead Time Optimization hardware peripheral has been added. It’s called DTC (Dead Time Control).
- A crystal oscillator has been added to the Real Time Clock (RTC).
- PMBus/I2C peripherals can now operate up to 1 MHz

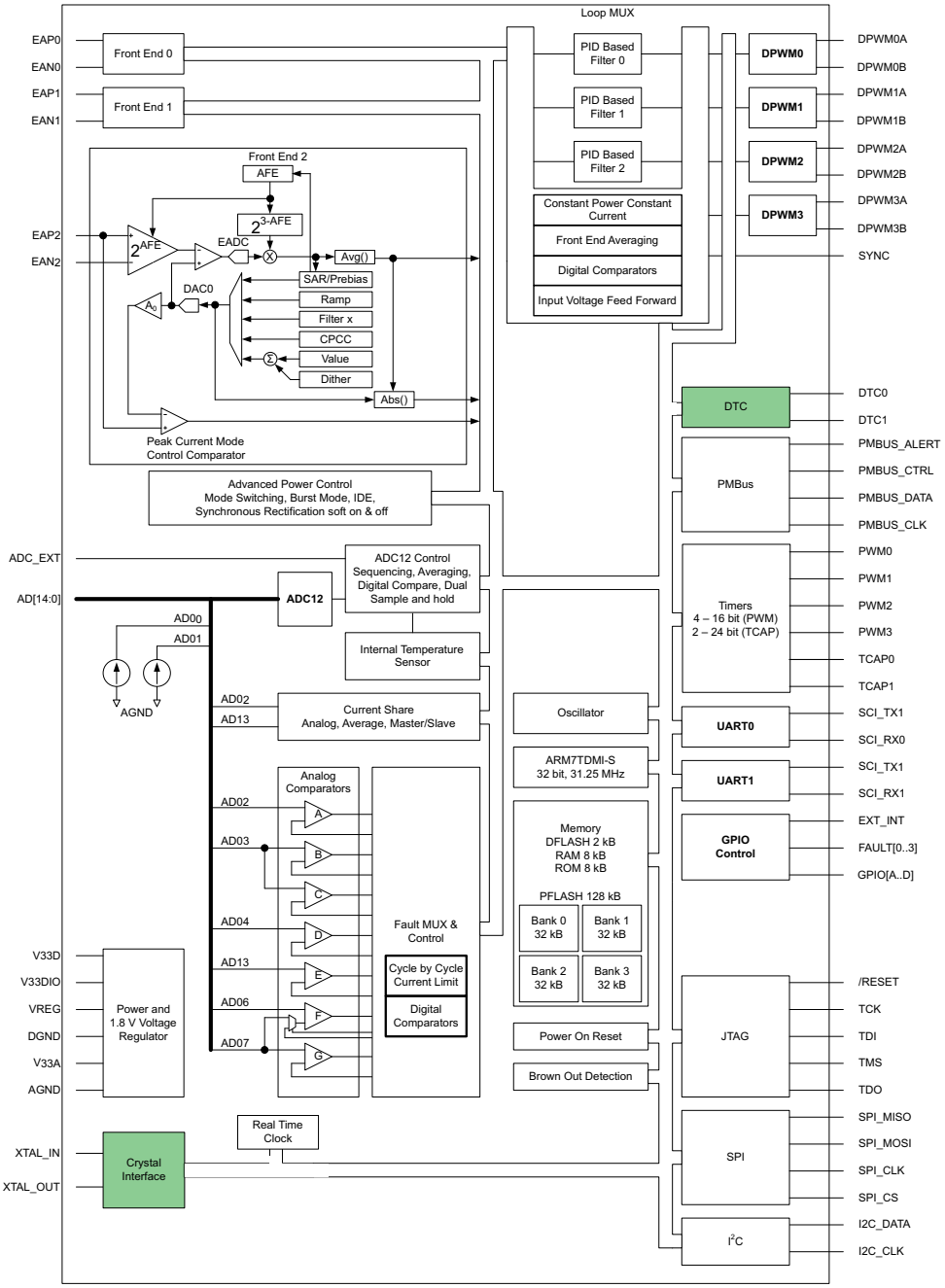


Figure 1-1. UCD3138128A Block Diagram

The UCD3138128 already has many additions and improvements over earlier devices, so consult the UCD3138128 Programmer's Manual as well if porting code from one of these earlier devices.

Device Overview Summary

2.1 New Features

Table 2-1. New Features in UCD3138128A

Peripheral	Features / Changes	Detail Description
DTC (new)	Synchronous Rectifier Optimization Algorithm with body diode conduction time sensing	Addition of DTC pins for UCD7138 Synchronous Rectifier Driver with Body Diode Conduction Time Reporting
UART	UART enhancements	UCD3138128: no auto baud rate adjustment UCD3138128A: UART auto calibration to correct BAUD Rate
RTC crystal	Real Time Clock Crystal Interface	A crystal oscillator circuit is added to the Real Time Clock to provide accurate timekeeping.

2.1.1 Body Diode Conduction Sensing

Benefits:

- Maximize system efficiency by minimizing MOSFET body diode conduction time
- Robust fast negative current protection.
- Simple interface
  - Minimum component count
  - No external sense element
  - Easy layout
- Superior to R_{DSon} sensing techniques
  - Better accuracy across entire load range
  - No minimum on time requirement
  - No parasitic L and R concerns

UCD3138128A has an advanced dead time control interface where it can accept UCD7138 output signals and optimize SR gate driver signals accordingly. The UCD7138 low-side MOSFET driver is a high performance driver for secondary-side synchronous rectification (SR) with body diode conduction sensing. The device is suitable for high power high efficiency isolated converter applications where dead-time optimization is desired.

The UCD7138 gate driver is a companion device to the UCD3138128A highly integrated digital controller for isolated power. DTC0 and DTC1 are received body diode conduction inputs from the UCD7138. SR0_DPWM and SR1_DPWM are the DPWM waveforms for the SRs. The red and green edges are moving edges controlled by both the filter output and the DTC interface. In each cycle, right after the falling edge of the SR DPWM waveform, a body diode conduction time detection window is generated. The detection window is defined by both DETECT_BLANK and DETECT_LEN registers. During this detection window, a 4-ns timer capture counts how long the body diode conducts. Then the SR DPWM falling edge of the next cycle is adjusted accordingly.

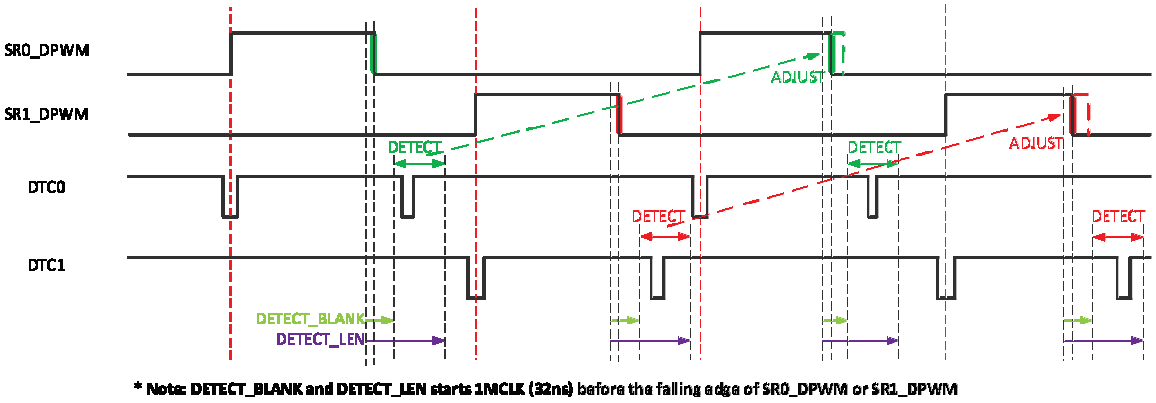


Figure 2-1. DTC Waveforms

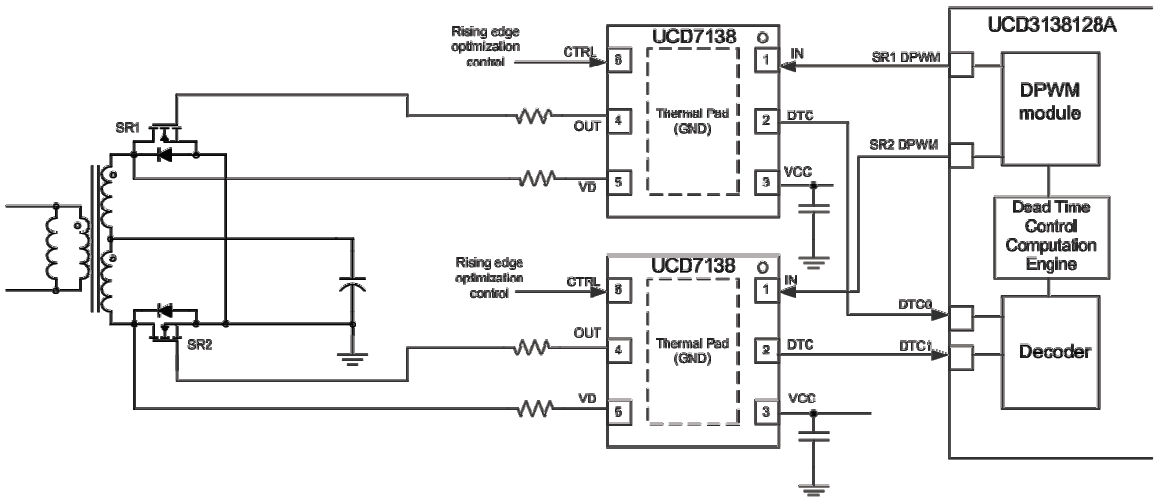


Figure 2-2. Low Side Gate Driver with Body Diode Conduction Sensing

For more information on using the UCD7138 with the UCD3138128A, see Using UCD7138 and UCD3138A for Advanced Synchronous Rectification Control.

2.1.2 UART Auto Baud Enhancement

The UCD3138128A has many UART enhancements. One of them is that it has in built hardware dedicated just to capture the receiving pulses on the Rx pin of the UART. This along with some minimal firmware can be used to calculate the exact BAUD rate of the other device.

Some of the other UART enhancements are:

- It has a finer resolution. The BAUD rate granularity is about 64 ns compared to the 512 ns of the ‘128. This permits significantly better baud rate matching at higher baud rates. A new register (UARTSBAUD) is used to control the divider for the extra resolution
- It has an auto sync on start bit. The free running counter of the UART gets reset when it detects a start bit. This makes the sampling time well aligned with the center of the pulses.
- It allows independent Rx and Tx BAUD rate capability. The UART Rx has some new registers: UARTRXMBAUD, UARTRXLBAUD and UARTRXSBAUD. They have the same meaning as the general UART registers: UARTMBAUD, UARTLBAUD and UARTSBAUD.

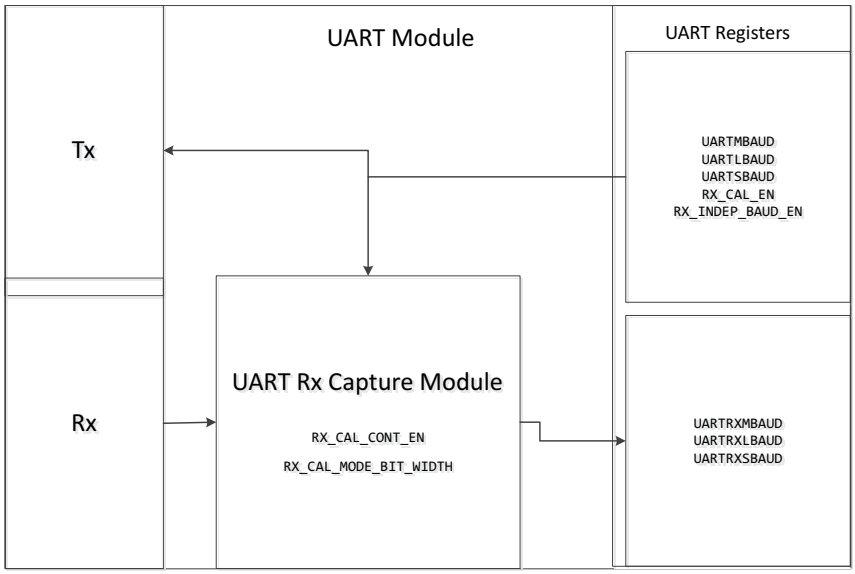


Figure 2-3. UART Enhancements

For more details please refer to Hardware based UART Auto BAUD correction [SPRxxxx]

2.1.3 RTC Crystal Oscillator Added

A crystal interface was added to the RTC logic from the UCD3138128. It is designed to be used with a 10 MHz external crystal. 3 bitfields were added to the RTCCTRL register to control internal capacitors and bias resistance. This should make it unnecessary to use external capacitors to match the crystal to the PC board and oscillator capacitance. See the data sheet for details on how to use these registers. The CONFIG_INCL bitfield in the RTCCTRL register is enhanced to support the crystal oscillator.

2.2 Bug Fixes and Enhancements

Table 2-2. Table 2. Enhancements in UCD3138128A

Peripheral	Features / Changes	Detail Description
ADC	Improved ADC INL accuracy at cold temp –40°C	UCD3138128: INL +/-2.5 LSBs typical from 25°C to 125°C UCD3138128A: INL +/- 4.5 LSBs max across temperature –40°C to 125°C

Table 2-2. Table 2. Enhancements in UCD3138128A (continued)

Peripheral	Features / Changes	Detail Description
DPWM	DPWMxA and B can be restarted on the fly without resetting the DPWM module.	UCD3138128: If either DPWM pin is latched off by a fault, the whole DPWM module has to be disabled to clear the fault. UCD3138128A: writing a 1 and then a 0 to the FLT_RESTART bit will restart either or both DPWM pins without turning off the entire module
PMBus	1 MHz support	UCD3138128: 400kHz support UCD3138128A: 1 MHz support
Chip Level	Current consumption	Please refer to electrical specification of UCD3138128A datasheet. [SLUSCA5]
Event	Resonant mode dead times are determined only by Event 1	UCD3138128: Dead time is programmed by all 4 Event registers. Dead Time 1 = Event 3 – Event 2 Dead Time 2 = Event 1 + Period Register – Event 4 Average Dead Time = (Dead Time 1 + Dead Time 2)/2 DPWM A Rising Edge = Event 1 DPWM A Falling Edge = Event 1 + Filter Duty – Average Dead Time Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register DPWM B Rising Edge = Event 1 + Filter Duty – Average Dead Time + (Event 3 – Event 2) DPWM B Falling Edge = Filter Period – (Period Register – Event 4) Phase Trigger = Phase Trigger Register value or Filter Duty UCD3138128A: Dead times are determined only by Event 1 register value. DPWM A Rising Edge = Event 1 DPWM A Falling Edge = Filter Duty – Event 1 + DTC Adjustment Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register DPWM B Rising Edge = Filter Duty + Event 1 DPWM B Falling Edge = Filter Period – Event 1 + DTC Adjustment Phase Trigger = Phase Trigger Register value or Filter Duty Note: It may be possible to use the DTC logic, with or without the UCD7138, to add asymmetry back into the resonant mode dead time if it is required.
Sync FET Soft Start	Waveform Change	UCD3138128 – Soft start keeps the Sync FET rising edge fixed as close as possible to the Primary FET falling edge. The falling edge of the Sync FET signal moves from the fixed rising edge toward the end of the period for ramp up, and moves it in from the end of the period for ramp down. UCD3138128A – Soft start keeps the Sync FET falling edge fixed as close as possible to the Primary FET rising edge, and moves the Sync FET rising edge toward the Primary FET falling edge for ramp up and away for ramp down.

2.3 Sync FET Soft Start

Here is a diagram showing the different FET soft start waveforms used on the two devices. Note that the 128 moves the falling edge of the Sync FET signal away from the fixed rising edge for ramp up, while the 128A moves the rising edge away from the fixed falling edge.

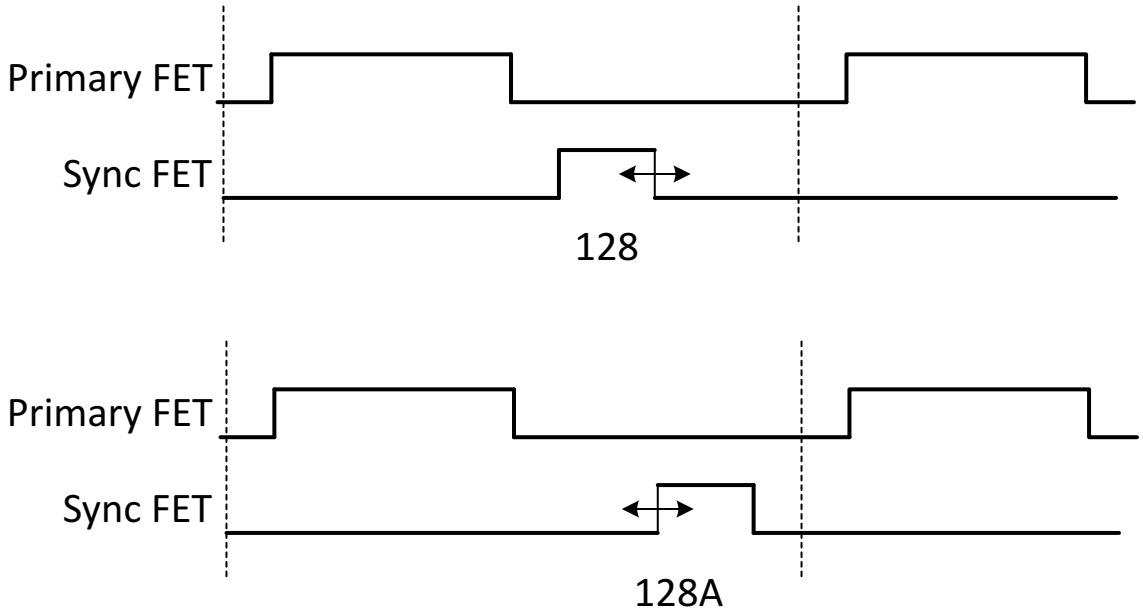


Figure 2-4. Sync FET Soft Start Changes

2.4 Pin Name and Interface Updates

This device is 100 % pin to pin backward compatible to UCD3138128. The GPIOA and GPIOB pins are now used for DTC. They can still be used for interrupts and for General Purpose I/O. The controls for interrupt functions are still in the same memory location, but the I/O functions (IN, OUT and DIR) are now inside the DTC registers. Note that the default values for the DIR bits are the same, but the meaning is different. The '128 DIR bit has 0 to make the pin an input, but the 0 default on the 128A makes the pin an output.

All of the bits dealing with interrupts are in the same location on both parts, but the names are different, because the pin names change from GPIO to DTC.

Here is a table with all of the variable names for the GPIOA. GPIOB is the same, except for replacing the A with a B.

Table 2-3. GPIOA Changes to DTC

Function	UCD3138128	UCD3138128A
Make GPIO	Always GPIO	LoopMuxRegs.DTCIOCTRL.bit.DTC_A_FUNC = 1
IN	GioRegs.FAULTIN.bit.GIO_A_IN	LoopMuxRegs.DTCIOCTRL.bit.DTC_A_GPIO_IN
Make Output	GioRegs.FAULTDIR.bit.GIO_A_DIR = 1	LoopMuxRegs.DTCIOCTRL.bit.DTC_A_GPIO_DIR = 0
Make Input	GioRegs.FAULTDIR.bit. GIO_A _DIR = 0	LoopMuxRegs.DTCIOCTRL.bit.DTC_A_GPIO_DIR = 1
Output Value	GioRegs.FAULTOUT.bit.GIO_A_OUT	LoopMuxRegs.DTCIOCTRL.bit.DTC_A_GPIO_VAL
Enable Interrupt	GioRegs.FAULTINTENA.bit.GIO_A_INT_EN = 1	GioRegs.FAULTINTENA.bit.DTC_A_INT_EN = 1
Interrupt Polarity	GioRegs.FAULTINTPOL.bit.GIO_A_INT_POL	GioRegs.FAULTINTPOL.bit.DTC_A_INT_POL
Interrupt Pending	GioRegs.FAULTINTPEND.bit.GIO_A_INT_PEND	GioRegs.FAULTINTPEND.bit.DTC_A_INT_PEND

GPIOC and GPIOD have similar changes, with their I/O functions in a special GioCDRegs register area. The same change applies to the DIR bit meaning here as for A and B above. The interrupt bits are unchanged from the '128.

Table 2-4. GPIOC Changes to GioCDRegs

Function	UCD3138128	UCD3138128A
Make GPIO	Always GPIO	Always GPIO
IN	GioRegs.FAULTIN.bit.GIO_C_IN	GioCDRegs.GIOCCTRL.bit.GIO_C_IN
Make Output	GioRegs.FAULTDIR.bit.GIO_C_DIR = 1	GioCDRegs.GIOCCTRL.bit.GIO_C_DIR = 0
Make Input	GioRegs.FAULTDIR.bit. GIO_C _DIR = 0	GioCDRegs.GIOCCTRL.bit.GIO_C_DIR = 1
Output Value	GioRegs.FAULTOUT.bit.GIO_C_OUT	GioCDRegs.GIOCCTRL.bit.GIO_C_VAL
Enable Interrupt	GioRegs.FAULTINTENA.bit.GIO_C_INT_EN = 1	Same
Interrupt Polarity	GioRegs.FAULTINTPOL.bit.GIO_C_INT_POL	Same
Interrupt Pending	GioRegs.FAULTINTPEND.bit.GIO_C_INT_PEND	Same

2.5 Revision Update

Table 2-5. Chip Revision ID Field Updated

Module	Features / Changes	Detail Description
Chip Level	Device ID/Revision Update	UCD3138128: DEV register returns 0x1447 Firmware DEVICE ID: “UCD3138128V1” UCD3138128A: DEV register returns 0x2447 Firmware: DEVICE ID “UCD3138128A”

2.6 Changes to Watchdog Timer Time Base

The design of the low speed clock which drives the watchdog timer has changed, which causes a change in the min and max range of the times for the watchdog. Please consult the datasheet for the latest timing.

Application Migration Requirements

3.1 Change to Device ID

The TI GUIs designed for use with the UCD parts use a PMBus command called DEVICE_ID to determine which device is being used. On the UCD3138128A, the initial part of the DEVICE_ID string should change to “UCD3138128A”.

3.2 Possible Changes to Layout and Power Supply Filtering

The UCD3138128A has different sensitivity to EMI and power supply noise than the UCD3138128. Designs that are marginal with the non-A may require changes to board layout and filtering to work with the A version. See the datasheet and the UCD3138 - Practical Design Guideline Application Note for more information.

3.3 LLC and Phase Shift-LLC Topologies

The UCD3138128A has a DTC interface that works in conjunction with the UCD7138 smart gate driver to continuously optimize dead times. This can improve reliability and efficiency and reduce development time. Please refer to Section 2.1.1, Body Diode Conduction Time Sensing for more details on how to use the DTC with the UCD7138.

See the changes in resonant dead time calculations in Table 2, Enhancements in UCD3138128A. If the dead times are symmetrical between the phases for LLC, there should be no change needed.

The new resonant mode dead time calculation doesn’t support asymmetrical dead times. It may be possible to use the DTC logic in manual mode without the UCD7138 to support some asymmetrical dead times. Check with Texas Instruments for more information.

The DTC with the UCD7138 can automatically provide asymmetrical dead times if they are appropriate.

3.4 HSFB, PFSB, PFC Technologies

No changes are needed for these topologies from UCD3138128 programs unless Sync FET soft start/stop is used. See the description of this change above. See the UCD3138128 Programmer’s Manual for changes required from other devices in the UCD3138 family.

Memory Map for UCD3138128A

This section describes all the peripheral registers of the UCD3138128A. Registers and bitfields highlighted in green have been changed from the UDC3138128.

Topic **Page**

4.1 Loop Mux Registers Reference

4.1.1 Front End Control 0 Mux Register (FECTRL0MUX)

Address 00120000

Figure 4-1. Front End Control 0 Mux Register (FECTRL0MUX)

13	12	11	10	9	8
NL_SEL		DPWM3_FRAME_SYNC_EN	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN	DPWM0_FRAME_SYNC_EN
R/W-00		R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-1. Front End Control 0 Mux Register (FECTRL0MUX) Register Field Descriptions

Bit	Field	Type	Reset	Description
13-12	NL_SEL	R/W	00	Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting 0 = Filter 0 NL Results used (Default) 1 = Filter 1 NL Results used 2 = Filter 2 NL Results used
11	DPWM3_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control 0 = DPWM 3 Frame Sync not routed to Front End Control (Default) 1 = DPWM 3 Frame Sync routed to Front End Control
10	DPWM2_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control 0 = DPWM 2 Frame Sync not routed to Front End Control (Default) 1 = DPWM 2 Frame Sync routed to Front End Control
9	DPWM1_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control 0 = DPWM 1 Frame Sync not routed to Front End Control (Default) 1 = DPWM 1 Frame Sync routed to Front End Control
8	DPWM0_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control 0 = DPWM 0 Frame Sync not routed to Front End Control (Default) 1 = DPWM 0 Frame Sync routed to Front End Control
7	DPWM3_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 3 PWM-B to Front End Contro l0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 3 PWM-B trigger routed to Front End Control
6	DPWM2_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control 0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 2 PWM-B trigger routed to Front End Control
5	DPWM1_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control 0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 1 PWM-B trigger routed to Front End Control
4	DPWM0_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control 0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 0 PWM-B trigger routed to Front End Control
3	DPWM3_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control 0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 3 PWM-A trigger routed to Front End Control

Table 4-1. Front End Control 0 Mux Register (FECTRL0MUX) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DPWM2_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control 0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 2 PWM-A trigger routed to Front End Control
1	DPWM1_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control 0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 1 PWM-A trigger routed to Front End Control
0	DPWM0_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control 0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 0 PWM-A trigger routed to Front End Control

4.1.2 Front End Control 1 Mux Register (FECTRL1MUX)

Address 00120004

Figure 4-2. Front End Control 1 Mux Register (FECTRL1MUX)

13	12	11	10	9	8
NL_SEL		DPWM3_FRAME_SYNC_EN	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN	DPWM0_FRAME_SYNC_EN
R/W-01		R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-2. Front End Control 1 Mux Register (FECTRL1MUX) Register Field Descriptions

Bit	Field	Type	Reset	Description
13-12	NL_SEL	R/W	01	Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting 0 = Filter 0 NL Results used 1 = Filter 1 NL Results used (Default) 2 = Filter 2 NL Results used
11	DPWM3_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control 0 = DPWM 3 Frame Sync not routed to Front End Control (Default) 1 = DPWM 3 Frame Sync routed to Front End Control
10	DPWM2_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control 0 = DPWM 2 Frame Sync not routed to Front End Control (Default) 1 = DPWM 2 Frame Sync routed to Front End Control
9	DPWM1_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control 0 = DPWM 1 Frame Sync not routed to Front End Control (Default) 1 = DPWM 1 Frame Sync routed to Front End Control
8	DPWM0_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control 0 = DPWM 0 Frame Sync not routed to Front End Control (Default) 1 = DPWM 0 Frame Sync routed to Front End Control
7	DPWM3_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 3 PWM-B to Front End Control 0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 3 PWM-B trigger routed to Front End Control
6	DPWM2_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control 0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 2 PWM-B trigger routed to Front End Control
5	DPWM1_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control 0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 1 PWM-B trigger routed to Front End Control
4	DPWM0_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control 0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 0 PWM-B trigger routed to Front End Control
3	DPWM3_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control 0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 3 PWM-A trigger routed to Front End Control
2	DPWM2_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control 0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 2 PWM-A trigger routed to Front End Control

Table 4-2. Front End Control 1 Mux Register (FECTRL1MUX) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DPWM1_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control 0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 1 PWM-A trigger routed to Front End Control
0	DPWM0_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control 0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 0 PWM-A trigger routed to Front End Control

4.1.3 Front End Control 2 Mux Register (FECTRL2MUX)

Address 00120008

Figure 4-3. Front End Control 2 Mux Register (FECTRL2MUX)

13	12	11	10	9	8
NL_SEL		DPWM3_FRAME_SYNC_EN	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN	DPWM0_FRAME_SYNC_EN
R/W-10		R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-3. Front End Control 2 Mux Register (FECTRL2MUX) Register Field Descriptions

Bit	Field	Type	Reset	Description
13-12	NL_SEL	R/W	10	Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting 0 = Filter 0 NL Results used 1 = Filter 1 NL Results used 2 = Filter 2 NL Results used (Default)
11	DPWM3_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control 0 = DPWM 3 Frame Sync not routed to Front End Control (Default) 1 = DPWM 3 Frame Sync routed to Front End Control
10	DPWM2_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control 0 = DPWM 2 Frame Sync not routed to Front End Control (Default) 1 = DPWM 2 Frame Sync routed to Front End Control
9	DPWM1_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control 0 = DPWM 1 Frame Sync not routed to Front End Control (Default) 1 = DPWM 1 Frame Sync routed to Front End Control
8	DPWM0_FRAME_SYNC_EN	R/W	0	Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control 0 = DPWM 0 Frame Sync not routed to Front End Control (Default) 1 = DPWM 0 Frame Sync routed to Front End Control
7	DPWM3_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 3 PWM-B to Front End Control 0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 3 PWM-B trigger routed to Front End Control
6	DPWM2_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control 0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 2 PWM-B trigger routed to Front End Control
5	DPWM1_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control 0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 1 PWM-B trigger routed to Front End Control
4	DPWM0_B_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control 0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default) 1 = DPWM 0 PWM-B trigger routed to Front End Control
3	DPWM3_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control 0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 3 PWM-A trigger routed to Front End Control
2	DPWM2_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control 0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 2 PWM-A trigger routed to Front End Control

Table 4-3. Front End Control 2 Mux Register (FECTRL2MUX) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DPWM1_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control 0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 1 PWM-A trigger routed to Front End Control
0	DPWM0_A_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control 0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default) 1 = DPWM 0 PWM-A trigger routed to Front End Control

4.1.4 Sample Trigger Control Register (SAMPTRIGCTRL)

Address 0012000C

Figure 4-4. Sample Trigger Control Register (SAMPTRIGCTRL)

11	10	9	8
FE2_TRIG_DPWM3_EN	FE2_TRIG_DPWM2_EN	FE2_TRIG_DPWM1_EN	FE2_TRIG_DPWM0_EN
R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
FE1_TRIG_ DPWM3_EN	FE1_TRIG_ DPWM2_EN	FE1_TRIG_ DPWM1_EN	FE1_TRIG_ DPWM0_EN	FE0_TRIG_ DPWM3_EN	FE0_TRIG_ DPWM2_EN	FE0_TRIG_ DPWM1_EN	FE0_TRIG_ DPWM0_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-4. Sample Trigger Control Register (SAMPTRIGCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
11	FE2_TRIG_ DPWM3_EN	R/W	0	Enables Sample Trigger from DPWM 3 to Front End Control 2 0 = DPWM 3 Sample Trigger not routed to Front End Control 2 (Default) 1 = DPWM 3 Sample Trigger routed to Front End Control 2
10	FE2_TRIG_ DPWM2_EN	R/W	0	Enables Sample Trigger from DPWM 2 to Front End Control 2 0 = DPWM 2 Sample Trigger not routed to Front End Control 2 (Default) 1 = DPWM 2 Sample Trigger routed to Front End Control 2
9	FE2_TRIG_ DPWM1_EN	R/W	0	Enables Sample Trigger from DPWM 1 to Front End Control 2 0 = DPWM 1 Sample Trigger not routed to Front End Control 2 (Default) 1 = DPWM 1 Sample Trigger routed to Front End Control 2
8	FE2_TRIG_ DPWM0_EN	R/W	0	Enables Sample Trigger from DPWM 0 to Front End Control 2 0 = DPWM 0 Sample Trigger not routed to Front End Control 2 (Default) 1 = DPWM 0 Sample Trigger routed to Front End Control 2
7	FE1_TRIG_ DPWM3_EN	R/W	0	Enables Sample Trigger from DPWM 3 to Front End Control 1 0 = DPWM 3 Sample Trigger not routed to Front End Control 1 (Default) 1 = DPWM 3 Sample Trigger routed to Front End Control 1
6	FE1_TRIG_ DPWM2_EN	R/W	0	Enables Sample Trigger from DPWM 2 to Front End Control 1 0 = DPWM 2 Sample Trigger not routed to Front End Control 1 (Default) 1 = DPWM 2 Sample Trigger routed to Front End Control 1
5	FE1_TRIG_ DPWM1_EN	R/W	0	Enables Sample Trigger from DPWM 1 to Front End Control 1 0 = DPWM 1 Sample Trigger not routed to Front End Control 1 (Default) 1 = DPWM 1 Sample Trigger routed to Front End Control 1
4	FE1_TRIG_ DPWM0_EN	R/W	0	Enables Sample Trigger from DPWM 0 to Front End Control 1 0 = DPWM 0 Sample Trigger not routed to Front End Control 1 (Default) 1 = DPWM 0 Sample Trigger routed to Front End Control 1
3	FE0_TRIG_ DPWM3_EN	R/W	0	Enables Sample Trigger from DPWM 3 to Front End Control 0 0 = DPWM 3 Sample Trigger not routed to Front End Control 0 (Default) 1 = DPWM 3 Sample Trigger routed to Front End Control 0
2	FE0_TRIG_ DPWM2_EN	R/W	0	Enables Sample Trigger from DPWM 2 to Front End Control 0 0 = DPWM 2 Sample Trigger not routed to Front End Control 0 (Default) 1 = DPWM 2 Sample Trigger routed to Front End Control 0
1	FE0_TRIG_ DPWM1_EN	R/W	0	Enables Sample Trigger from DPWM 1 to Front End Control 0 0 = DPWM 1 Sample Trigger not routed to Front End Control 0 (Default) 1 = DPWM 1 Sample Trigger routed to Front End Control 0
0	FE0_TRIG_ DPWM0_EN	R/W	0	Enables Sample Trigger from DPWM 0 to Front End Control 0 0 = DPWM 0 Sample Trigger not routed to Front End Control 0 (Default) 1 = DPWM 0 Sample Trigger routed to Front End Control 0

4.1.5 External DAC Control Register (EXTDACCTRL)

Address 00120010

Figure 4-5. External DAC Control Register (EXTDACCTRL)

26–24	23–19	18–16
DAC2_SEL	Reserved	DAC1_SEL
R/W-000	R/W-0 0000	R/W-000

15–11	10–8	7–3	2	1	0
Reserved	DAC0_SEL	Reserved	EXT_DAC2_EN	EXT_DAC1_EN	EXT_DAC0_EN
R-0 0000	R/W-000	R-0 0000	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-5. External DAC Control Register (EXTDACCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
26-24	DAC2_SEL	R/W	000	Configures DAC 2 setpoint in External DAC Mode 0 = DAC 0 Setpoint Selected (Default) 1 = DAC 1 Setpoint Selected 3 = Output of Constant Power Module Selected 4 = Filter 0 Output Selected 5 = Filter 1 Output Selected 6 = Filter 2 Output Selected
23-19	Reserved	R	0 0000	
18-16	DAC1_SEL	R/W	000	Configures DAC 1 setpoint in External DAC Mode 0 = DAC 0 Setpoint Selected (Default) 2 = DAC 2 Setpoint Selected 3 = Output of Constant Power Module Selected 4 = Filter 0 Output Selected 5 = Filter 1 Output Selected 6 = Filter 2 Output Selected
15-11	Reserved	R	0 0000	
10-8	DAC0_SEL	R/W	000	Configures DAC 0 setpoint in External DAC Mode 1 = DAC 1 Setpoint Selected 2 = DAC 2 Setpoint Selected 3 = Output of Constant Power Module Selected 4 = Filter 0 Output Selected 5 = Filter 1 Output Selected 6 = Filter 2 Output Selected
7-3	Reserved	R	0 0000	
2	EXT_DAC2_EN	R/W	0	External DAC 1 Mode Enable 0 = External DAC Mode disabled. DAC 1 setpoint driven from Front End Control Module (Default) 1 = External DAC Mode enabled, DAC 1 setpoint driven by DAC1_SEL configuration
1	EXT_DAC1_EN	R/W	0	External DAC 1 Mode Enable 0 = External DAC Mode disabled. DAC 1 setpoint driven from Front End Control Module (Default) 1 = External DAC Mode enabled, DAC 1 setpoint driven by DAC1_SEL configuration
0	EXT_DAC0_EN	R/W	0	External DAC 0 Mode Enable 0 = External DAC Mode disabled. DAC 0 setpoint driven from Front End Control Module (Default) 1 = External DAC Mode enabled, DAC 0 setpoint driven by DAC0_SEL configuration

4.1.6 Filter Mux Register (FILTERMUX)

Address 00120014

Figure 4-6. Filter Mux Register (FILTERMUX)

29	28	27	26	25	24
FILTER2_KCOMP_SEL		FILTER1_KCOMP_SEL		FILTER0_KCOMP_SEL	
R/W-00		R/W-00		R/W-00	

23	19	18	17	16
Reserved		FILTER2_FFWD_SEL	FILTER1_FFWD_SEL	FILTER0_FFWD_SEL
R-0 0000		R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8
Reserved		FILTER2_PER_SEL		FILTER1_PER_SEL		FILTER0_PER_SEL	
R-00		R/W-00		R/W-00		R/W-00	

7	6	5	4	3	2	1	0
Reserved		FILTER2_FE_SEL		FILTER1_FE_SEL		FILTER0_FE_SEL	
R-00		R/W-10		R/W-01		R/W-00	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-6. Filter Mux Register (FILTERMUX) Register Field Descriptions

Bit	Field	Type	Reset	Description
29-28	FILTER2_KCOMP_SEL	R/W	00	Selects KComp value routed to Filter 2 Module 0 = KComp 0 Value Selected (Default) 1 = KComp 1 Value Selected 2 = KComp 2 Value Selected
27-26	FILTER1_KCOMP_SEL	R/W	00	Selects KComp value routed to Filter 1 Module 0 = KComp 0 Value Selected (Default) 1 = KComp 1 Value Selected 2 = KComp 2 Value Selected
25-24	FILTER0_KCOMP_SEL	R/W	00	Selects KComp value routed to Filter 0 Module 0 = KComp 0 Value Selected (Default) 1 = KComp 1 Value Selected 2 = KComp 2 Value Selected
23-19	Reserved	R	0 0000	
18	FILTER2_FFWD_SEL	R/W	0	Configures Feedforward value routed to Filter 2 Module 0 = Filter 0 Output Selected (Default) 1 = Filter 1 Output Selected
17	FILTER1_FFWD_SEL	R/W	0	Configures Feedforward value routed to Filter 1 Module 0 = Filter 0 Output Selected (Default) 1 = Filter 2 Output Selected
16	FILTER0_FFWD_SEL	R/W	0	Configures Feedforward value routed to Filter 0 Module 0 = Filter 1 Output Selected (Default) 1 = Filter 2 Output Selected
15-14	Reserved	R	00	
13-12	FILTER2_PER_SEL	R/W	00	Selects source of switching cycle period for Filter 2 Module 0 = DPWM 0 Switching Period (Default) 1 = DPWM 1 Switching Period 2 = DPWM 2 Switching Period 3 = DPWM 3 Switching Period

Table 4-6. Filter Mux Register (FILTERMUX) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	FILTER1_PER_SEL	R/W	00	Selects source of switching cycle period for Filter 1 Module 0 = DPWM 0 Switching Period (Default) 1 = DPWM 1 Switching Period 2 = DPWM 2 Switching Period 3 = DPWM 3 Switching Period
9-8	FILTER0_PER_SEL	R/W	00	Selects source of switching cycle period for Filter 0 Module 0 = DPWM 0 Switching Period (Default) 1 = DPWM 1 Switching Period 2 = DPWM 2 Switching Period 3 = DPWM 3 Switching Period
7-6	Reserved	R		
5-4	FILTER2_FE_SEL	R/W	10	Selects which Front End Module provides data for Filter 2 Module 0 = Front End Module 0 provides data to Filter 1 = Front End Module 1 provides data to Filter 2 = Front End Module 2 provides data to Filter (Default)
3-2	FILTER1_FE_SEL	R/W	01	Selects which Front End Module provides data for Filter 1 Module 0 = Front End Module 0 provides data to Filter 1 = Front End Module 1 provides data to Filter (Default) 2 = Front End Module 2 provides data to Filter
1-0	FILTER0_FE_SEL	R/W	00	Selects which Front End Module provides data for Filter 0 Module 0 = Front End Module 0 provides data to Filter (Default) 1 = Front End Module 1 provides data to Filter 2 = Front End Module 2 provides data to Filter

4.1.7 Filter KComp A Register (FILTERKCOMPA)

Address 00120018

Figure 4-7. Filter KComp A Register (FILTERKCOMPA)

29 16	15 14	13 0
KCOMP1	Reserved	KCOMP0
R/W-00 0000 0000 0000	R-00	R/W-00 0000 0111 1101

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-7. Filter KComp A Register (FILTERKCOMPA) Register Field Descriptions

Bit	Field	Type	Reset	Description
29-16	KCOMP1	R/W	00 0000 0000 0000	14-bit value used in filter output calculations replacing the DPWM switching period value
15-14	Reserved	R	00	
13-0	KCOMP0	R/W	00 0000 0111 1101	14-bit value used in filter output calculations replacing the DPWM switching period value

4.1.8 Filter KComp B Register (FILTERKCOMPB)

Address 0012001C

Figure 4-8. Filter KComp B Register (FILTERKCOMPB)

13		0
KCOMP2		
R/W-00 0000 0000 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-8. Filter KComp B Register (FILTERKCOMPB) Register Field Descriptions

Bit	Field	Type	Reset	Description
13-0	KCOMP2	R/W	00 0000 0000 0000	14-bit value used in filter output calculations replacing the DPWM switching period value

4.1.9 DPWM Mux Register (DPWMMUX)

Address 00120020

Figure 4-9. DPWM Mux Register (DPWMMUX)

31	30	29	28	27	26	25	24
DPWM3_SYNC_FET_SEL		DPWM2_SYNC_FET_SEL		DPWM1_SYNC_FET_SEL		DPWM0_SYNC_FET_SEL	
R/W-00		R/W-00		R/W-00		R/W-00	
23	22	21	20	19	18	17	16
Reserved				DPWM3_SYNC_SEL		DPWM2_SYNC_SEL	
R-0000				R/W-00		R/W-00	
15	14	13	12	11	10	9	8
DPWM1_SYNC_SEL		DPWM0_SYNC_SEL		DPWM3_FILTER_SEL			DPWM2_FILTER_SEL
R/W-00		R/W-00		R/W-000			R/W-010
7	6	5	4	3	2	1	0
DPWM2_FILTER_SEL		DPWM1_FILTER_SEL		DPWM0_FILTER_SEL			
R/W-010		R/W-001		R/W-000			

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-9. DPWM Mux Register (DPWMMUX) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DPWM3_SYNC_FET_SEL	R/W	00	Selects Ramp source for DPWM3 PWM-B SyncFET soft on/off 0 = Front End 0 Ramp output selected (Default) 1 = Front End 1 Ramp output selected 2 = Front End 2 Ramp output selected
29-28	DPWM2_SYNC_FET_SEL	R/W	00	Selects Ramp source for DPWM2 PWM-B SyncFET soft on/off 0 = Front End 0 Ramp output selected (Default) 1 = Front End 1 Ramp output selected 2 = Front End 2 Ramp output selected
27-26	DPWM1_SYNC_FET_SEL	R/W	00	Selects Ramp source for DPWM1 PWM-B SyncFET soft on/off 0 = Front End 0 Ramp output selected (Default) 1 = Front End 1 Ramp output selected 2 = Front End 2 Ramp output selected
25-24	DPWM0_SYNC_FET_SEL	R/W	00	Selects Ramp source for DPWM0 PWM-B SyncFET soft on/off 0 = Front End 0 Ramp output selected (Default) 1 = Front End 1 Ramp output selected 2 = Front End 2 Ramp output selected
23-20	Reserved	R	0000	
19-18	DPWM3_SYNC_SEL	R/W	00	Selects Master Sync for DPWM 3 when DPWM 3 configured in slave mode 0 = DPWM 0 Sync (Default) 1 = DPWM 1 Sync 2 = DPWM 2 Sync 3 = DPWM 3 Sync
17-16	DPWM2_SYNC_SEL	R/W	00	Selects Master Sync for DPWM 2 when DPWM 2 configured in slave mode 0 = DPWM 0 Sync (Default) 1 = DPWM 1 Sync 2 = DPWM 2 Sync 3 = DPWM 3 Sync
15-14	DPWM1_SYNC_SEL	R/W	00	Selects Master Sync for DPWM 1 when DPWM 1 configured in slave mode 0 = DPWM 0 Sync (Default) 1 = DPWM 1 Sync 2 = DPWM 2 Sync 3 = DPWM 3 Sync

Table 4-9. DPWM Mux Register (DPWMMUX) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	DPWM0_SYNC_SEL	R/W	00	Selects Master Sync for DPWM 0 when DPWM 0 configured in slave mode 0 = DPWM 0 Sync (Default) 1 = DPWM 1 Sync 2 = DPWM 2 Sync 3 = DPWM 3 Sync
11-9	DPWM3_FILTER_SEL	R/W	000	Selects source of duty cycle/resonant period for DPWM Module 3 0 = Filter 0 Output Selected (Default) 1 = Filter 1 Output Selected 2 = Filter 2 Output Selected 3 = Constant Power Module Selected 4 = DPWM_ON_TIME value from Light Load Control Register
8-6	DPWM2_FILTER_SEL	R/W	010	Selects source of duty cycle/resonant period for DPWM Module 2 0 = Filter 0 Output Selected 1 = Filter 1 Output Selected 2 = Filter 2 Output Selected (Default) 3 = Constant Power Module Selected 4 = DPWM_ON_TIME value from Light Load Control Register
5-3	DPWM1_FILTER_SEL	R/W	001	Selects source of duty cycle/resonant period for DPWM Module 1 0 = Filter 0 Output Selected 1 = Filter 1 Output Selected (Default) 2 = Filter 2 Output Selected 3 = Constant Power Module Selected 4 = DPWM_ON_TIME value from Light Load Control Register
2-0	DPWM0_FILTER_SEL	R/W	000	Selects source of duty cycle/resonant period for DPWM Module 0 0 = Filter 0 Output Selected (Default) 1 = Filter 1 Output Selected 2 = Filter 2 Output Selected 3 = Constant Power Module Selected 4 = DPWM_ON_TIME value from Light Load Control Register

4.1.10 Constant Power Control Register (CPCTRL)

Address 00120024

Figure 4-10. Constant Power Control Register (CPCTRL)

16	15	14	13	12	11	10	9	8
CCPC_INT_EN	DAC_COMP_EN	FW_DIVISOR_EN	LOWER_COMP_EN	VLOOP_FREEZE_EN	VLOOP_SEL		CLOOP_SEL	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-00		R/W-00	

7	6	5	4	3	2	1	0
THRESH_SEL			DIVISOR_SEL		CPCC_CONFIG		CPCC_EN
R/W-000			R/W-00		R/W-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-10. Constant Power Control Register (CPCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
16	CCPC_INT_EN	R/W	0	Constant Power/Constant Current Interrupt Enable 0 = Interrupt disabled on mode switches (Default) 1 = Interrupt enabled on mode switches
15	DAC_COMP_EN	R/W	0	Enables comparison of DAC Setpoint and quotient of Max Power/Sense Current in Loop Switching Mode. Minimum of DAC setpoint and calculated quotient sets voltage loop setpoint in Constant Voltage and Constant Power modes 0 = Operating Mode controls Voltage Loop DAC Setpoint (Default) 1 = Minimum of DAC setpoint and calculated quotient used as Voltage Loop DAC Setpoint
14	FW_DIVISOR_EN	R/W	0	Enables Firmware value for divisor in Constant Power calculations 0 = Divisor selected by DIVISOR_SEL (Bits 7:6) (Default) 1 = Divisor driven by Firmware Current Register
13	LOWER_COMP_EN	R/W	0	Enables output of lowest duty from current or voltage loop when Constant Power/Constant Current module controls loop output 0 = Loop output controlled by mode selection, voltage loop selected in constant voltage and constant power mode, current loop selected in constant current mode (Default) 1 = Loop output controlled by lowest duty from voltage or current loops
12	VLOOP_FREEZE_EN	R/W	0	Enables freezing of Voltage Loop Integrator when current loop selected in Loop Switching configuration 0 = Freezing of Voltage Loop Integrator disabled (Default) 1 = Freezing of Voltage Loop Integrator enabled
11-10	VLOOP_SEL	R/W	00	Configures voltage loop for loop switching mode 0 = Filter 0 Output Selected (Default) 1 = Filter 1 Output Selected 2 = Filter 2 Output Selected
9-8	CLOOP_SEL	R/W	00	Configures current loop for loop switching mode 0 = Filter 0 Output Selected (Default) 1 = Filter 1 Output Selected 2 = Filter 2 Output Selected
7-5	THRESH_SEL	R/W	000	Configures input threshold selected for use in Constant Power comparison 0 = Filter 0 Output Selected (Default) 1 = Filter 1 Output Selected 2 = Filter 2 Output Selected 3 = Front End 0 Absolute Value Data Selected 4 = Front End 1 Absolute Value Data Selected 5 = Front End 2 Absolute Value Data Selected

Table 4-10. Constant Power Control Register (CPCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	DIVISOR_SEL	R/W	00	Configures value used for divisor in Constant Power calculations 0 = Front End 0 Absolute Value Data Selected (Default) 1 = Front End 1 Absolute Value Data Selected 2 = Front End 2 Absolute Value Data Selected
2-1	CPCC_CONFIG	R/W	0	Controls Constant Power/Constant Current module configuration 0 = Average Current Mode (Default) 1 = Constant Power Module controls selection of voltage/current loop 2 = Constant Power Module error switching mode
0	CPCC_EN	R/W	0	Constant Power Constant/Current Module Enable 0 = Constant Power/Constant Current Module disabled (Default) 1 = Constant Power/Constant Current Module enabled

4.1.11 Constant Power Nominal Threshold Register (CPNOM)

Address 00120028

Figure 4-11. Constant Power Nominal Threshold Register (CPNOM)

25 16	15 10	9 0
NOM_CURRENT_UPPER	Reserved	NOM_CURRENT_LOWER
R/W-00 0000 0000	R-00 0000	R/W-00 0000 0000

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-11. Constant Power Nominal Threshold Register (CPNOM) Register Field Descriptions

Bit	Field	Type	Reset	Description
25-16	NOM_CURRENT_UPPER	R/W	00 0000 0000	Configures INOM value used in Constant Power/Constant Current Calculations, when sensed value exceeds NOM_CURRENT_UPPER in Constant Voltage mode, setpoint will switch to Constant Power mode
15-10	Reserved	R	00 0000	
9-0	NOM_CURRENT_LOWER	R/W	00 0000 0000	Configures INOM value used in Constant Power/Constant Current Calculations, when sensed value falls below NOM_CURRENT_LOWER in Constant Power mode, setpoint will switch to Constant Voltage mode

4.1.12 Constant Power Max Threshold Register (CPMAX)

Address 0012002C

Figure 4-12. Constant Power Max Threshold Register (CPMAX)

25	16	15	10	9	0
MAX_CURRENT_UPPER		Reserved		MAX_CURRENT_LOWER	
R/W-00 0000 0000		R-00 0000		R/W-00 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-12. Constant Power Max Threshold Register (CPMAX) Register Field Descriptions

Bit	Field	Type	Reset	Description
25-16	MAX_CURRENT_UPPER	R/W	00 0000 0000	Configures IMAX value used in Constant Power/Constant Current Calculations, when sensed value exceeds MAX_CURRENT_UPPER in Constant Power mode, setpoint will switch to Max Current mode
15-10	Reserved	R	00 0000	
9-0	MAX_CURRENT_LOWER	R/W	00 0000 0000	Configures IMAX value used in Constant Power/Constant Current Calculations, when sensed value falls below MAX_CURRENT_LOWER in Max Current mode, setpoint will switch to Constant Power mode

4.1.13 Constant Power Configuration Register (CPCONFIG)

Address 00120030

Figure 4-13. Constant Power Configuration Register (CPCONFIG)

25 16	15 10	9 0
MAX_CURRENT	Reserved	NOM_VOLTAGE
R/W-00 0000 0000	R-00 0000	R/W-00 0000 0000

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-13. Constant Power Configuration Register (CPCONFIG) Register Field Descriptions

Bit	Field	Type	Reset	Description
25-16	MAX_CURRENT	R/W	00 0000 0000	Configures I_{MAX} setpoint used in Constant Power/Constant Current Calculations in Max Current mode
15-10	Reserved	R	00 0000	
9-0	NOM_VOLTAGE	R/W	00 0000 0000	Configures V_{NOM} setpoint used in Constant Power/Constant Current Calculations in Constant Voltage mode (Loop Oring configuration selected)

4.1.14 Constant Power Max Power Register (CPMAXPWR)

Address 00120034

Figure 4-14. Constant Power Max Power Register (CPMAXPWR)

19	0
MAX_POWER	
R/W-0000 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-14. Constant Power Max Power Register (CPMAXPWR) Register Field Descriptions

Bit	Field	Type	Reset	Description
19-0	MAX_POWER	R/W	0000 0000 0000 0000 0000	Configures P_{MAX} value used in Constant Power/Constant Current calculations in Constant Power mode

4.1.15 Constant Power Integrator Threshold Register (CPINTTHRESH)

Address 00120038

Figure 4-15. Constant Power Integrator Threshold Register (CPINTTHRESH)

23		0
INT_THRESH		
R/W-0000 0000 0000 0000 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-15. Constant Power Integrator Threshold Register (CPINTTHRESH) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	INT_THRESH	R/W	0000 0000 0000 0000 0000	24-bit signed value added to Current Loop Duty value to determine when to freeze Current Loop Integrator

4.1.16 Constant Power Firmware Divisor Register (CPFWDIVISOR)

Address 0012003C

Figure 4-16. Constant Power Firmware Divisor Register (CPFWDIVISOR)

9	0
FW_DIVISOR	
R/W-00 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-16. Constant Power Firmware Divisor Register (CPFWDIVISOR) Register Field Descriptions

Bit	Field	Type	Reset	Description
9-0	FW_DIVISOR	R/W	00 0000 0000	10-bit value used in Constant Power calculation when firmware value is selected in Bit 17 of Constant Power Control Register

4.1.17 Constant Power Status Register (CPSTAT)

Address 00120040

Figure 4-17. Constant Power Status Register (CPSTAT)

8	7	6	5	4	3	2	1	0
CONSTANT_CUR	CONSTANT_PWR	CONSTANT_VOLT	CC_TO_CV_INT	CV_TO_CC_INT	CC_TO_CP_INT	CP_TO_CC_INT	CP_TO_CV_INT	CV_TO_CP_INT
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-17. Constant Power Status Register (CPSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CONSTANT_CUR	R	0	Constant Current Mode Indication 0 = Constant Current Mode not enabled 1 = Constant Current Mode enabled
7	CONSTANT_PWR	R	0	Constant Power Mode Indication 0 = Constant Power Mode not enabled 1 = Constant Power Mode enabled
6	CONSTANT_VOLT	R	0	Constant Voltage Mode Indication 0 = Constant Voltage Mode not enabled 1 = Constant Voltage Mode enabled
5	CC_TO_CV_INT	R	0	Constant Current Mode to Constant Voltage Mode latched status, cleared on read 0 = No transition from Constant Current to Constant Voltage detected 1 = Transition from Constant Current to Constant Voltage detected
4	CV_TO_CC_INT	R	0	Constant Voltage Mode to Constant Current Mode latched status, cleared on read 0 = No transition from Constant Voltage to Constant Current detected 1 = Transition from Constant Voltage to Constant Current detected
3	CC_TO_CP_INT	R	0	Constant Current Mode to Constant Power Mode latched status, cleared on read 0 = No transition from Constant Current to Constant Power detected 1 = Transition from Constant Current to Constant Power detected
2	CP_TO_CC_INT	R	0	Constant Power Mode to Constant Current Mode latched status, cleared on read 0 = No transition from Constant Power to Constant Current detected 1 = Transition from Constant Power to Constant Current detected
1	CP_TO_CV_INT	R	0	Constant Power Mode to Constant Voltage Mode latched status, cleared on read 0 = No transition from Constant Power to Constant Voltage detected 1 = Transition from Constant Power to Constant Voltage detected
0	CV_TO_CP_INT	R	0	Constant Voltage Mode to Constant Power Mode latched status, cleared on read 0 = No transition from Constant Voltage to Constant Power detected 1 = Transition from Constant Voltage to Constant Power detected

4.1.18 Cycle Adjustment Control Register (CYCADJCTRL)

Address 00120044

Figure 4-18. Cycle Adjustment Control Register (CYCADJCTRL)

9 7	6 5	4 3	2 1	0
CYC_ADJ_GAIN	CYC_ADJ_SYNC	SECOND_SAMPLE_SEL	FIRST_SAMPLE_SEL	CYC_ADJ_EN
R/W-000	R/W-00	R/W-00	R/W-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-18. Cycle Adjustment Control Register (CYCADJCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
9-7	CYC_ADJ_GAIN	R/W	000	Configures gain of Cycle Adjustment calculation 0 = 1x gain (Default) 1 = 2x gain 2 = 4x gain 3 = 8x gain 4 = 16x gain 5 = 32x gain 6 = 64x gain 7 = 128x gain
6-5	CYC_ADJ_SYNC	R/W	00	Selects which DPWM A trigger synchronizes cycle adjustment calculation, first 2 samples after receipt of DPWM A trigger will be used for Cycle Adjustment Calculation. 0 = DPWM-1A trigger selected (Default) 1 = DPWM-2A trigger selected 2 = DPWM-3A trigger selected 3 = DPWM-4A trigger selected
4-3	SECOND_SAMPLE_SEL	R/W	00	Configures Front End Module Data used for Second Sample of Cycle Adjustment Calculation 0 = Front End Module 0 Error Data selected (Default) 1 = Front End Module 1 Error Data selected 2 = Front End Module 2 Error Data selected
2-1	FIRST_SAMPLE_SEL	R/W	00	Configures Front End Module Data used for First Sample of Cycle Adjustment Calculation 0 = Front End Module 0 Error Data selected (Default) 1 = Front End Module 1 Error Data selected 2 = Front End Module 2 Error Data selected
0	CYC_ADJ_EN	R/W	0	Cycle Adjustment Calculation Enable 0 = Cycle Adjustment Calculation disabled (Default) 1 = Cycle Adjustment Calculation enabled

4.1.19 Cycle Adjustment Limit Register (CYCADJLIM)

Address 00120048

Figure 4-19. Cycle Adjustment Limit Register (CYCADJLIM)

28	16	15	13	12	0
CYC_ADJ_UPPER_LIMIT		Reserved		CYC_ADJ_LOWER_LIM	
R/W-0 0000 0000 0000		R-000		R/W-0 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-19. Cycle Adjustment Limit Register (CYCADJLIM) Register Field Descriptions

Bit	Field	Type	Reset	Description
28-16	CYC_ADJ _UPPER_LIMIT	R/W	0 0000 0000 0000	Cycle Adjustment Calculation signed upper limit value, output of Cycle Adjustment Calculation is clamped at the upper limit, if calculated result exceeds the upper limit. LSB resolution equals High Frequency Oscillator period/16.
15-13	Reserved	R	000	
12-0	CYC_ADJ _LOWER_LIM	R/W	0 0000 0000 0000	Cycle Adjustment Calculation signed lower limit value, output of Cycle Adjustment Calculation is clamped at the lower limit, if calculated result falls below the lower limit. LSB resolution equals High Frequency Oscillator period/16.

4.1.20 Cycle Adjustment Status Register (CYCADJSTAT)

Address 0012004C

Figure 4-20. Cycle Adjustment Status Register (CYCADJSTAT)

28 16	15 10	9 0
CYC_ADJ_CALC	Reserved	CYC_ADJ_ERROR
R-0	R-00 0000	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-20. Cycle Adjustment Status Register (CYCADJSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
28-16	CYC_ADJ_CALC	R	0	13-bit signed value representing calculated Cycle Adjustment provided to DPWM module based on first 2 error samples
15-10	Reserved	R	00 0000	
9-0	CYC_ADJ _ERROR	R	0	10-bit signed value representing calculated error of the first 2 error samples received

4.1.21 Global Enable Register (GLBEN)

Address 00120050

Figure 4-21. Global Enable Register (GLBEN)

10	9	8	7 4	3	2	1	0
FE_CTRL2_EN	FE_CTRL1_EN	FE_CTRL0_EN	Reserved	DPWM3_EN	DPWM2_EN	DPWM1_EN	DPWM0_EN
R/W-0	R/W-0	R/W-0	R-0000	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-21. Global Enable Register (GLBEN) Register Field Descriptions

Bit	Field	Type	Reset	Description
10	FE_CTRL2_EN	R/W	0	Global Firmware Enable for Front End Control 2 Module 0 = Front End Control 2 Module Disabled (Default) 1 = Front End Control 2 Module Enabled
9	FE_CTRL1_EN	R/W	0	Global Firmware Enable for Front End Control 1 Module 0 = Front End Control 1 Module Disabled (Default) 1 = Front End Control 1 Module Enabled
8	FE_CTRL0_EN	R/W	0	Global Firmware Enable for Front End Control 0 Module 0 = Front End Control 0 Module Disabled (Default) 1 = Front End Control 0 Module Enabled
7-4	Reserved	R	0000	
3	DPWM3_EN	R/W	0	Global Firmware Enable for DPWM 3 Module 0 = DPWM 3 Module Disabled (Default) 1 = DPWM 3 Module Enabled
2	DPWM2_EN	R/W	0	Global Firmware Enable for DPWM 2 Module 0 = DPWM 2 Module Disabled (Default) 1 = DPWM 2 Module Enabled
1	DPWM1_EN	R/W	0	Global Firmware Enable for DPWM 1 Module 0 = DPWM 1 Module Disabled (Default) 1 = DPWM 1 Module Enabled
0	DPWM0_EN	R/W	0	Global Firmware Enable for DPWM 0 Module 0 = DPWM 0 Module Disabled (Default) 1 = DPWM 0 Module Enabled

4.1.22 PWM Global Period Register (PWMGLBPRD)

Address 00120054

Figure 4-22. PWM Global Period Register (PWMGLBPRD)

17	4	3	0
PRD		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-22. PWM Global Period Register (PWMGLBPRD) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	PRD	R/W	00 0000 0000 0000	Global PWM Period value, overriding DPWM Period settings when global PWM period is selected within each DPWM module
3-0	Reserved	R	0000	

4.1.23 Sync Control Register (SYNCCTRL)

Address 00120058

Figure 4-23. Sync Control Register (SYNCCTRL)

5	4	2	1	0
SYNC_IN	SYNC_MUX_SEL		SYNC_OUT	SYNC_DIR
R-0	R/W-001		R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-23. Sync Control Register (SYNCCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
5	SYNC_IN	R	0	Value of Sync pin 0 = Logic level low present on Sync pin 1 = Logic level high present on Sync pin
4-2	SYNC_MUX_SEL	R/W	001	Selects which module controls Sync pin output 000 = DPWM 0 Sync Output (Default) 001 = DPWM 1 Sync Output 010 = DPWM 2 Sync Output 011 = DPWM 3 Sync Output 100 = Value from SYNC_OUT (Bit 1) 101 = Value specified by CLKSR in CLKCNTL (See Section 4.18.1) 110 = Low-Frequency Oscillator Clock Output 111 = Driven low
1	SYNC_OUT	R/W	1	Configure output value for Sync pin, if used as an output 0 = Sync pin driven low in output mode 1 = Sync pin driven high in output mode (Default)
0	SYNC_DIR	R/W	1	Configure direction of Sync pin 0 = Sync pin configured as an output pin 1 = Sync pin configured as an input pin (Default)

4.1.24 Light Load Control Register (LLCTRL)

Address 0012005C

Figure 4-24. Light Load Control Register (LLCTRL)

25							8
DPWM_ON_TIME							
R/W-00 0000 0000 0000 0000							
7	6	5	4	3	2	1	0
Reserved				CYCLE_CNT_EN	LL_FILTER_SEL		LL_EN
R-0000				R/W-0	R/W-00		R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-24. Light Load Control Register (LLCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
25-8	DPWM_ON_TIME	R/W	00 0000 0000 0000 0000	DPWM pulse width used for EADC-based light load mode operation, when selected Filter data exceeds TURN_ON_THRESH value
7-4	Reserved	R	0000	
3	CYCLE_CNT_EN	R/W	0	Enables Switching Cycle Counter for enabling constant pulse widths when configured in Light Load operation 0 = Switching Cycle Counter disabled (Default) 1 = Switching Cycle Counter enabled
2-1	LL_FILTER_SEL	R/W	00	Configures source of filter data for Light Load comparisons 0 = Filter 0 data selected (Default) 1 = Filter 1 data selected 2 = Filter 2 data selected
0	LL_EN	R/W	0	EADC-based Light Load Mode Enable 0 = Light Load Mode disabled (Default) 1 = Light Load Mode enabled

4.1.25 Light Load Enable Threshold Register (LLENTHRESH)

Address 00120060

Figure 4-25. Light Load Enable Threshold Register (LLENTHRESH)

31	24	23	18	17	0
CYCLE_CNT_THRESH		Reserved		TURN_ON_THRESH	
R/W-0000 0000		R-0000 00		R/W-00 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-25. Light Load Enable Threshold Register (LLENTHRESH) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CYCLE_CNT _THRESH	R/W	0000 0000	Switching Cycle threshold where constant width DPWM pulses are enabled when number of switching cycles without pulses exceeds threshold
23-18	Reserved	R	0000 00	
17-0	TURN_ON _THRESH	R/W	00 0000 0000 000 0000	Filter data threshold where constant width DPWM pulses are enabled when filter data exceeds threshold

4.1.26 Light Load Disable Threshold Register (LLDISTHRESH)

Address 00120064

Figure 4-26. Light Load Disable Threshold Register (LLDISTHRESH)

17		0
TURN_OFF_THRESH		
R/W-00 0000 0000 0000 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-26. Light Load Disable Threshold Register (LLDISTHRESH) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-0	TURN_OFF _THRESH	R/W	00 0000 0000 0000 0000	Filter data threshold where constant width DPWM pulses are disabled when filter data falls below threshold

4.1.27 Analog Peak Current Mode Control Register (APCMCTRL)

Address 00120070

Figure 4-27. Analog Peak Current Mode Control Register (APCMCTRL)

5	4	3	2	1	0
PCM_FILTER_SEL		PCM_LATCH_EN	PCM_FE_SEL		PCM_EN
R/W-00		R/W-0	R/W-00		R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-27. Analog Peak Current Mode Control Register (APCMCTRL)Register Field Descriptions

Bit	Field	Type	Reset	Description
5-4	PCM_FILTER_SEL	R/W	00	Selects source of Peak Current Slope Compensation Ramp Start 0 = Filter 0 data selected (Default) 1 = Filter 1 data selected 2 = Filter 2 data selected 3 = Constant Power/Constant Current data selected
3	PCM_LATCH_EN	R/W	0	Enables latching of Peak Current Flag to end of frame 0 = PCM Flag is not latched to end of PCM Frame (Default) 1 = PCM Flag is latched to end of PCM Frame
2-1	PCM_FE_SEL	R/W	00	Selects source of Front End Comparator output for Analog Peak Current Mode Control 0 = Front End Control 0 Comparator output selected (Default) 1 = Front End Control 1 Comparator output selected 2 = Front End Control 2 Comparator output selected
0	PCM_EN	R/W	0	Analog Peak Current Mode Control Module Enable 0 = Analog Peak Current Mode Control Module disabled (Default) 1 = Analog Peak Current Mode Control Module enabled

4.1.28 DTC Control Register (DTCCTRL)

Address 00120078

Figure 4-28. DTC Control Register (DTCCTRL)

22	21	20	19	17	16
FLT_INT_EN	FLT_MAX		FLT_STEP		FLT_THRESH
R/W-0	R/W-0		R/W-0		R/W-0

15	13	12	9	8	5	4	3	2	1	0
FLT_THRESH		PWM_A_SEL		PWM_B_SEL		A_POL	B_POL	INPUT_MODE	MODE	DTC_EN
R/W-0		R/W-0		R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-28. DTC Control Register (DTCCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
22	FLT_IN_EN	R/W	0	Enables interrupt generation when a fault flag condition has been met 0 = Interrupt disabled (default) 1 = Interrupt enabled
21-20	FLT_MAX	R/W	0	Sets the number of consecutive detected faults before a fault step is utilized 0 = 1 (default) 1 = 2 2 = 4 3 = 8
19-17	FLT_STEP	R/W	0	Sets the negative step size when a fault condition is detected that exceeds the fault max value. If the fault_max condition has not been met the step size is -1. Step size is in HFO clock increments. 0 = -1 (default) 1 = -5 2 = -10 3 = -25 4 = -50 5 = -75 6 = -100 7 = -125
16-13	FLT_THRESH	R/W	0	Sets the measurement threshold for a fault condition to initiate a fault step. Threshold is in HFO clock increments.
12-9	PWM_A_SEL	R/W	0	Selects the phase A negative edge reference to begin a measurement window 0 = Disabled (Default) 1 = DPWM-0-A 2 = DPWM-1-A 3 = DPWM-2-A 4 = DPWM-3-A 5 = DPWM-0-B 6 = DPWM-1-B 7 = DPWM-2-B 8 = DPWM-3-B

Table 4-28. DTC Control Register (DTCCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-5	PWM_B_SEL	R/W	0	Selects the phase B negative edge reference to begin a measurement window 0 = Disabled (Default) 1 = DPWM-0-A 2 = DPWM-1-A 3 = DPWM-2-A 4 = DPWM-3-A 5 = DPWM-0-B 6 = DPWM-1-B 7 = DPWM-2-B 8 = DPWM-3-B
4	A_POL	R/W	0	Sets the signal polarity of the DTC input to the device 0 = Active Low (Default) 1 = Active High
3	B_POL	R/W	0	Sets the signal polarity of the DTC input to the device 0 = Active Low (Default) 1 = Active High
2	INPUT_MODE	R/W	0	Sets the input method for the DTC module 0 = Phase A and Phase B input signals occur on separate inputs (Default) 1 = Phase A and Phase B input signals occur on the same input
1	MODE	R/W	0	Sets mode control of the DTC phase accumulator values 0 = Automatic Mode. Accumulators A and B are changed by hardware and stay within limits programmed in the DTCLIMIT register. (Default) 1 = Manual Mode. Accumulator A and B set by programmed values in the DTCMANUAL register.
0	DTC_EN	R/W	0	DTC Enable 0 = Dead-time Compensate Module disabled (Default) 1 = Dead-time Compensate Module enabled

4.1.29 DTC Target Register (DTCTARGET)

Address 0012007C

Figure 4-29. DTC Target Register (DTCTARGET)

23	22	21	20	19	18	17	16
DETECT_BLANK							DETECT_LEN
R/W-000 0000							R/W-0000 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DETECT_LEN							TARGET_OFFSET		TARGET_LOW						
R/W-0000 0000							R/W-00		R/W-000 0000						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-29. DTC Target Register (DTCTARGET) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-17	DETECT_BLANK	R/W	000 0000	Sets the target measurement window blanking length, in HFO clock increments.
16-9	DETECT_LEN	R/W	0000 0000	Sets the target measurement window length, in HFO clock increments.
8-7	TARGET_OFFSET	R/W	00	Target Threshold Offset. Target upper threshold = target low + target offset 0 = 0 (Default) 1 = 2 HFO clocks 2 = 4 HFO clocks 3 = 8 HFO clocks
6-0	TARGET_LOW	R/W	000 0000	Target Lower Threshold, in HFO clock increments

4.1.30 DTC Auto Control Limit Register (DTCLIMIT)

Address 00120080

Figure 4-30. DTC Auto Control Limit Register (DTCLIMIT)

19	10	9	0
ADJ_MAX		ADJ_MIN	
R/W-01 1111 1111		R/W-10 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-30. DTC Auto Control Limit Register (DTCLIMIT) Register Field Descriptions

Bit	Field	Type	Reset	Description
19-10	ADJ_MAX	R/W	01 1111 1111	Sets the signed integer upper clamp for the accumulators. The integer range is (-512 to 511)
9-0	ADJ_MIN	R/W	10 0000 0000	Sets the signed integer lower clamp for the accumulators. The integer range is (-512 to 511)

4.1.31 DTC Manual Control Register (DTCMANUAL)

Address 00120084

Register is ignored in automatic mode.

Figure 4-31. DTC Manual Control Register (DTCMANUAL)

19	10	9	0
A_ADJ		B_ADJ	
R/W-00 0000 0000		R/W-00 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-31. DTC Manual Control Register (DTCMANUAL) Register Field Descriptions

Bit	Field	Type	Reset	Description
19-10	A_ADJ	R/W	00 0000 0000	Sets the signed A accumulator value when manual control is enabled.
9-0	B_ADJ	R/W	00 0000 0000	Sets the signed B accumulator value when manual control is enabled.

4.1.32 DTC Monitor Register (DTCMONITOR)

Address 00120088

Figure 4-32. DTC Monitor Register (DTCMONITOR)

19	10	9	0
A_ADJ		B_ADJ	
R/W-00 0000 0000		R/W-00 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-32. DTC Monitor Register (DTCMONITOR) Register Field Descriptions

Bit	Field	Type	Reset	Description
19-10	A_ADJ	R/W	00 0000 0000	Monitored accumulator A value from the DTC module
9-0	B_ADJ	R/W	00 0000 0000	Monitored accumulator B value from the DTC module

4.1.33 DTC Status Register (DTCSTAT)

Address 0012008C

Figure 4-33. DTC Status Register (DTCSTAT)

14	8	7	1	0
A_CNT		B_CNT		FLAG
R-000 0000		R-000 0000		R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-33. DTC Status Register (DTCSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
14-8	A_CNT	R	000 0000	Last measurement value for phase A input signal
7-1	B_CNT	R	000 0000	Last measurement value for phase B input signal
0	FLAG	R	0	Flag is set when the fault count exceeds the FLT MAX value programmed in the DTCCTRL register.

4.1.34 DTC IO Control Register (DTCIOCTRL)

Address 00120090

Figure 4-34. DTC IO Control Register (DTCIOCTRL)

7	6	5	4	3	2	1	0
DTC_B_FUNC	DTC_B_GPIO_DIR	DTC_B_GPIO_VAL	DTC_B_GPIO_IN	DTC_A_FUNC	DTC_A_GPIO_DIR	DTC_A_GPIO_VAL	DTC_A_GPIO_IN
R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-34. DTC IO Control Register (DTCIOCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DTC_B_FUNC	R/W	1	DTC Functional Mode 0 = GPIO Mode 1 = Functional Mode (Default)
6	DTC_B_GPIO_DIR	R/W	0	DTC GPIO Direction 0 = Output Pin (Default) 1 = Input Pin
5	DTC_B_GPIO_VAL	R/W	0	DTC GPIO Output Pin Value 0 = Drive a 0 when pin is configured as an output in GPIO Mode 1 = Drive a 1 when pin is configured as an output in GPIO Mode
4	DTC_B_GPIO_IN	R/W	0	DTC GPIO Input Pin Value 0 = Pin reads as 0 1 = Pin reads as 1
3	DTC_A_FUNC	R/W	1	DTC Functional Mode 0 = GPIO Mode 1 = Functional Mode (Default)
2	DTC_A_GPIO_DIR	R/W	0	DTC GPIO Direction 0 = Output Pin (Default) 1 = Input Pin
1	DTC_A_GPIO_VAL	R/W	0	DTC GPIO Output Pin Value 0 = Drive a 0 when pin is configured as an output in GPIO Mode 1 = Drive a 1 when pin is configured as an output in GPIO Mode
0	DTC_A_GPIO_IN	R/W	0	DTC GPIO Input Pin Value 0 = Pin reads as 0 1 = Pin reads as 1

4.2 Fault Mux Registers Reference

4.2.1 Analog Comparator Control 0 Register (ACOMPCTRL0)

Address 00130000

Figure 4-35. Analog Comparator Control 0 Register (ACOMPCTRL0)

30						24
ACOMP_B_THRESH						
R/W-000 0000						
23	22	21	19	18	17	16
Reserved		ACOMP_B_SEL		ACOMP_B_POL	ACOMP_B_INT_EN	Reserved
R-00		R/W-000		R/W-1	R/W-0	R-00
15	14					8
Reserved	ACOMP_A_THRESH					
R-00	R/W-000 0000					
7	6	5	3	2	1	0
Reserved		ACOMP_A_SEL		ACOMP_A_POL	ACOMP_A_INT_EN	ACOMP_EN
R-00		R/W-000		R/W-1	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-35. Analog Comparator Control 0 Register (ACOMPCTRL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
30-24	ACOMP_B_THRESH	R/W	000 0000	Configures Analog Comparator B Threshold value 0 = Comparator Reference of 19.53125 mV (Default) 1 = Comparator Reference of 39.0625 mV …….. 127 = Comparator Reference of 2.5 V
23-22	Reserved	R	00	
21-19	ACOMP_B_SEL	R/W	000	Configures Analog Comparator B Threshold 0 = Analog Comparator B Threshold set by ACOMP_B_THRESH (Default) 1 = Analog Comparator B Threshold set by Comparator Ramp 0 2 = Analog Comparator B Threshold set by Filter 0 Output 3 = Analog Comparator B Threshold set by Filter 1 Output 4 = Analog Comparator B Threshold set by Filter 2 Output
18	ACOMP_B_POL	R/W	1	Analog Comparator B Polarity 0 = Comparator result enabled when input falls below threshold 1 = Comparator result enabled when input exceeds threshold (Default)
17	ACOMP_B_INT_EN	R/W	0	Analog Comparator B Interrupt Enable 0 = Disables Analog Comparator B Interrupt generation (Default) 1 = Enables Analog Comparator B Interrupt generation
16-15	Reserved	R	00	
14-8	ACOMP_A_THRESH	R/W	000 0000	Configures Analog Comparator A Threshold 0 = Comparator Reference of 19.53125 mV (Default) 1 = Comparator Reference of 39.0625 mV …….. 127 = Comparator Reference of 2.5 V
7-6	Reserved	R	00	
5-3	ACOMP_A_SEL	R/W	000	Configures Analog Comparator A Threshold 0 = Analog Comparator A Threshold set by ACOMP_A_THRESH (Default) 1 = Analog Comparator A Threshold set by Comparator Ramp 0 2 = Analog Comparator A Threshold set by Filter 0 Output 3 = Analog Comparator A Threshold set by Filter 1 Output 4 = Analog Comparator A Threshold set by Filter 2 Output
2	ACOMP_A_POL	R/W	1	Analog Comparator A Polarity 0 = Comparator result enabled when input falls below threshold 1 = Comparator result enabled when input exceeds threshold (Default)

Table 4-35. Analog Comparator Control 0 Register (ACOMPCTRL0) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ACOMP_A_INT_EN	R/W	0	Analog Comparator A Interrupt Enable 0 = Disables Analog Comparator A Interrupt generation (Default) 1 = Enables Analog Comparator A Interrupt generation
0	ACOMP_EN	R/W	0	Analog Comparators Enable 0 = Analog Comparators Disabled (Default) 1 = Analog Comparators Enabled

4.2.2 Analog Comparator Control 1 Register (ACOMPCTRL1)

Address 00130004

Figure 4-36. Analog Comparator Control 1 Register (ACOMPCTRL1)

30						24
ACOMP_D_THRESH						
R/W-000 0000						
23	22	21	19	18	17	16
Reserved		ACOMP_D_SEL		ACOMP_D_POL	ACOMP_D_INT_EN	ACOMP_D_OUT_EN
R-00		R/W-000		R/W-1	R/W-0	R/W-0
15	14					8
Reserved	ACOMP_C_THRESH					
R-0	R/W-000 0000					
7	6	5	3	2	1	0
Reserved		ACOMP_C_SEL		ACOMP_C_POL	ACOMP_C_INT_EN	Reserved
R-00		R/W-000		R/W-1	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-36. Analog Comparator Control 1 Register (ACOMPCTRL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
30-24	ACOMP_D_THRESH	R/W	000 0000	Configures Analog Comparator D Threshold 0 = Comparator Reference of 19.53125 mV (Default) 1 = Comparator Reference of 39.0625 mV …….. 127 = Comparator Reference of 2.5 V
23-22	Reserved	R	00	
21-19	ACOMP_D_SEL	R/W	000	Configures Analog Comparator D Threshold 0 = Analog Comparator D Threshold set by ACOMP_D_THRESH (Default) 1 = Analog Comparator D Threshold set by Comparator Ramp 0 2 = Analog Comparator D Threshold set by Filter 0 Output 3 = Analog Comparator D Threshold set by Filter 1 Output 4 = Analog Comparator D Threshold set by Filter 2 Output
18	ACOMP_D_POL	R/W	1	Analog Comparator D Polarity 0 = Comparator result enabled when input falls below threshold 1 = Comparator result enabled when input exceeds threshold (Default)
17	ACOMP_D_INT_EN	R/W	0	Analog Comparator D Interrupt Enable 0 = Disables Analog Comparator D Interrupt generation (Default) 1 = Enables Analog Comparator D Interrupt generation
16	ACOMP_D_OUT_EN	R/W	0	Analog Comparator D DAC Output Enable 0 = Disables output of Comparator DAC D onto AD pin (Default) 1 = Enables output of Comparator DAC D onto AD pin
15	Reserved	R	0	
14-8	ACOMP_C_THRESH	R/W	000 0000	Configures Analog Comparator C Threshold 0 = Comparator Reference of 19.53125 mV (Default) 1 = Comparator Reference of 39.0625 mV …….. 127 = Comparator Reference of 2.5 V
7-6	Reserved	R	00	

Table 4-36. Analog Comparator Control 1 Register (ACOMPCTRL1) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	ACOMP_C_SEL	R/W	000	Configures Analog Comparator C Threshold 0 = Analog Comparator C Threshold set by ACOMP_C_THRESH (Default) 1 = Analog Comparator C Threshold set by Comparator Ramp 0 2 = Analog Comparator C Threshold set by Filter 0 Output 3 = Analog Comparator C Threshold set by Filter 1 Output 4 = Analog Comparator C Threshold set by Filter 2 Output
2	ACOMP_C_POL	R/W	1	Analog Comparator C Polarity 0 = Comparator result enabled when input falls below threshold 1 = Comparator result enabled when input exceeds threshold (Default)
1	ACOMP_C_INT_EN	R/W	0	Analog Comparator C Interrupt Enable 0 = Disables Analog Comparator C Interrupt generation (Default) 1 = Enables Analog Comparator C Interrupt generation
0	Reserved	R	0	

4.2.3 Analog Comparator Control 2 Register (ACOMPCTRL2)

Address 00130008

Figure 4-37. Analog Comparator Control 2 Register (ACOMPCTRL2)

30						24
ACOMP_F_THRESH						
R/W-000 0000						
23	22	21	19	18	17	16
Reserved	ACOMP_F_REF_SEL	ACOMP_F_SEL		ACOMP_F_POL	ACOMP_F_INT_EN	ACOMP_F_OUT_EN
R-0	R/W-0	R/W-000		R/W-1	R/W-0	R/W-0
15	14					8
Reserved	ACOMP_E_THRESH					
R-0	R/W-000 0000					
7	6	5	3	2	1	0
Reserved		ACOMP_E_SEL		ACOMP_E_POL	ACOMP_E_INT_EN	ACOMP_E_OUT_EN
R-00		R/W-000		R/W-1	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-37. Analog Comparator Control 2 Register (ACOMPCTRL2) Register Field Descriptions

Bit	Field	Type	Reset	Description
30-24	ACOMP_F_THRESH	R/W	000 0000	Configures Analog Comparator F Threshold 0 = Comparator Reference of 19.53125 mV (Default) 1 = Comparator Reference of 39.0625 mV …….. 127 = Comparator Reference of 2.5 V
23	Reserved	R	0	
22	ACOMP_F_REF_SEL	R/W	0	Analog Comparator F Reference Select 0 = Selects internal DAC reference (Default) 1 = Selects reference driven from AD-07 pin
21-19	ACOMP_F_SEL	R/W	000	Configures Analog Comparator F Threshold 0 = Analog Comparator F Threshold set by ACOMP_F_THRESH (Default) 1 = Analog Comparator F Threshold set by Comparator Ramp 0 2 = Analog Comparator F Threshold set by Filter 0 Output 3 = Analog Comparator F Threshold set by Filter 1 Output 4 = Analog Comparator F Threshold set by Filter 2 Output
18	ACOMP_F_POL	R/W	1	Analog Comparator F Polarity 0 = Comparator result enabled when input falls below threshold 1 = Comparator result enabled when input exceeds threshold (Default)
17	ACOMP_F_INT_EN	R/W	0	Analog Comparator F Interrupt Enable 0 = Disables Analog Comparator F Interrupt generation (Default) 1 = Enables Analog Comparator F Interrupt generation
16	ACOMP_F_OUT_EN	R/W	0	Analog Comparator F DAC Output Enable 0 = Disables output of Comparator DAC F onto AD pin (Default) 1 = Enables output of Comparator DAC F onto AD pin
15	Reserved	R	0	
14-8	ACOMP_E_THRESH	R/W	000 0000	Configures Analog Comparator E Threshold 0 = Comparator Reference of 19.53125 mV (Default) 1 = Comparator Reference of 39.0625 mV …….. 127 = Comparator Reference of 2.5 V
7-6	Reserved	R	00	

Table 4-37. Analog Comparator Control 2 Register (ACOMPCTRL2) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	ACOMP_E_SEL	R/W	000	Configures Analog Comparator E Threshold 0 = Analog Comparator E Threshold set by ACOMP_E_THRESH (Default) 1 = Analog Comparator E Threshold set by Comparator Ramp 0 2 = Analog Comparator E Threshold set by Filter 0 Output 3 = Analog Comparator E Threshold set by Filter 1 Output 4 = Analog Comparator E Threshold set by Filter 2 Output
2	ACOMP_E_POL	R/W	1	Analog Comparator E Polarity 0 = Comparator result enabled when input falls below threshold 1 = Comparator result enabled when input exceeds threshold (Default)
1	ACOMP_E_INT_EN	R/W	0	Analog Comparator E Interrupt Enable 0 = Disables Analog Comparator E Interrupt generation (Default) 1 = Enables Analog Comparator E Interrupt generation
0	ACOMP_E_OUT_EN	R/W	0	Analog Comparator E DAC Output Enable 0 = Disables output of Comparator DAC E onto AD pin (Default) 1 = Enables output of Comparator DAC E onto AD pin

4.2.4 Analog Comparator Control 3 Register (ACOMPCTRL3)

Address 0013000C

Figure 4-38. Analog Comparator Control 3 Register (ACOMPCTRL3)

14								8
ACOMP_G_THRESH								
R/W-000 0000								
7	6	5			3	2	1	0
Reserved		ACOMP_G_SEL				ACOMP_G_POL	ACOMP_G_INT_EN	ACOMP_G_OUT_EN
R-00		R/W-000				R/W-1	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-38. Analog Comparator Control 3 Register (ACOMPCTRL3) Register Field Descriptions

Bit	Field	Type	Reset	Description
14-8	ACOMP_G_THRESH	R/W	000 0000	Configures Analog Comparator G Threshold 0 = Comparator Reference of 19.53125 mV (Default) 1 = Comparator Reference of 39.0625 mV …….. 127 = Comparator Reference of 2.5 V
7-6	Reserved	R	00	
5-3	ACOMP_G_SEL	R/W	000	Configures Analog Comparator G Threshold 0 = Analog Comparator G Threshold set by ACOMP_G_THRESH (Default) 1 = Analog Comparator G Threshold set by Comparator Ramp 0 2 = Analog Comparator G Threshold set by Filter 0 Output 3 = Analog Comparator G Threshold set by Filter 1 Output 4 = Analog Comparator G Threshold set by Filter 2 Output
2	ACOMP_G_POL	R/W	1	Analog Comparator G Polarity 0 = Comparator result enabled when input falls below threshold 1 = Comparator result enabled when input exceeds threshold (Default)
1	ACOMP_G_INT_EN	R/W	0	Analog Comparator G Interrupt Enable 0 = Disables Analog Comparator G Interrupt generation (Default) 1 = Enables Analog Comparator G Interrupt generation
0	ACOMP_G_OUT_EN	R/W	0	Analog Comparator G DAC Output Enable 0 = Disables output of Comparator DAC G onto AD pin (Default) 1 = Enables output of Comparator DAC G onto AD pin

4.2.5 External Fault Control Register (EXTFAULTCTRL)

Address 00130010

Figure 4-39. External Fault Control Register (EXTFAULTCTRL)

11	10	9	8
FAULT3_POL	FAULT2_POL	FAULT1_POL	FAULT0_POL
R/W-1	R/W-1	R/W-1	R/W-1

7	6	5	4	3	2	1	0
FAULT3_INT_EN	FAULT2_INT_EN	FAULT1_INT_EN	FAULT0_INT_EN	FAULT3_DET_EN	FAULT2_DET_EN	FAULT1_DET_EN	FAULT0_DET_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-39. External Fault Control Register (EXTFAULTCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
11	FAULT3_POL	R/W	1	Polarity configuration for FAULT[3] pin 0 = Fault detection enabled on falling edge 1 = Fault detection enabled on rising edge (Default)
10	FAULT2_POL	R/W	1	Polarity configuration for FAULT[2] pin 0 = Fault detection enabled on falling edge 1 = Fault detection enabled on rising edge (Default)
9	FAULT1_POL	R/W	1	Polarity configuration for FAULT[1] pin 0 = Fault detection enabled on falling edge 1 = Fault detection enabled on rising edge (Default)
8	FAULT0_POL	R/W	1	Polarity configuration for FAULT[0] pin 0 = Fault detection enabled on falling edge 1 = Fault detection enabled on rising edge (Default)
7	FAULT3_INT_EN	R/W	0	FAULT[3] Pin Interrupt Enable 0 = Disables Fault Detection Interrupt generation (Default) 1 = Enables Fault Detection Interrupt generation
6	FAULT2_INT_EN	R/W	0	FAULT[2] Pin Interrupt Enable 0 = Disables Fault Detection Interrupt generation (Default) 1 = Enables Fault Detection Interrupt generation
5	FAULT1_INT_EN	R/W	0	FAULT[1] Pin Interrupt Enable 0 = Disables Fault Detection Interrupt generation (Default) 1 = Enables Fault Detection Interrupt generation
4	FAULT0_INT_EN	R/W	0	FAULT[0] Pin Interrupt Enable 0 = Disables Fault Detection Interrupt generation (Default) 1 = Enables Fault Detection Interrupt generation
3	FAULT3_DET_EN	R/W	0	FAULT[3] Pin Detection Enable 0 = Fault Detection Disabled (Default) 1 = Fault Detection Enabled
2	FAULT2_DET_EN	R/W	0	FAULT[2] Pin Detection Enable 0 = Fault Detection Disabled (Default) 1 = Fault Detection Enabled
1	FAULT1_DET_EN	R/W	0	FAULT[1] Pin Detection Enable 0 = Fault Detection Disabled (Default) 1 = Fault Detection Enabled
0	FAULT0_DET_EN	R/W	0	FAULT[0] Pin Detection Enable 0 = Fault Detection Disabled (Default) 1 = Fault Detection Enabled

4.2.6 Fault Mux Interrupt Status Register (FAULTMUXINTSTAT)

Address 00130014

Figure 4-40. Fault Mux Interrupt Status Register (FAULTMUXINTSTAT)

17	16	15	14	13	12	11	10	9	8
XTAL_FAIL	DCOMP3	DCOMP2	DCOMP1	DCOMP0	LFO_FAIL	FAULT3	FAULT2	FAULT1	FAULT0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
DCM_DETECT	ACOMP_G	ACOMP_F	ACOMP_E	ACOMP_D	ACOMP_C	ACOMP_B	ACOMP_A
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-40. Fault Mux Interrupt Status Register (FAULTMUXINTSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
17	XTAL_FAIL	R	0	XTAL Fail Interrupt Status, cleared by read of status register 0 = XTAL failure not detected 1 = XTAL failure detected
16	DCOMP3	R	0	Digital Comparator 3 Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
15	DCOMP2	R	0	Digital Comparator 2 Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
14	DCOMP1	R	0	Digital Comparator 1 Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
13	DCOMP0	R	0	Digital Comparator 0 Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
12	LFO_FAIL	R	0	Low Frequency Oscillator Failure Interrupt Status, cleared by read of status register 0 = Low Frequency Oscillator operational 1 = Low Frequency Oscillator failure detected
11	FAULT3	R	0	External FAULT[3] Interrupt Detection 0 = No External GPIO detection found 1 = External GPIO detection found
10	FAULT2	R	0	External FAULT[2] Interrupt Detection 0 = No External GPIO detection found 1 = External GPIO detection found
9	FAULT1	R	0	External FAULT[1] Interrupt Detection 0 = No External GPIO detection found 1 = External GPIO detection found
8	FAULT0	R	0	External FAULT[0] Interrupt Detection 0 = No External GPIO detection found 1 = External GPIO detection found
7	DCM_DETECT	R	0	Discontinuous Conduction Mode Interrupt Status, cleared by read of status register 0 = Discontinuous Conduction Mode detected 1 = Discontinuous Conduction Mode not detected
6	ACOMP_G	R	0	Analog Comparator G Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active

Table 4-40. Fault Mux Interrupt Status Register (FAULTMUXINTSTAT) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ACOMP_F	R	0	Analog Comparator F Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
4	ACOMP_E	R	0	Analog Comparator E Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
3	ACOMP_D	R	0	Analog Comparator D Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
2	ACOMP_C	R	0	Analog Comparator C Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
1	ACOMP_B	R	0	Analog Comparator B Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active
0	ACOMP_A	R	0	Analog Comparator A Interrupt Status, cleared by read of status register 0 = Comparator threshold interrupt inactive 1 = Comparator threshold interrupt active

4.2.7 Fault Mux Raw Status Register (FAULTMUXRAWSTAT)

Address 00130018

Figure 4-41. Fault Mux Raw Status Register (FAULTMUXRAWSTAT)

17	16	15	14	13	12	11	10	9	8
XTAL_FAIL	DCOMP3	DCOMP2	DCOMP1	DCOMP0	LFO_FAIL	FAULT3	FAULT2	FAULT1	FAULT0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
DCM_DETECT	ACOMP_G	ACOMP_F	ACOMP_E	ACOMP_D	ACOMP_C	ACOMP_B	ACOMP_A
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-41. Fault Mux Raw Status Register (FAULTMUXRAWSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
17	XTAL_FAIL	R	0	XTAL Fail Raw Status 0 = XTAL failure not detected 1 = XTAL failure detected
16	DCOMP3	R	0	Digital Comparator 3 Raw Status 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
15	DCOMP2	R	0	Digital Comparator 2 Raw Status 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
14	DCOMP1	R	0	Digital Comparator 1 Raw Status 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
13	DCOMP0	R	0	Digital Comparator 0 Raw Status 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
12	LFO_FAIL	R	0	Low Frequency Oscillator Failure Raw Status 0 = Low Frequency Oscillator operationaL 1 = Low Frequency Oscillator failure detected
11	FAULT3	R	0	External Fault Detection on FAULT[3] pin 0 = No External FAULT[3] detection found 1 = External GPIO detection found
10	FAULT2	R	0	External Fault Detection on FAULT[2] pin 0 = No External FAULT[2] detection found 1 = External GPIO detection found
9	FAULT1	R	0	External Fault Detection on FAULT[1] pin 0 = No External FAULT[1] detection found 1 = External GPIO detection found
8	FAULT0	R	0	External Fault Detection on FAULT[0] pin 0 = No External FAULT[0] detection found 1 = External GPIO detection found
7	DCM_DETECT	R	0	Discontinuous Conduction Mode Raw Status 0 = Discontinuous Conduction Mode detected 1 = Discontinuous Conduction Mode not detected
6	ACOMP_G	R	0	Analog Comparator G Raw Result 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded

Table 4-41. Fault Mux Raw Status Register (FAULTMUXRAWSTAT) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ACOMP_F	R	0	Analog Comparator F Raw Result 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
4	ACOMP_E	R	0	Analog Comparator E Raw Result 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
3	ACOMP_D	R	0	Analog Comparator D Raw Result 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
2	ACOMP_C	R	0	Analog Comparator C Raw Result 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
1	ACOMP_B	R	0	Analog Comparator B Raw Result 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded
0	ACOMP_A	R	0	Analog Comparator A Raw Result 0 = Comparator threshold not exceeded 1 = Comparator threshold exceeded

4.2.8 Comparator Ramp Control 0 Register (COMPRAMP0)

Address 0013001C

Figure 4-42. Comparator Ramp Control 0 Register (COMPRAMP0)

31	28	27	24
START_VALUE_SEL		STEP_SIZE	
R/W-0000		R/W-00 0000 0000 0000 0000	

23	16
STEP_SIZE	
R/W-00 0000 0000 0000 0000	

15	10	9	8
STEP_SIZE		CLKS_PER_STEP	
R/W-00 0000 0000 0000 0000		R/W-0 0000	

7	5	4	3	2	1	0
CLKS_PER_STEP		DPWM3_TRIG_EN	DPWM2_TRIG_EN	DPWM1_TRIG_EN	DPWM0_TRIG_EN	RAMP_EN
R/W-0 0000		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-42. Comparator Ramp Control 0 Register (COMPRAMP0) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	START_VALUE_SEL	R/W	0000	Configures comparator ramp starting value 0 = Filter 0 Output (Bits 17-11) (Default) 1 = Filter 1 Output (Bits 17-11) 2 = Filter 2 Output (Bits 17-11) 3 = Analog Comparator Threshold A Value 4 = Analog Comparator Threshold B Value 5 = Analog Comparator Threshold C Value 6 = Analog Comparator Threshold D Value 7 = Analog Comparator Threshold E Value 8 = Analog Comparator Threshold F Value 9 = Analog Comparator Threshold G Value
27-10	STEP_SIZE	R/W	00 0000 0000 0000 0000	Programmable 18-bit unsigned comparator step with Bits 27:24 representing the integer portion of the comparator step (0-15 Comparator steps of 19.5mV each) and Bits 23:10 representing the fractional portion of the comparator step
9-5	CLKS_PER_STEP	R/W	0 0000	Selects number of MCLK (HFO_OSC/8) clock cycles per comparator step where number of subcycles can vary from 1 to 32 0 = 1 MCLK clock cycles per step (Default) 1 = 2 MCLK clock cycles per step 2 = 3 MCLK clock cycles per step ……. 31 = 32 MCLK clock cycles per step
4	DPWM3_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 3 to Analog Comparator Ramp 0 0 = DPWM 3 trigger not routed to Analog Comparator Ramp 0 (Default) 1 = DPWM 3 trigger routed to Analog Comparator Ramp 0
3	DPWM2_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 2 to Analog Comparator Ramp 0 0 = DPWM 2 trigger not routed to Analog Comparator Ramp 0 (Default) 1 = DPWM 2 trigger routed to Analog Comparator Ramp 0
2	DPWM1_TRIG_EN	R/W	0	Enables DPWM Trigger from DPWM 1 to Analog Comparator Ramp 0 0 = DPWM 1 trigger not routed to Analog Comparator Ramp 0 (Default) 1 = DPWM 1 trigger routed to Analog Comparator Ramp 0

Table 4-42. Comparator Ramp Control 0 Register (COMPRAMP0) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DPWM0_TRIG _EN	R/W	0	Enables DPWM Trigger from DPWM 0 to Analog Comparator Ramp 0 0 = DPWM 0 trigger not routed to Analog Comparator Ramp 0 (Default) 1 = DPWM 0 trigger routed to Analog Comparator Ramp 0
0	RAMP_EN	R/W	0	Enable for Analog Comparator Ramp 0 0 = Analog Comparator Ramp disabled (Default) 1 = Analog Comparator Ramp enabled

4.2.9 Digital Comparator Control 0 Register (DCOMPCTRL0)

Address 00130020

Figure 4-43. Digital Comparator Control 0 Register (DCOMPCTRL0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNT_THRESH								Reserved					COMP_POL	FE_SEL	
R/W-0000 0000								R-0000 0					R/W-0	R/W-000	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE_SEL	CNT_CLR	CNT_CONFIG	INT_EN	COMP_EN	THRESH										
R/W-000	R/W-0	R/W-0	R/W-0	R/W-0	R/W-000 0000 0000										

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-43. Digital Comparator Control 0 Register (DCOMPCTRL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CNT_THRESH	R/W	0000 0000	Sets the number of received comparator events before declaring a fault
23-19	Reserved	R	0000 0	
18	COMP_POL	R/W	0	Digital Comparator 0 Polarity 0 = Digital Comparator result asserted if value below threshold (Default) 1 = Digital Comparator result asserted if value above threshold
17-15	FE_SEL	R/W	000	Selects which Front End absolute data is used for Digital Comparison with threshold 0 = Front End 0 absolute data selected (Default) 1 = Front End 1 absolute data selected 2 = Front End 2 absolute data selected 3 = Front End 0 error data selected 4 = Front End 1 error data selected 5 = Front End 2 error data selected
14	CNT_CLR	R/W	0	Comparator Detection Counter clear 0 = No clear of Comparator Detection Counter (Default) 1 = Clear Comparator Detection counter and associated fault
13	CNT_CONFIG	R/W	0	Comparator Detection Counter configuration 0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default) 1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold
12	INT_EN	R/W	0	Comparator Interrupt Enable 0 = Disables Comparator Interrupt generation (Default) 1 = Enables Comparator Interrupt generation
11	COMP_EN	R/W	0	Digital Comparator 0 Enable 0 = Disables Digital Comparator 0 (Default) 1 = Enables Digital Comparator 0
10-0	THRESH	R/W	000 0000 0000	Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

4.2.10 Digital Comparator Control 1 Register (DCOMPCTRL1)

Address 00130024

Figure 4-44. Digital Comparator Control 1 Register (DCOMPCTRL1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNT_THRESH								Reserved					COMP_POL	FE_SEL	
R/W-0000 0000								R-0000 0					R/W-0	R/W-000	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE_SEL	CNT_CLR	CNT_CONFIG	INT_EN	COMP_EN	THRESH										
R/W-000	R/W-0	R/W-0	R/W-0	R/W-0	R/W-000 0000 0000										

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-44. Digital Comparator Control 1 Register (DCOMPCTRL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CNT_THRESH	R/W	0000 0000	Sets the number of received comparator events before declaring a fault
23-19	Reserved	R	0000 0	
18	COMP_POL	R/W	0	Digital Comparator 0 Polarity 0 = Digital Comparator result asserted if value below threshold (Default) 1 = Digital Comparator result asserted if value above threshold
17-15	FE_SEL	R/W	000	Selects which Front End absolute data is used for Digital Comparison with threshold 0 = Front End 0 absolute data selected (Default) 1 = Front End 1 absolute data selected 2 = Front End 2 absolute data selected 3 = Front End 0 error data selected 4 = Front End 1 error data selected 5 = Front End 2 error data selected
14	CNT_CLR	R/W	0	Comparator Detection Counter clear 0 = No clear of Comparator Detection Counter (Default) 1 = Clear Comparator Detection counter and associated fault
13	CNT_CONFIG	R/W	0	Comparator Detection Counter configuration 0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default) 1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold
12	INT_EN	R/W	0	Comparator Interrupt Enable 0 = Disables Comparator Interrupt generation (Default) 1 = Enables Comparator Interrupt generation
11	COMP_EN	R/W	0	Digital Comparator 0 Enable 0 = Disables Digital Comparator 0 (Default) 1 = Enables Digital Comparator 0
10-0	THRESH	R/W	000 0000 0000	Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

4.2.11 Digital Comparator Control 2 Register (DCOMPCTRL2)

Address 00130028

Figure 4-45. Digital Comparator Control 2 Register (DCOMPCTRL2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNT_THRESH								Reserved					COMP_POL	FE_SEL	
R/W-0000 0000								R-0000 0					R/W-0	R/W-000	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE_SEL	CNT_CLR	CNT_CONFIG	INT_EN	COMP_EN	THRESH										
R/W-000	R/W-0	R/W-0	R/W-0	R/W-0	R/W-000 0000 0000										

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-45. Digital Comparator Control 2 Register (DCOMPCTRL2) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CNT_THRESH	R/W	0000 0000	Sets the number of received comparator events before declaring a fault
23-19	Reserved	R	0000 0	
18	COMP_POL	R/W	0	Digital Comparator 0 Polarity 0 = Digital Comparator result asserted if value below threshold (Default) 1 = Digital Comparator result asserted if value above threshold
17-15	FE_SEL	R/W	000	Selects which Front End absolute data is used for Digital Comparison with threshold 0 = Front End 0 absolute data selected (Default) 1 = Front End 1 absolute data selected 2 = Front End 2 absolute data selected 3 = Front End 0 error data selected 4 = Front End 1 error data selected 5 = Front End 2 error data selected
14	CNT_CLR	R/W	0	Comparator Detection Counter clear 0 = No clear of Comparator Detection Counter (Default) 1 = Clear Comparator Detection counter and associated fault
13	CNT_CONFIG	R/W	0	Comparator Detection Counter configuration 0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default) 1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold
12	INT_EN	R/W	0	Comparator Interrupt Enable 0 = Disables Comparator Interrupt generation (Default) 1 = Enables Comparator Interrupt generation
11	COMP_EN	R/W	0	Digital Comparator 0 Enable 0 = Disables Digital Comparator 0 (Default) 1 = Enables Digital Comparator 0
10-0	THRESH	R/W	000 0000 0000	Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

4.2.12 Digital Comparator Control 3 Register (DCOMPCTRL3)

Address 0013002C

Figure 4-46. Digital Comparator Control 3 Register (DCOMPCTRL3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNT_THRESH								Reserved					COMP_POL	FE_SEL	
R/W-000 0000								R-0000 0					R/W-0	R/W-000	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE_SEL	CNT_CLR	CNT_CONFIG	INT_EN	COMP_EN	THRESH										
R/W-000	R/W-0	R/W-0	R/W-0	R/W-0	R/W-000 0000 0000										

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-46. Digital Comparator Control 3 Register (DCOMPCTRL3) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CNT_THRESH	R/W	0000 0000	Sets the number of received comparator events before declaring a fault
23-19	Reserved	R	0000 0	
18	COMP_POL	R/W	0	Digital Comparator 1 Polarity 0 = Digital Comparator result asserted if value below threshold (Default) 1 = Digital Comparator result asserted if value above threshold
17-15	FE_SEL	R/W	000	Selects which Front End absolute data is used for Digital Comparison with threshold 0 = Front End 0 absolute data selected (Default) 1 = Front End 1 absolute data selected 2 = Front End 2 absolute data selected 3 = Front End 0 error data selected 4 = Front End 1 error data selected 5 = Front End 2 error data selected
14	CNT_CLR	R/W	0	Comparator Detection Counter clear 0 = No clear of Comparator Detection Counter (Default) 1 = Clear Comparator Detection counter and associated fault
13	CNT_CONFIG	R/W	0	Comparator Detection Counter configuration 0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default) 1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold
12	INT_EN	R/W	0	Comparator Interrupt Enable 0 = Disables Comparator Interrupt generation (Default) 1 = Enables Comparator Interrupt generation
11	COMP_EN	R/W	0	Digital Comparator 3 Enable 0 = Disables Digital Comparator 3 (Default) 1 = Enables Digital Comparator 3
10-0	THRESH	R/W	000 0000 0000	Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

4.2.13 Digital Comparator Counter Status Register (DCOMPCNTSTAT)

Address 00130030

Figure 4-47. Digital Comparator Counter Status Register (DCOMPCNTSTAT)

31	24	23	16	15	8	7	0
DCOMP3_CNT		DCOMP2_CNT		DCOMP1_CNT		DCOMP0_CNT	
R-0		R-0		R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-47. Digital Comparator Counter Status Register (DCOMPCNTSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DCOMP3_CNT	R	0	Current value of Digital Comparator 3 detection counter
23-16	DCOMP2_CNT	R	0	Current value of Digital Comparator 2 detection counter
15-8	DCOMP1_CNT	R	0	Current value of Digital Comparator 1 detection counter
7-0	DCOMP0_CNT	R	0	Current value of Digital Comparator 0 detection counter

4.2.14 DPWM 0 Current Limit Control Register (DPWM0CLIM)

Address 00130034

Figure 4-48. DPWM 0 Current Limit Control Register (DPWM0CLIM)

15	14	13	12	11	10	9	8
ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN	FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-48. DPWM 0 Current Limit Control Register (DPWM0CLIM) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ANALOG_PCM_EN	R/W	0	Enables Analog Peak Current detection result for DPWM 0 Current Limit 0 = Analog Peak Current detection disabled for current limit (Default) 1 = Analog Peak Current detection enabled for current limit
14	DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 0 Current Limit 0 = Digital Comparator 3 result disabled for current limit (Default) 1 = Digital Comparator 3 result enabled for current limit
13	DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 0 Current Limit 0 = Digital Comparator 2 result disabled for current limit (Default) 1 = Digital Comparator 2 result enabled for current limit
12	DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 0 Current Limit 0 = Digital Comparator 1 result disabled for current limit (Default) 1 = Digital Comparator 1 result enabled for current limit
11	DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 0 Current Limit 0 = Digital Comparator 0 result disabled for current limit (Default) 1 = Digital Comparator 0 result enabled for current limit
10	FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 0 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
9	FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 0 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
8	FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 0 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
7	FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 0 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
6	ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 0 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
5	ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 0 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
4	ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 0 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

Table 4-48. DPWM 0 Current Limit Control Register (DPWM0CLIM) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 0 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
2	ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 0 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
1	ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 0 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
0	ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 0 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

4.2.15 DPWM 0 Fault AB Detection Register (DPWM0FLTABDET)

Address 00130038

Figure 4-49. DPWM 0 Fault AB Detection Register (DPWM0FLTABDET)

14	13	12	11	10	9	8
DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN	FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-49. DPWM 0 Fault AB Detection Register (DPWM0FLTABDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
14	DCOMP3_EN	R/W	0	
13	DCOMP2_EN	R/W	0	
12	DCOMP1_EN	R/W	0	
11	DCOMP0_EN	R/W	0	
10	FAULT3_EN	R/W	0	
9	FAULT2_EN	R/W	0	
8	FAULT1_EN	R/W	0	
7	FAULT0_EN	R/W	0	
6	ACOMP_G_EN	R/W	0	
5	ACOMP_F_EN	R/W	0	
4	ACOMP_E_EN	R/W	0	
3	ACOMP_D_EN	R/W	0	
2	ACOMP_C_EN	R/W	0	
1	ACOMP_B_EN	R/W	0	
0	ACOMP_A_EN	R/W	0	

4.2.16 DPWM 0 Fault Detection Register (DPWM0FAULTDET)

Address 0013003C

Figure 4-50. DPWM 0 Fault Detection Register (DPWM0FAULTDET)

30	29	28	27	26	25	24
PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN	PWMB_FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
PWMB_FAULT0_EN	PWMB_ACOMP_G_EN	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
Reserved	PWMA_DCOMP3_EN	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN	PWMA_FAULT3_EN	PWMA_FAULT2_EN	PWMA_FAULT1_EN
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
PWMA_FAULT0_EN	PWMA_ACOMP_G_EN	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-50. DPWM 0 Fault Detection Register (DPWM0FAULTDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
30	PWMB_DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 0 PWM-B Fault Detection 0 = Digital Comparator 3 disabled for fault detection (Default) 1 = Digital Comparator 3 enabled for fault detection
29	PWMB_DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 0 PWM-B Fault Detection 0 = Digital Comparator 2 disabled for fault detection (Default) 1 = Digital Comparator 2 enabled for fault detection
28	PWMB_DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 0 PWM-B Fault Detection 0 = Digital Comparator 1 disabled for fault detection (Default) 1 = Digital Comparator 1 enabled for fault detection
27	PWMB_DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 0 PWM-B Fault Detection 0 = Digital Comparator 0 disabled for fault detection (Default) 1 = Digital Comparator 0 enabled for fault detection
26	PWMB_FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 0 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
25	PWMB_FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 0 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
24	PWMB_FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 0 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
23	PWMB_FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 0 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
22	PWMB_ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 0 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

Table 4-50. DPWM 0 Fault Detection Register (DPWM0FAULTDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PWMB_ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 0 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
20	PWMB_ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 0 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
19	PWMB_ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 0 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
18	PWMB_ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 0 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
17	PWMB_ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 0 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
16	PWMB_ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 0 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
15	Reserved	R	0	
14	PWMA_DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 0 PWM-A Fault Detection 0 = Digital Comparator 3 disabled for fault detection (Default) 1 = Digital Comparator 3 enabled for fault detection
13	PWMA_DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 0 PWM-A Fault Detection 0 = Digital Comparator 2 disabled for fault detection (Default) 1 = Digital Comparator 2 enabled for fault detection
12	PWMA_DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 0 PWM-A Fault Detection 0 = Digital Comparator 1 disabled for fault detection (Default) 1 = Digital Comparator 1 enabled for fault detection
11	PWMA_DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 0 PWM-A Fault Detection 0 = Digital Comparator 0 disabled for fault detection (Default) 1 = Digital Comparator 0 enabled for fault detection
10	PWMA_FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 0 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
9	PWMA_FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 0 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
8	PWMA_FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 0 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
7	PWMA_FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 0 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
6	PWMA_ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 0 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
5	PWMA_ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 0 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

Table 4-50. DPWM 0 Fault Detection Register (DPWM0FAULTDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PWMA_ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 0 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
3	PWMA_ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 0 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
2	PWMA_ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 0 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
1	PWMA_ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 0 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
0	PWMA_ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 0 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

4.2.17 DPWM 1 Current Limit Control Register (DPWM1CLIM)

Address 00130044

Figure 4-51. DPWM 1 Current Limit Control Register (DPWM1CLIM)

15	14	13	12	11	10	9	8
ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN	FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-51. DPWM 1 Current Limit Control Register (DPWM1CLIM) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ANALOG_PCM_EN	R/W	0	Enables Analog Peak Current detection result for DPWM 1 Current Limit 0 = Analog Peak Current detection disabled for current limit (Default) 1 = Analog Peak Current detection enabled for current limit
14	DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 1 Current Limit 0 = Digital Comparator 3 result disabled for current limit (Default) 1 = Digital Comparator 3 result enabled for current limit
13	DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 1 Current Limit 0 = Digital Comparator 2 result disabled for current limit (Default) 1 = Digital Comparator 2 result enabled for current limit
12	DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 1 Current Limit 0 = Digital Comparator 1 result disabled for current limit (Default) 1 = Digital Comparator 1 result enabled for current limit
11	DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 1 Current Limit 0 = Digital Comparator 0 result disabled for current limit (Default) 1 = Digital Comparator 0 result enabled for current limit
10	FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 1 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
9	FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 1 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
8	FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 1 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
7	FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 1 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
6	ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
5	ACOMP_F_EN	R/W	0	Enables Analog Comparator Fresult for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
4	ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

Table 4-51. DPWM 1 Current Limit Control Register (DPWM1CLIM) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
2	ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
1	ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
0	ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

4.2.18 DPWM 1 Fault AB Detection Register (DPWM1FLTABDET)

Address 00130048

Figure 4-52. DPWM 1 Fault AB Detection Register (DPWM1FLTABDET)

14	13	12	11	10	9	8
DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN	FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-52. DPWM 1 Fault AB Detection Register (DPWM1FLTABDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
14	DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 1 Current Limit 0 = Digital Comparator 3 result disabled for current limit (Default) 1 = Digital Comparator 3 result enabled for current limit
13	DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 1 Current Limit 0 = Digital Comparator 2 result disabled for current limit (Default) 1 = Digital Comparator 2 result enabled for current limit
12	DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 1 Current Limit 0 = Digital Comparator 1 result disabled for current limit (Default) 1 = Digital Comparator 1 result enabled for current limit
11	DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 1 Current Limit 0 = Digital Comparator 0 result disabled for current limit (Default) 1 = Digital Comparator 0 result enabled for current limit
10	FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 1 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
9	FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 1 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
8	FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 1 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
7	FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 1 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
6	ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
5	ACOMP_F_EN	R/W	0	Enables Analog Comparator Fresult for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
4	ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
3	ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

Table 4-52. DPWM 1 Fault AB Detection Register (DPWM1FLTABDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
1	ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
0	ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 1 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

4.2.19 DPWM 1 Fault Detection Register (DPWM1FAULTDET)

Address 0013004C

Figure 4-53. DPWM 1 Fault Detection Register (DPWM1FAULTDET)

30	29	28	27	26	25	24
PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN	PWMB_FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
PWMB_FAULT0_EN	PWMB_ACOMP_G_EN	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
Reserved	PWMA_DCOMP3_EN	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN	PWMA_FAULT3_EN	PWMA_FAULT2_EN	PWMA_FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
PWMA_FAULT0_EN	PWMA_ACOMP_G_EN	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-53. DPWM 1 Fault Detection Register (DPWM1FAULTDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
30	PWMB_DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 1 PWM-B Fault Detection 0 = Digital Comparator 3 disabled for fault detection (Default) 1 = Digital Comparator 3 enabled for fault detection
29	PWMB_DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 1 PWM-B Fault Detection 0 = Digital Comparator 2 disabled for fault detection (Default) 1 = Digital Comparator 2 enabled for fault detection
28	PWMB_DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 1 PWM-B Fault Detection 0 = Digital Comparator 1 disabled for fault detection (Default) 1 = Digital Comparator 1 enabled for fault detection
27	PWMB_DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 1 PWM-B Fault Detection 0 = Digital Comparator 0 disabled for fault detection (Default) 1 = Digital Comparator 0 enabled for fault detection
26	PWMB_FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 1 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
25	PWMB_FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 1 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
24	PWMB_FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 1 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
23	PWMB_FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 1 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
22	PWMB_ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 1 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

Table 4-53. DPWM 1 Fault Detection Register (DPWM1FAULTDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PWMB_ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 1 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
20	PWMB_ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 1 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
19	PWMB_ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 1 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
18	PWMB_ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 1 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
17	PWMB_ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 1 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
16	PWMB_ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 1 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
15	Reserved	R	0	
14	PWMA_DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 1 PWM-A Fault Detection 0 = Digital Comparator 3 disabled for fault detection (Default) 1 = Digital Comparator 3 enabled for fault detection
13	PWMA_DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 1 PWM-A Fault Detection 0 = Digital Comparator 2 disabled for fault detection (Default) 1 = Digital Comparator 2 enabled for fault detection
12	PWMA_DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 1 PWM-A Fault Detection 0 = Digital Comparator 1 disabled for fault detection (Default) 1 = Digital Comparator 1 enabled for fault detection
11	PWMA_DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 1 PWM-A Fault Detection 0 = Digital Comparator 0 disabled for fault detection (Default) 1 = Digital Comparator 0 enabled for fault detection
10	PWMA_FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 1 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
9	PWMA_FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 1 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
8	PWMA_FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 1 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
7	PWMA_FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 1 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
6	PWMA_ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 1 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
5	PWMA_ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 1 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

Table 4-53. DPWM 1 Fault Detection Register (DPWM1FAULTDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PWMA_ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 1 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
3	PWMA_ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 1 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
2	PWMA_ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 1 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
1	PWMA_ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 1 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
0	PWMA_ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 1 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

4.2.20 DPWM 2 Current Limit Control Register (DPWM2CLIM)

Address 00130054

Figure 4-54. DPWM 2 Current Limit Control Register (DPWM2CLIM)

15	14	13	12	11	10	9	8
ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN	FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-54. DPWM 2 Current Limit Control Register (DPWM2CLIM) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ANALOG_PCM_EN	R/W	0	Enables Analog Peak Current detection result for DPWM 2 Current Limit 0 = Analog Peak Current detection disabled for current limit (Default) 1 = Analog Peak Current detection enabled for current limit
14	DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 2 Current Limit 0 = Digital Comparator 3 result disabled for current limit (Default) 1 = Digital Comparator 3 result enabled for current limit
13	DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 2 Current Limit 0 = Digital Comparator 2 result disabled for current limit (Default) 1 = Digital Comparator 2 result enabled for current limit
12	DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 2 Current Limit 0 = Digital Comparator 1 result disabled for current limit (Default) 1 = Digital Comparator 1 result enabled for current limit
11	DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 2 Current Limit 0 = Digital Comparator 0 result disabled for current limit (Default) 1 = Digital Comparator 0 result enabled for current limit
10	FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 2 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
9	FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 2 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
8	FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 2 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
7	FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 2 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
6	ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 2 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
5	ACOMP_F_EN	R/W	0	Enables Analog Comparator Fresult for DPWM 2 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
4	ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 2 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

Table 4-54. DPWM 2 Current Limit Control Register (DPWM2CLIM) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 2 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
2	ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 2 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
1	ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 2 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
0	ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 2 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

4.2.21 DPWM 2 Fault AB Detection Register (DPWM2FLTABDET)

Address 00130058

Figure 4-55. DPWM 2 Fault AB Detection Register (DPWM2FLTABDET)

14	13	12	11	10	9	8
DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN	FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-55. DPWM 2 Fault AB Detection Register (DPWM2FLTABDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
14	DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 2 Fault AB Detection 0 = Digital Comparator 3 disabled for Fault AB detection (Default) 1 = Digital Comparator 3 enabled for Fault AB detection
13	DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 2 Fault AB Detection 0 = Digital Comparator 2 disabled for Fault AB detection (Default) 1 = Digital Comparator 2 enabled for Fault AB detection
12	DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 2 Fault AB Detection 0 = Digital Comparator 1 disabled for Fault AB detection (Default) 1 = Digital Comparator 1 enabled for Fault AB detection
11	DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 2 Fault AB Detection 0 = Digital Comparator 0 disabled for Fault AB detection (Default) 1 = Digital Comparator 0 enabled for Fault AB detection
10	FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 2 Fault AB detection 0 = External Fault pin disabled for Fault AB detection (Default) 1 = External Fault pin enabled for Fault AB detection
9	FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 2 Fault AB detection 0 = External Fault pin disabled for Fault AB detection (Default) 1 = External Fault pin enabled for Fault AB detection
8	FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 2 Fault AB detection 0 = External Fault pin disabled for Fault AB detection (Default) 1 = External Fault pin enabled for Fault AB detection
7	FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 2 Fault AB detection 0 = External Fault pin disabled for Fault AB detection (Default) 1 = External Fault pin enabled for Fault AB detection
6	ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 2 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
5	ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 2 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
4	ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 2 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
3	ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 2 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection

Table 4-55. DPWM 2 Fault AB Detection Register (DPWM2FLTABDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 2 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
1	ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 2 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
0	ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 2 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection

4.2.22 DPWM 2 Fault Detection Register (DPWM2FAULTDET)

Address 0013005C

Figure 4-56. DPWM 2 Fault Detection Register (DPWM2FAULTDET)

30	29	28	27	26	25	24
PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN	PWMB_FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
PWMB_FAULT0_EN	PWMB_ACOMP_G_EN	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
Reserved	PWMA_DCOMP3_EN	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN	PWMA_FAULT3_EN	PWMA_FAULT2_EN	PWMA_FAULT1_EN
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
PWMA_FAULT0_EN	PWMA_ACOMP_G_EN	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-56. DPWM 2 Fault Detection Register (DPWM2FAULTDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
30	PWMB_DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 2 PWM-B Fault Detection 0 = Digital Comparator 3 disabled for fault detection (Default) 1 = Digital Comparator 3 enabled for fault detection
29	PWMB_DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 2 PWM-B Fault Detection 0 = Digital Comparator 2 disabled for fault detection (Default) 1 = Digital Comparator 2 enabled for fault detection
28	PWMB_DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 2 PWM-B Fault Detection 0 = Digital Comparator 1 disabled for fault detection (Default) 1 = Digital Comparator 1 enabled for fault detection
27	PWMB_DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 2 PWM-B Fault Detection 0 = Digital Comparator 0 disabled for fault detection (Default) 1 = Digital Comparator 0 enabled for fault detection
26	PWMB_FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 2 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
25	PWMB_FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 2 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
24	PWMB_FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 2 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
23	PWMB_FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 2 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
22	PWMB_ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 2 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

Table 4-56. DPWM 2 Fault Detection Register (DPWM2FAULTDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PWMB_ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 2 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
20	PWMB_ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 2 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
19	PWMB_ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 2 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
18	PWMB_ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 2 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
17	PWMB_ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 2 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
16	PWMB_ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 2 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
15	Reserved	R	0	
14	PWMA_DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 2 PWM-A Fault Detection 0 = Digital Comparator 3 disabled for fault detection (Default) 1 = Digital Comparator 3 enabled for fault detection
13	PWMA_DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 2 PWM-A Fault Detection 0 = Digital Comparator 2 disabled for fault detection (Default) 1 = Digital Comparator 2 enabled for fault detection
12	PWMA_DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 2 PWM-A Fault Detection 0 = Digital Comparator 1 disabled for fault detection (Default) 1 = Digital Comparator 1 enabled for fault detection
11	PWMA_DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 2 PWM-A Fault Detection 0 = Digital Comparator 0 disabled for fault detection (Default) 1 = Digital Comparator 0 enabled for fault detection
10	PWMA_FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 2 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
9	PWMA_FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 2 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
8	PWMA_FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 2 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
7	PWMA_FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 2 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
6	PWMA_ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 2 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
5	PWMA_ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 2 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

Table 4-56. DPWM 2 Fault Detection Register (DPWM2FAULTDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PWMA_ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 2 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
3	PWMA_ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 2 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
2	PWMA_ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 2 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
1	PWMA_ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 2 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
0	PWMA_ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 2 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

4.2.23 DPWM 3 Current Limit Control Register (DPWM3CLIM)

Address 00130064

Figure 4-57. DPWM 3 Current Limit Control Register (DPWM3CLIM)

15	14	13	12	11	10	9	8
ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN	FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-57. DPWM 3 Current Limit Control Register (DPWM3CLIM) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ANALOG_PCM_EN	R/W	0	Enables Analog Peak Current detection result for DPWM 3 Current Limit 0 = Analog Peak Current detection disabled for current limit (Default) 1 = Analog Peak Current detection enabled for current limit
14	DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 3 Current Limit 0 = Digital Comparator 3 result disabled for current limit (Default) 1 = Digital Comparator 3 result enabled for current limit
13	DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 3 Current Limit 0 = Digital Comparator 2 result disabled for current limit (Default) 1 = Digital Comparator 2 result enabled for current limit
12	DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 3 Current Limit 0 = Digital Comparator 1 result disabled for current limit (Default) 1 = Digital Comparator 1 result enabled for current limit
11	DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 3 Current Limit 0 = Digital Comparator 0 result disabled for current limit (Default) 1 = Digital Comparator 0 result enabled for current limit
10	FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 3 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
9	FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 3 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
8	FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 3 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
7	FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 3 Current Limit 0 = External Fault pin disabled for current limit (Default) 1 = External Fault pin enabled for current limit
6	ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 3 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
5	ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 3 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
4	ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 3 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

Table 4-57. DPWM 3 Current Limit Control Register (DPWM3CLIM) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 3 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
2	ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 3 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
1	ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 3 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit
0	ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 3 Current Limit 0 = Analog Comparator result disabled for current limit (Default) 1 = Analog Comparator result enabled for current limit

4.2.24 DPWM 3 Fault AB Detection Register (DPWM3FLTABDET)

Address 00130068

Figure 4-58. DPWM 3 Fault AB Detection Register (DPWM3FLTABDET)

14	13	12	11	10	9	8
DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN	FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-58. DPWM 3 Fault AB Detection Register (DPWM3FLTABDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
14	DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 3 Fault AB Detection 0 = Digital Comparator 3 disabled for Fault AB detection (Default) 1 = Digital Comparator 3 enabled for Fault AB detection
13	DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 3 Fault AB Detection 0 = Digital Comparator 2 disabled for Fault AB detection (Default) 1 = Digital Comparator 2 enabled for Fault AB detection
12	DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 3 Fault AB Detection 0 = Digital Comparator 1 disabled for Fault AB detection (Default) 1 = Digital Comparator 1 enabled for Fault AB detection
11	DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 3 Fault AB Detection 0 = Digital Comparator 0 disabled for Fault AB detection (Default) 1 = Digital Comparator 0 enabled for Fault AB detection
10	FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 3 Fault AB detection 0 = External Fault pin disabled for Fault AB detection (Default) 1 = External Fault pin enabled for Fault AB detection
9	FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 3 Fault AB detection 0 = External Fault pin disabled for Fault AB detection (Default) 1 = External Fault pin enabled for Fault AB detection
8	FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 3 Fault AB detection 0 = External Fault pin disabled for Fault AB detection (Default) 1 = External Fault pin enabled for Fault AB detection
7	FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 3 Fault AB detection 0 = External Fault pin disabled for Fault AB detection (Default) 1 = External Fault pin enabled for Fault AB detection
6	ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 3 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
5	ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 3 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
4	ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 3 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
3	ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 3 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection

Table 4-58. DPWM 3 Fault AB Detection Register (DPWM3FLTABDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 3 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
1	ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 3 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection
0	ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 3 Fault AB detection 0 = Analog Comparator result disabled for Fault AB detection (Default) 1 = Analog Comparator result enabled for Fault AB detection

4.2.25 DPWM 3 Fault Detection Register (DPWM3FAULTDET)

Address 0013006C

Figure 4-59. DPWM 3 Fault Detection Register (DPWM3FAULTDET)

30	29	28	27	26	25	24
PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN	PWMB_FAULT1_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
PWMB_FAULT0_EN	PWMB_ACOMP_G_EN	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
Reserved	PWMA_DCOMP3_EN	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN	PWMA_FAULT3_EN	PWMA_FAULT2_EN	PWMA_FAULT1_EN
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
PWMA_FAULT0_EN	PWMA_ACOMP_G_EN	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-59. DPWM 3 Fault Detection Register (DPWM3FAULTDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
30	PWMB_DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 3 PWM-B Fault Detection 0 = Digital Comparator 3 disabled for fault detection (Default) 1 = Digital Comparator 3 enabled for fault detection
29	PWMB_DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 3 PWM-B Fault Detection 0 = Digital Comparator 2 disabled for fault detection (Default) 1 = Digital Comparator 2 enabled for fault detection
28	PWMB_DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 3 PWM-B Fault Detection 0 = Digital Comparator 1 disabled for fault detection (Default) 1 = Digital Comparator 1 enabled for fault detection
27	PWMB_DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 3 PWM-B Fault Detection 0 = Digital Comparator 0 disabled for fault detection (Default) 1 = Digital Comparator 0 enabled for fault detection
26	PWMB_FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 3 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
25	PWMB_FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 3 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
24	PWMB_FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 3 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
23	PWMB_FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 3 PWM-B Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
22	PWMB_ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 3 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

Table 4-59. DPWM 3 Fault Detection Register (DPWM3FAULTDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PWMB_ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 3 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
20	PWMB_ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 3 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
19	PWMB_ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 3 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
18	PWMB_ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 3 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
17	PWMB_ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 3 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
16	PWMB_ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 3 PWM-B Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
15	Reserved	R	0	
14	PWMA_DCOMP3_EN	R/W	0	Enables Digital Comparator 3 result for DPWM 3 PWM-A Fault Detection 0 = Digital Comparator 3 disabled for fault detection (Default) 1 = Digital Comparator 3 enabled for fault detection
13	PWMA_DCOMP2_EN	R/W	0	Enables Digital Comparator 2 result for DPWM 3 PWM-A Fault Detection 0 = Digital Comparator 2 disabled for fault detection (Default) 1 = Digital Comparator 2 enabled for fault detection
12	PWMA_DCOMP1_EN	R/W	0	Enables Digital Comparator 1 result for DPWM 3 PWM-A Fault Detection 0 = Digital Comparator 1 disabled for fault detection (Default) 1 = Digital Comparator 1 enabled for fault detection
11	PWMA_DCOMP0_EN	R/W	0	Enables Digital Comparator 0 result for DPWM 3 PWM-A Fault Detection 0 = Digital Comparator 0 disabled for fault detection (Default) 1 = Digital Comparator 0 enabled for fault detection
10	PWMA_FAULT3_EN	R/W	0	Enables FAULT[3] pin for DPWM 3 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
9	PWMA_FAULT2_EN	R/W	0	Enables FAULT[2] pin for DPWM 3 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
8	PWMA_FAULT1_EN	R/W	0	Enables FAULT[1] pin for DPWM 3 PWM-A Fault Detection 0 = External Fault pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
7	PWMA_FAULT0_EN	R/W	0	Enables FAULT[0] pin for DPWM 3 PWM-A Fault Detection 0 = External FaulT pin disabled for fault detection (Default) 1 = External Fault pin enabled for fault detection
6	PWMA_ACOMP_G_EN	R/W	0	Enables Analog Comparator G result for DPWM 3 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
5	PWMA_ACOMP_F_EN	R/W	0	Enables Analog Comparator F result for DPWM 3 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

Table 4-59. DPWM 3 Fault Detection Register (DPWM3FAULTDET) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PWMA_ACOMP_E_EN	R/W	0	Enables Analog Comparator E result for DPWM 3 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
3	PWMA_ACOMP_D_EN	R/W	0	Enables Analog Comparator D result for DPWM 3 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
2	PWMA_ACOMP_C_EN	R/W	0	Enables Analog Comparator C result for DPWM 3 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
1	PWMA_ACOMP_B_EN	R/W	0	Enables Analog Comparator B result for DPWM 3 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection
0	PWMA_ACOMP_A_EN	R/W	0	Enables Analog Comparator A result for DPWM 3 PWM-A Fault detection 0 = Analog Comparator result disabled for fault detection (Default) 1 = Analog Comparator result enabled for fault detection

4.2.26 HFO Fail Detect Register (HFOFAILDET)

Address 00130074

Figure 4-60. HFO Fail Detect Register (HFOFAILDET)

17	1	0
HFO_FAIL_THRESH		HFO_DETECT_EN
R/W-0 0000 0000 1111 1111		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-60. HFO Fail Detect Register (HFOFAILDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-1	HFO_FAIL_THRESH	R/W	0 0000 0000 1111 1111	Configures threshold where a clear flag is used to clear a counter in the Low Frequency Oscillator domain (if LFO counter overflows, a reset will be generated), resolution of threshold equals High Frequency Oscillator period
0	HFO_DETECT_EN	R/W	0	Enables High Frequency Oscillator Failure Detection logic, device will be reset upon detection of an oscillator failure 0 = Disables High Frequency Oscillator Failure Detection (Default) 1 = Enables High Frequency Oscillator Failure Detection

4.2.27 LFO Fail Detect Register (LFOFAILDET)

Address 00130078

Figure 4-61. LFO Fail Detect Register (LFOFAILDET)

6	2	1	0
LFO_FAIL_THRESH		LFO_FAIL_INT_EN	LFO_DETECT_EN
R/W-0 0011		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-61. LFO Fail Detect Register (LFOFAILDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
6-2	LFO_FAIL_THRESH	R/W	0 0011	Configures threshold where a clear flag is used to clear a counter in the High Frequency Oscillator domain (if HFO counter overflows, a reset will be generated), resolution of threshold equals Low Frequency Oscillator period
1	LFO_FAIL_INT_EN	R/W	0	Low Frequency Oscillator Fail Interrupt Enable 0 = Disables Interrupt Generation upon LFO Failure Detection (Default) 1 = Enables Interrupt Generation upon LFO Failure Detection
0	LFO_DETECT_EN	R/W	0	Enables Low Frequency Oscillator Failure Detection logic, interrupt will be generated upon detection of an oscillator failure 0 = Disables Low Frequency Oscillator Failure Detection (Default) 1 = Enables Low Frequency Oscillator Failure Detection

4.2.28 IDE Control Register (IDECTRL)

Address 0013007C

Figure 4-62. IDE Control Register (IDECTRL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DCM_LIMIT_H								DCM_LIMIT_L							
R/W-0000 0000								R/W-0000 0000							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DCM_INT_EN	IDE_KD												
R-00		R/W-0	R/W-0 0000 0000 0000												

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-62. IDE Control Register (IDECTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DCM_LIMIT_H	R/W	0000 0000	Value added to 1-Da value to provide hysteresis for exiting DCM mode
23-16	DCM_LIMIT_L	R/W	0000 0000	Value subtracted from 1-Da value to provide hysteresis for entering DCM mode
15-14	Reserved	R	00	
13	DCM_INT_EN	R/W	0	Enables Discontinuous Conduction Mode (DCM) interrupt generation based on selected Filter outputs 0 = Disables DCM Detection Interrupt (Default) 1 = Enables DCM Detection Interrupt
12-0	IDE_KD	R/W	0 0000 0000 0000	13-bit unsigned value used to calculate the DPWM B Pulse width when configured in IDE Mode. IDE_KD is configured in 4.9 format, with the integer portion of the KD value ranging from 0 to 15 and 9 fractional bits available for the pulse width calculation.

4.2.29 XTAL Fail Detect Register (XTALFAILDET)

Address 0x00130080

Figure 4-63. XTAL Fail Detect Register (XTALFAILDET)

11	10	9	8	7	6	5	4	3	2	1	0
XTAL_FAIL_UPPER_THRESH					XTAL_FAIL_LOWER_THRESH					XTAL_FAIL_INT_EN	XTAL_DETECT_EN
R/W-1 0000					R/W-0 1010					R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-63. XTAL Fail Detect Register (XTALFAILDET) Register Field Descriptions

Bit	Field	Type	Reset	Description
11-7	XTAL_FAIL_UPPER_THRESH	R/W	1 0000	Configures a upper threshold which the MCLK count will be compared to when the XTAL counter sends a clear signal to the MCLK counter, resolution of threshold equals one MCLK period. XTAL counter sends a clear to the MCLK counter every 3 XTAL periods.
6-2	XTAL_FAIL_LOWER_THRESH	R/W	0 1010	Configures a lower threshold which the MCLK count will be compared to when the XTAL counter sends a clear signal to the MCLK counter, resolution of threshold equals one MCLK period. XTAL counter sends a clear to the MCLK counter every 3 XTAL periods.
1	XTAL_FAIL_INT_EN	R/W	0	XTAL Fail Interrupt Enable 0 = Disables Interrupt Generation upon XTAL Failure Detection (Default) 1 = Enables Interrupt Generation upon XTAL Failure Detection
0	XTAL_DETECT_EN	R/W	0	Enables XTAL Failure Detection logic, interrupt will be generated upon detection of an oscillator failure 0 = Disables XTAL Failure Detection (Default) 1 = Enables XTAL Failure Detection

4.3 RTC - Real Time Clock Interface

4.3.1 RTC Control Register (RTCCTRL)

Address FFF7E400

BIAS_R and the CONFIG_CL bitfields must be set to coordinated values. See the data sheet for more information.

Figure 4-64. RTC Control Register (RTCCTRL)

17	16
BIAS_R	
R/W-100	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIAS_R	CONFIG_CL_XOUT					Reserved	CONFIG_CL_XIN					CONFIG_INCL		Reserved	PRESET_EN
R/W-100	R/W-0 1111					R-0	R/W-0 1111					R/W-11		R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-64. RTC Control Register (RTCCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-15	BIAS_R	R/W	100	Selects the bias resistor for the XTAL startup circuit 0 = 403 ohms 1 = 301 ohms 2 = 198 ohms 3 = 99 ohms 4 = 49 ohms (Default) 5 = 49 ohms 6 = 49 ohms 7 = 49 ohms
14-10	CONFIG_CL_XOUT	R/W	0 1111	Increments total load on crystal XOUT from 0 – 40pF. 1 LSB = 2pF. Any code higher than decimal 20 results in 40pF
9	Reserved	R	0	
8-4	CONFIG_CL_XIN	R/W	0 1111	Increments total load on crystal XIN from 0 – 40pF. 1 LSB = 2pF. Any code higher than decimal 20 results in 40pF
3-2	CONFIG_INCL	R/W	11	For analog configuration only 00 = standard crystal operation 01 = standard crystal operation 10 = enables external clock input on XTAL_IN pin 11 = disable (Default)
1	Reserved	R	0	
0	PRESET_EN	R/W	0	Counter preset enable 0 = RTC Preset Disabled (Default) 1 = RTC Preset Enabled

4.3.2 RTC Counter Register (RTCCOUNT)

Address FFF7E404

Figure 4-65. RTC Counter Register (RTCCOUNT)

27	26	25	24	23	22	21	20	19	18	17	16
DAYS											HOURS
R-0											R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HOURS				MINS						SECS					
R-0				R-0						R-0					

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-65. RTC Counter Register (RTCCOUNT) Register Field Descriptions

Bit	Field	Type	Reset	Description
27-17	DAYS	R	0	Current count of days
16-12	HOURS	R	0	Current count of hours
11-6	MINS	R	0	Current count of minutes
5-0	SECS	R	0	Current count of seconds

4.3.3 RTC Preset Register (RTCPRESET)

Address FFF7E408

Figure 4-66. RTC Preset Register (RTCPRESET)

27	26	25	24	23	22	21	20	19	18	17	16
DAYS											HOURS
R-0											R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HOURS				MINS						SECS					
R-0				R-0						R-0					

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-66. RTC Preset Register (RTCPRESET) Register Field Descriptions

Bit	Field	Type	Reset	Description
27-17	DAYS	R/W	0	Preset value of days
16-12	HOURS	R/W	0	Preset value of hours
11-6	MINS	R/W	0	Preset value of minutes
5-0	SECS	R/W	0	Preset value of seconds

4.3.4 RTC Interrupt Enable Register (RTCINTEN)

Address FFF7E40C

Figure 4-67. RTC Interrupt Enable Register (RTCINTEN)

3	2	1	0
SEC60	SEC30	SEC10	SEC
R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-67. RTC Interrupt Enable Register (RTCINTEN) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	SEC60	R/W	0	Enable interrupts every 60 seconds
2	SEC30	R/W	0	Enable interrupts every 30 seconds
1	SEC10	R/W	0	Enable interrupts every 10 seconds
0	SEC	R/W	0	Enable interrupts every 1 second

4.3.5 RTC Interrupt Status Register (RTCINTSTAT)

Address FFF7E410

Figure 4-68. RTC Interrupt Status Register (RTCINTSTAT)

3	2	1	0
SEC60	SEC30	SEC10	SEC
R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-68. RTC Interrupt Status Register (RTCINTSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	SEC60	R	0	Interrupt flag for 60 seconds
2	SEC30	R	0	Interrupt flag for 30 seconds
1	SEC10	R	0	Interrupt flag for 10 seconds
0	SEC	R	0	Interrupt flag for 1 second

4.3.6 RTC Prescale Register (RTCPRESCALE)

Address FFF7E414

Figure 4-69. RTC Prescale Register (RTCPRESCALE)

9	0
PRESCALE	
R/W-10 1100 1111	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-69. RTC Prescale Register (RTCPRESCALE) Register Field Descriptions

Bit	Field	Type	Reset	Description
9-0	PRESCALE	R/W	10 1100 1111	Prescaler value Optimal value for a 10Mhz XTAL is 0x2CF, which counts 10 million reference clock cycles before incrementing the second counter. Each bit increment/decrement from 0x2CF of the prescale value adds or subtracts 8 counts to the rollover value associated with the 1 second counter. Counter rollover adjustments can be made between 0x1CF and 0x3CF, which gives +/- 256 counts to the rollover value. 1 sec count = (10^6 * XtalPeriod) + [(PRESCALE - 0x2CF)*(8 *XtalPeriod)] For example, an ideal 10Mhz clock, 100ns period, would be: 1 sec count = (10^6 * 100ns) + [(PRESCALE - 0x2CF) * (800ns)]

4.4 GIOD - GIO C and D Pins Control

4.4.1 GIO C Control Register (GIOCCTRL)

Address FFF7E608

Figure 4-70. GIO C Control Register (GIOCCTRL)

2	1	0
GIO_C_DIR	GIO_C_VAL	GIO_C_IN
R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-70. GIO C Control Register (GIOCCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
2	GIO_C_DIR	R/W	0	I/O Direction for Pin GPIO_C 0 = Pin is an Output 1 = Pin is an Input
1	GIO_C_VAL	R/W	0	Output Value for Pin GPIO_C 0 = Output is 0 1 = Output is 1
0	GIO_C_IN	R/W	0	State of Pin GPIO_C 0 = Pin is a 0 1 = Pin is a 1

4.4.2 GIO D Control Register (GIODCTRL)

Address FFF7E60C

Figure 4-71. GIO D Control Register (GIODCTRL)

2	1	0
GIO_D_DIR	GIO_D_VAL	GIO_D_IN
R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-71. GIO D Control Register (GIODCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
2	GIO_D_DIR	R/W	0	I/O Direction for Pin GPIOD 0 = Pin is an Output 1 = Pin is an Input
1	GIO_D_VAL	R/W	0	Output Value for Pin GPIOD 0 = Output is 0 1 = Output is 1
0	GIO_D_IN	R/W	0	State of Pin GPIOD 0 = Pin is a 0 1 = Pin is a 1

4.5 SPI – Serial Peripheral Interface

4.5.1 SPI Control Register (SPICTRL)

Address FFF7E800

Figure 4-72. SPI Control Register (SPICTRL)

23	21	20	16
CLKRATE		FRMLEN	
R/W-000		R/W-0 0000	

15	11	10	7	6	5	4	3	2	1	0
RXCNT		TXCNT		WRSTORE	WRSTART	POL	PHA	INTEN	MODE	SPIEN
R/W-0 0000		R/W-0000		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-72. SPI Control Register (SPICTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-21	CLKRATE	R/W	000	Master clock rate relative to ICLK 0 = SCK is ICLK/2 (Default) 1 = SCK is ICLK/4 2 = SCK is ICLK/8 3 = SCK is ICLK/16
20-16	FRMLEN	R/W	0 0000	Sets the number of messages (TXCNT + RXCNT) to hold CS low when acting as SPI Master. SPI Slave does not use these configuration bits.
15-11	RXCNT	R/W	0 0000	Sets the number bytes to receive after TXCNT bytes have been transmitted when acting as SPI Master. Sets the number of bytes that the SPI Slave expects CS to be low.
10-7	TXCNT	R/W	0000	Sets the bytes to transmit from the SPITX registers when acting as SPI Master. SPI Slave does not use these configuration bits.
6	WRSTORE	R/W	0	Places or discards data received during TXCNT when SPI Master. 0 = Data received during TXCNT discarded (Default) 1 = Data received during TXCNT placed in RXBUF
5	WRSTART	R/W	0	Sets which WRREG initiates transfer when SPI master. 0 = Write to SPITX-0 starts message transfer (Default) 1 = Write to SPITX-1 starts message transfer
4	POL	R/W	0	The polarity bit, together with the phase bit, determines the transfer-mode.
3	PHA	R/W	0	The phase bit, together with the polarity bit, determines the transfer-mode.
2	INTEN	R/W	0	Enable interrupt generation to the CPU 0 = Disabled (Default) 1 = Enabled
1	MODE	R/W	0	Configures SPI mode 0 = Master Mode (Default) 1 = Slave mode
0	SPIEN	R/W	0	Enable for SPI Module 0 = Disabled (Default) 1 = Enabled

4.5.2 SPI Status Register (SPISTAT)

Address FFF7E804

Figure 4-73. SPI Status Register (SPISTAT)

7	6	5	4	3	2	1	0
FRMCNT					WRCOL	BUSY	SPIF
R-X					R-X	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-73. SPI Status Register (SPISTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	FRMCNT	R	X	Indicates the number of messages remaining in the FRMLEN before SCS will go inactive. (Only used in SPI Master)
2	WRCOL	R	X	SPI interface is busy
1	BUSY	R	X	SPI interface is busy (Only used in SPI Master)
0	SPIF	R	X	SPI Flag, set when current message is complete. Write a ‘1’ to clear

4.5.3 SPI Pin Function Register (SPIFUNC)

Address FFF7E808

Figure 4-74. SPI Pin Function Register (SPIFUNC)

3	2	1	0
MISO	MOSI	SCS	SCK
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-74. SPI Pin Function Register (SPIFUNC) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	MISO	R/W	0	0 = SPI Mode (default) 1 = GPIO Mode
2	MOSI	R/W	0	0 = SPI Mode (default) 1 = GPIO Mode
1	SCS	R/W	0	0 = SPI Mode (default) 1 = GPIO Mode
0	SCK	R/W	0	0 = SPI Mode (default) 1 = GPIO Mode

4.5.4 SPI Pin Direction Register (SPIDIR)

Address FFF7E80C

Figure 4-75. SPI Pin Direction Register (SPIDIR)

3	2	1	0
MISO	MOSI	SCS	SCK
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-75. SPI Pin Direction Register (SPIDIR) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	MISO	R/W	0	0 = Output in GPIO Mode (default) 1 = Input in GPIO Mode
2	MOSI	R/W	0	0 = Output in GPIO Mode (default) 1 = Input in GPIO Mode
1	SCS	R/W	0	0 = Output in GPIO Mode (default) 1 = Input in GPIO Mode
0	SCK	R/W	0	0 = Output in GPIO Mode (default) 1 = Input in GPIO Mode

4.5.5 SPI Pin GP Out Register (SPIGPOUT)

Address FFF7E810

Figure 4-76. SPI Pin GP Out Register (SPIGPOUT)

3	2	1	0
MISO	MOSI	SCS	SCK
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-76. SPI Pin GP Out Register (SPIGPOUT) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	MISO	R/W	0	0 = Pin driven to 0 when configured as an output in GPIO Mode (default) 1 = Pin driven to 1 when configured as an output in GPIO Mode
2	MOSI	R/W	0	0 = Pin driven to 0 when configured as an output in GPIO Mode (default) 1 = Pin driven to 1 when configured as an output in GPIO Mode
1	SCS	R/W	0	0 = Pin driven to 0 when configured as an output in GPIO Mode (default) 1 = Pin driven to 1 when configured as an output in GPIO Mode
0	SCK	R/W	0	0 = Pin driven to 0 when configured as an output in GPIO Mode (default) 1 = Pin driven to 1 when configured as an output in GPIO Mode

4.5.6 SPI Pin GP In Register (SPIGPIN)

Address FFF7E814

Figure 4-77. SPI Pin GP In Register (SPIGPIN)

3	2	1	0
MISO	MOSI	SCS	SCK
R-X	R-X	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

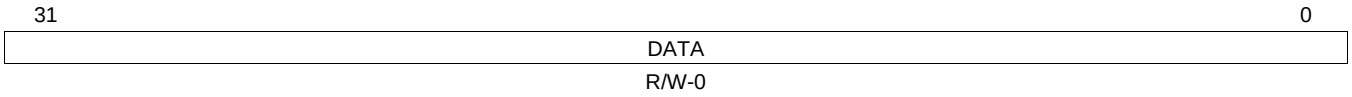
Table 4-77. SPI Pin GP In Register (SPIGPIN) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	MISO	R	X	0= Pin Value is 0 1= Pin Value is 1
2	MOSI	R	X	0= Pin Value is 0 1= Pin Value is 1
1	SCS	R	X	0= Pin Value is 0 1= Pin Value is 1
0	SCK	R	X	0= Pin Value is 0 1= Pin Value is 1

4.5.7 SPI TX Buffer Register 0 (SPITX0)

Address FFF7E818

Figure 4-78. SPI TX Buffer Register 0 (SPITX0)



LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-78. SPI TX Buffer Register 0 (SPITX0) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R?W	0	First 32-bit word to be transmitted in SPI-Master mode. Only 32-bit word to be transmitted in SPI-Slave mode.

4.5.8 SPI TX Buffer Register 1 (SPITX1)

Address FFF7E81C

Figure 4-79. SPI TX Buffer Register 1 (SPITX1)

31	0
DATA	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

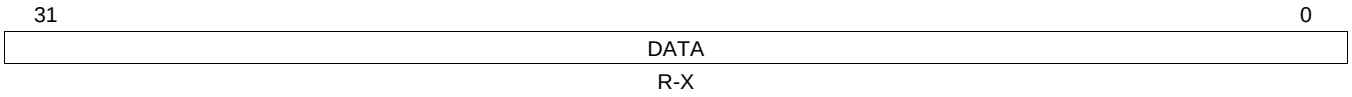
Table 4-79. SPI TX Buffer Register 1 (SPITX1) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0	Second 32-bit word to be transmitted in SPI-Master mode. Not used in SPI-Slave Mode.

4.5.9 SPI Read Buffer Register 0 (SPIRX0)

Address FFF7E820

Figure 4-80. SPI Read Buffer Register 0 (SPIRX0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-80. SPI Read Buffer Register 0 (SPIRX0) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	X	First 32-bit word received in SPI-Master/Slave mode.

4.5.10 SPI Read Buffer Register 1 (SPIRX1)

Address FFF7E824

Figure 4-81. SPI Read Buffer Register 1 (SPIRX1)

31	0
DATA	
R-X	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-81. SPI Read Buffer Register 1 (SPIRX1) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	X	Second 32-bit word received in SPI-Master mode. Not used in SPI-Slave Mode.

4.5.11 SPI Read Buffer Register 2 (SPIRX2)

Address FFF7E828

Figure 4-82. SPI Read Buffer Register 2 (SPIRX2)

31	0
DATA	
R-X	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-82. SPI Read Buffer Register 2 (SPIRX2) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	X	Third 32-bit word received in SPI-Master mode. Not used in SPI-Slave Mode.

4.5.12 SPI Read Buffer Register 3 (SPIRX3)

Address FFF7E82C

Figure 4-83. SPI Read Buffer Register 3 (SPIRX3)

31	0
DATA	
R-X	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-83. SPI Read Buffer Register 3 (SPIRX3) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	X	Fourth 32-bit word received in SPI-Master mode. Not used in SPI-Slave Mode.

4.6 UART Registers Reference

4.6.1 UART Control Register 0 (UARTCTRL0)

Address FFF7EC00 – UART 0 Control Register 0

Address FFF7ED00 – UART 1 Control Register 0

Figure 4-84. UART Control Register 0 (UARTCTRL0)

7	6	5	4	3	2	0
STOP	PARITY	PARITY_ENA	SYNC_MODE	ADDR_MODE	DATA_SIZE	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-84. UART Control Register 0 (UARTCTRL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STOP	R/W	0	Configures stop bits for each frame 0 = One STOP bit included in each frame (Default) 1 = Two STOP bits included in each frame
6	PARITY	R/W	0	Sets odd or even parity 0 = Even parity (Default) 1 = Odd parity
5	PARITY_ENA	R/W	0	Enables parity transmission 0 = No parity bit included in each frame (Default) 1 = One parity bit included in each frame
4	SYNC_MODE	R/W	0	Selects between Synchronous mode and Asynchronous mode 0 = Synchronous (Not supported in UCD3138, set this bit always to one) 1 = Asynchronous
3	ADDR_MODE	R/W	0	Selects between Idle and Address Bit Mode 0 = IDLE Line mode with no Address bit (Default) 1 = Address Bit mode with one Address bit
2-0	DATA_SIZE	R/W	000	Determines the TX and RX byte size 000 = 1 bit of data (Default) 001 = 2 bit of data 010 = 3 bits of data 011 = 4 bits of data 100 = 5 bits of data 101 = 6 bits of data 110 = 7 bits of data 111 = 8 bits of data

4.6.2 UART Receive Status Register (UARTRXST)

Address FFF7EC04 – UART 0 Receive Status Register

Address FFF7ED04 – UART 1 Receive Status Register

Figure 4-85. UART Receive Status Register (UARTRXST)

4	3	2	1	0
RX_IDLE	SLEEP	RX_RDY	RX_WAKE	RX_ENA
R-0	R/W-0	R-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-85. UART Receive Status Register (UARTRXST) Register Field Descriptions

Bit	Field	Type	Reset	Description
4	RX_IDLE	R	0	RX Idle status bit 0 = Not in Rx Idle State 1 = Rx Idle detected
3	SLEEP	R/W	0	Sleep Mode Configuration 0 = Sleep Mode disabled (Default) 1 = Sleep Mode enabled
2	RX_RDY	R	0	UART Receiver ready status bit 0 = UART Receiver not ready 1 = UART Receiver ready
1	RX_WAKE	R	0	UART Receiver wake status bit 0 = UART Receiver has not entered wakeup state 1 = UART Receiver has entered wakeup state
0	RX_ENA	R/W	0	Turns on UART Receiver 0 = UART Receiver disabled (Default) 1 = UART Receiver enabled

4.6.3 UART Transmit Status Register (UARTTXST)

Address FFF7EC08 – UART 0 Transmit Status Register

Address FFF7ED08 – UART 1 Transmit Status Register

Figure 4-86. UART Transmit Status Register (UARTTXST)

7	6	5	4	3	2	1	0
CONTINUE	LOOPBACK	Reserved		TX_EMPTY	TX_RDY	TX_WAKE	TX_ENA
R/W-0	R/W-0	R-00		R-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-86. UART Transmit Status Register (UARTTXST) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONTINUE	R/W	0	Configure operation in suspend mode 0 = Stop transmitting on suspend (Default) 1 = Continue transmitting after initiation of suspend
6	LOOPBACK	R/W	0	Loopback Mode Configuration 0 = Normal mode (Default) 1 = Loopback Mode
5-4	Reserved	R	00	
3	TX_EMPTY	R	0	Transmit buffer status 0 = Transmit buffer is not empty 1 = Transmit buffer is empty
2	TX_RDY	R	0	Transmitter Ready 0 = UART Transmitter is not ready 1 = UART Transmitter is ready to transmit data
1	TX_WAKE	R/W	0	TX wake control bit 0 = UART Transmitter Wakeup disabled (Default) 1 = UART Transmitter Wakeup enabled
0	TX_ENA	R/W	0	Turns on TX module 0 = UART Transmitter Disabled (Default) 1 = UART Transmitter Enabled

4.6.4 UART Control Register 3 (UARTCTRL3)

Address FFF7EC0C – UART 0 Control Register 3

Address FFF7ED0C – UART 1 Control Register 3

Figure 4-87. UART Control Register 3 (UARTCTRL3)

7	6	5	4	3	2	1	0
SW_RESET	POWERDOWN	CLOCK	RX_INT_ENA	TX_INT_ENA	WAKEUP_INT_ENA	BRKDT_INT_ENA	ERR_INT_ENA
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-87. UART Control Register 3 (UARTCTRL3) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_RESET	R/W	0	Software reset for UART Transmitter/Receiver 0 = Disables Software Reset (Default) 1 = Enables Software Reset
6	POWERDOWN	R/W	0	Power-down Transmitter/Receiver Control 0 = Disables Power-down mode (Default) 1 = Enables Power-down mode
5	CLOCK	R/W	0	UART Clock Select 0 = Selects external clock (Default) 1 = Selects internal clock
4	RX_INT_ENA	R/W	0	Enables the interrupts from UART Receiver 0 = Disables interrupts from UART Receiver (Default) 1 = Enables interrupts from UART Receiver
3	TX_INT_ENA	R/W	0	Enables the interrupts from UART Transmitter 0 = Disables interrupts from UART Transmitter (Default) 1 = Enables interrupts from UART Transmitter
2	WAKEUP_INT_ENA	R/W	0	Enables the wakeup interrupt from UART 0 = Disables Wakeup Interrupt (Default) 1 = Enables Wakeup Interrupt
1	BRKDT_INT_ENA	R/W	0	Enables the Broken Circuit interrupt from UART Receiver 0 = Disables Broken Circuit Interrupt (Default) 1 = Enables Broken Circuit Interrupt
0	ERR_INT_ENA	R/W	0	Enables UART Receiver Error Interrupt 0 = Disables UART Receiver Error Interrupt (Default) 1 = Enables UART Receiver Error Interrupt

4.6.5 UART Interrupt Status Register (UARTINTST)

Address FFF7EC10 – UART 0 Interrupt Status Register

Address FFF7ED10 – UART 1 Interrupt Status Register

Figure 4-88. UART Interrupt Status Register (UARTINTST)

7	6	5	4	3	2	1	0
BUS_BUSY	Reserved	FRAME_ERR	OVERRUN_ERR	PARITY_ERR	WAKEUP_INT	BRKDT_INT	RX_ERR
R-0	R-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset
R/C- means that bit can be read or cleared; each of the bits except RXERR and BUS BUSY can be cleared by writing a 1 to the bit.

Table 4-88. UART Interrupt Status Register (UARTINTST) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUS_BUSY	R	0	UART Receiver Busy Indicator 0 = UART Receiver ready to accept new frame 1 = UART Receiver currently processing message
6	Reserved	R	0	
5	FRAME_ERR	R/C	0	UART Receiver Framing Error 0 = No framing error found within incoming data message 1 = Indicates the incoming data message had a framing error
4	OVERRUN_ERR	R/C	0	UART Receiver Buffer Overflow 0 = No overflow condition found in receive buffer 1 = Indicates the receive buffer has overflowed
3	PARITY_ERR	R/C	0	UART Receiver Parity Error 0 = No parity error found on the incoming data message 1 = Indicates a parity error found on the incoming data message
2	WAKEUP_INT	R/C	0	UART Receiver Wakeup Interrupt 0 = No Wakeup Interrupt received from UART Receiver 1 = Wakeup Interrupt received from UART Receiver
1	BRKDT_INT	R/C	0	UART Receiver Broken Circuit Interrupt 0 = No Broken Circuit interrupt received from UART Receiver 1 = Indicates a Broken Circuit interrupt received from UART Receiver
0	RX_ERR	R	0	UART Receiver Error 0 = No UART Receiver Errors detected 1 = Frame Error or Overrun error or Parity Error or Broken Circuit error received from UART Receiver

4.6.6 UART Baud Divisor High Byte Register (UARTHBAUD)

Address FFF7EC14 – UART 0 Baud Divisor High Byte Register

Address FFF7ED14 – UART 1 Baud Divisor High Byte Register

Figure 4-89. UART Baud Divisor High Byte Register (UARTHBAUD)

7	0
BAUD_DIV_H	
R/W-0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-89. UART Baud Divisor High Byte Register (UARTHBAUD) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAUD_DIV_H	R/W	0000 0000	Sets the high byte of the 24 bit baud rate selector

4.6.7 UART Baud Divisor Middle Byte Register (UARTMBAUD)

Address FFF7EC18 – UART 0 Baud Divisor Middle Byte Register

Address FFF7ED18 – UART 1 Baud Divisor Middle Byte Register

Figure 4-90. UART Baud Divisor Middle Byte Register (UARTMBAUD)

7							0
BAUD_DIV_M							
R/W-0000 0000							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-90. UART Baud Divisor Middle Byte Register (UARTMBAUD) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAUD_DIV_M	R/W	0000 0000	Sets the middle byte of the 24 bit baud rate selector

4.6.8 UART Baud Divisor Low Byte Register (UARTLBAUD)

Address FFF7EC1C – UART 0 Baud Divisor Low Byte Register

Address FFF7ED1C – UART 1 Baud Divisor Low Byte Register

Figure 4-91. UART Baud Divisor Low Byte Register (UARTLBAUD)

7							0
BAUD_DIV_L							
R/W-0000 0000							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-91. UART Baud Divisor Low Byte Register (UARTLBAUD) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAUD_DIV_L	R/W	0000 0000	Sets the low byte of the 24 bit baud rate selector

4.6.9 UART Receive Buffer (UARTRXBUF)

Address FFF7EC24 – UART 0 Receive Buffer

Address FFF7ED24 – UART 1 Receive Buffer

Figure 4-92. UART Receive Buffer (UARTRXBUF)

7							0
RXDAT							
R-0							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-92. UART Receive Buffer (UARTRXBUF) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RXDAT	R	0	Contains the last data byte received from the UART Receiver

4.6.10 UART Transmit Buffer (UARTTXBUF)

Address FFF7EC28 – UART 0 Transmit Buffer

Address FFF7ED28 – UART 1 Transmit Buffer

Figure 4-93. UART Transmit Buffer (UARTTXBUF)

7	0
TXDAT	
R/W-0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-93. UART Transmit Buffer (UARTTXBUF) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TXDAT	R/W	0000 0000	Contains the data byte to be transmitted by the UART Transmitter

4.6.11 UART I/O Control Register (UARTIOCTRLRX, UARTIOCTRLTX)

Address FFF7EC30 – UART 0 I/O (RX) Control Register

Address FFF7ED30 – UART 1 I/O (RX) Control Register

Address FFF7EC34 – UART 0 I/O (TX) Control Register

Address FFF7ED34 – UART 1 I/O (TX) Control Register

Figure 4-94. UART I/O Control Register (UARTIOCTRLRX, UARTIOCTRLTX)

3	2	1	0
DATA_IN	DATA_OUT	IO_FUNC	IO_DIR
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-94. UART I/O Control Register (UARTIOCTRLRX, UARTIOCTRLTX) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	DATA_IN	R	0	Data received from pin when configured as GPIO
2	DATA_OUT	R/W	0	Data transmitted to pin when configured as GPIO
1	IO_FUNC	R/W	0	Selects the function for UART pins 0 = GPIO mode (Default) 1 = Normal UART operation
0	IO_DIR	R/W	0	Pin direction when configured as GPIO 0 = Input (Default) 1 = Output

4.6.12 UART Baud Divisor Sub Bits Register (UARTSBAUD)

Address FFF7EC38 – UART 0 Baud Divisor Sub Bits Register

Address FFF7ED38 – UART 1 Baud Divisor Sub Bits Register

Figure 4-95. UART Baud Divisor Sub Bits Register (UARTSBAUD)

2	1	0
BAUD_SUB		
R/W-000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-95. UART Baud Divisor Sub Bits Register (UARTSBAUD) Register Field Descriptions

Bit	Field	Type	Reset	Description
2-0	BAUD_SUB	R/W	000	Each LSB adds one ICLK period to the baud period calculated via the values programed in the UARTHBAUD, UARTMBAUD, and UARTLBAUD registers.

4.6.13 UART RX Control Register 4 (UARTRXCTRL4)

Address FFF7EC3C – UART 0 RX Control Register 4

Address FFF7ED3C – UART 1 RX Control Register 4

Figure 4-96. UART RX Control Register 4 (UARTRXCTRL4)

7 6	5	4 3	2	1	0
RX_CENTER_SAMPLE_EN	RX_CAL_CONTINUOUS_EN	RX_CAL_MODE_BIT_WIDTH	RX_CAL_MODE_EN	Reserved	RX_SYNC_ON_START_EN
R/W-00	R/W-0	R/W-00	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-96. UART RX Control Register 4 (UARTRXCTRL4) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RX_CENTER_SAMPLE_EN	R/W	00	Sample position for the UART RX 00 = Takes 3 samples to the right of the data eye (Default) 01 = Takes 3 samples in the center of the data eye 10 = Takes 3 samples to the left of the data eye 11 = Reserved
5	RX_CAL_CONTINUOUS_EN	R/W	0	Continuously captures baud pulses 0 = Baud pulses will not be captured without a low to high toggle of the RX_CAL_MODE_EN bit. (Default) 1 = Baud pulses will continue to be captured and the updated values will be written to the UARTRXMBAUD, UARTRXLBAUD, and UARTRXSBAUD registers.
4-3	RX_CAL_MODE_BIT_WIDTH	R/W	00	Sets the maximum number of baud periods a pulse (transition on the RX line of 1->0->1 or 0->1->0) can span and still be recorded in the UARTRXMBAUD, UARTRXLBAUD, and UARTRXSBAUD registers. The CAL mode feature helps refine the baud period programmed in the UARTHBAUD, UARTMBAUD, UARTLBAUD, and UARTSBAUD registers. 00 = Captures a low pulse (1->0->1) that spans 1 baud period (Default) 01 = Captures a low pulse (1->0->1) that spans 1-4 baud periods 10 = Captures a low pulse (1->0->1) that spans 1-12 baud periods 11 = Captures a low/high pulse that spans 1 baud period
2	RX_CAL_MODE_EN	R/W	0	Enables the capture feature of the UART. Recorded pulses are stored in the UARTRXMBAUD, UARTRXLBAUD, and UARTRXSBAUD registers. 0 = Disables the capture features of the UART (Default) 1 = Enables the capture feature of the UART
1	Reserved	R	0	
0	RX_SYNC_ON_START_EN	R/W	0	Enables the sync on start feature of the UART RX. Set RX_INDEP_BAUD_EN to ‘1’ and the program the UARTRXMBAUD, UARTRXLBAUD, and UARTRXSBAUD registers with the desired communication speed to utilize this feature. 0 = Start bit is detected based on the free running TX baud rate counter. (Default) 1 = Start bit immediately detected.

4.6.14 UART RX Control Register 5 (UARTRXCTRL5)

Address FFF7EC40 – UART 0 RX Control Register 5

Address FFF7ED40 – UART 1 RX Control Register 5

Figure 4-97. UART RX Control Register 5 (UARTRXCTRL5)

1	0
RX_OVERSAMPLE_ERR	RX_INDEP_BAUD_EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-97. UART RX Control Register 5 (UARTRXCTRL5) Register Field Descriptions

Bit	Field	Type	Reset	Description
1	RX_OVERSAMPLE_ERR	R	0	Indicates when the 3 data samples taken in the eye of the transmission are not identical. 0 = All sampled bits are identical 1 = Sampled bits are not identical
0	RX_INDEP_BAUD_EN	R/W	0	UART RX independent baud rate enabled 0 = Universal baud rate registers are used (UARTHBAUD, UARTMBAUD, and UARTLBAUD) to program both the TX and RX baud rates. One counter is used for both the TX and RX; therefore, sync on start mode must be disabled. (Default) 1 = UART RX baud rate is programmed by the UARTRXMBAUD, UARTRXLBAUD, and UARTRXSBAUD registers. UART TX baud rate is programmed by the UARTHBAUD, UARTMBAUD, UARTLBAUD, and UARTSBAUD registers. Two independent counters are used for the TX and RX; therefore, sync on start mode can be enabled.

4.6.15 UART RX Baud Divisor Middle Byte Register (UARTRXMBAUD)

Address FFF7EC44– UART 0 RX Baud Divisor Middle Byte Register

Address FFF7ED44 – UART 1 RX Baud Divisor Middle Byte Register

Figure 4-98. UART RX Baud Divisor Middle Byte Register (UARTRXMBAUD)

7	6	5	4	3	2	1	0
RX_M_BAUD							
R/W-0000 0000							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-98. UART RX Baud Divisor Middle Byte Register (UARTRXMBAUD) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RX_M_BAUD	R/W	0000 0000	Middle byte of the 16-bit RX baud rate selector. This is a dual purpose register. When RX_INDEP_BAUD_EN = 0 and RX_CAL_MODE_EN = 1 this register is used to read the middle byte of the measured input baud pulse width. When RX_INDEP_BAUD_EN = 1 this register is used to program the middle byte of the 16-bit RX baud rate selector.

4.6.16 UART RX Baud Divisor Low Byte Register (UARTRXLBAUD)

Address FFF7EC48– UART 0 RX Baud Divisor Low Byte Register

Address FFF7ED48 – UART 1 RX Baud Divisor Low Byte Register

Figure 4-99. UART RX Baud Divisor Low Byte Register (UARTRXLBAUD)

7	6	5	4	3	2	1	0
RX_L_BAUD							
R/W-0000 0000							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-99. UART RX Baud Divisor Low Byte Register (UARTRXLBAUD) Register Field Descriptions

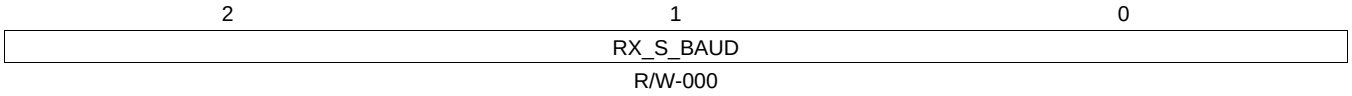
Bit	Field	Type	Reset	Description
7-0	RX_L_BAUD	R/W	0000 0000	Low byte of the 16-bit RX baud rate selector. This is a dual purpose register. When RX_INDEP_BAUD_EN = 0 and RX_CAL_MODE_EN = 1 this register is used to read the low byte of the measured input baud pulse width. When RX_INDEP_BAUD_EN = 1 this register is used to program the low byte of the 16-bit RX baud rate selector.

4.6.17 UART RX Baud Divisor Sub Bits Register (UARTRXSBAUD)

Address FFF7EC4C– UART 0 RX Baud Divisor Sub Bits Register

Address FFF7ED4C – UART 1 RX Baud Divisor Sub Bits Register

Figure 4-100. UART RX Baud Divisor Sub Bits Register (UARTRXSBAUD)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-100. UART RX Baud Divisor Sub Bits Register (UARTRXSBAUD) Register Field Descriptions

Bit	Field	Type	Reset	Description
2-0	RX_S_BAUD	R/W	000	Each LSB adds one ICLK period to the baud period calculated via the values programed in the UARTRXMBAUD and UARTRXLBAUD registers. This is a dual purpose register. When RX_INDEP_BAUD_EN = 0 and RX_CAL_MODE_EN = 1 this register is used to read the sub bits of the measured input baud pulse width. When RX_INDEP_BAUD_EN = 1 this register is used to program the sub bits of the RX baud rate selector.

4.7 ADC Registers

4.7.1 ADC Control Register (ADCCTRL)

Address 00140000

Figure 4-101. ADC Control Register (ADCCTRL)

31	30	29	28	27	26	25	24
EXT_TRIG_DLY							
R/W-0000 0000							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXT_TRIG_GPIO_VAL	EXT_TRIG_GPIO_DIR	EXT_TRIG_GPIO_EN	EXT_TRIG_EN	EXT_TRIG_SEL			
R/W-0	R/W-0	R/W-0	R/W-0	R-0000			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SAMPLING_SEL			ADC_SEL_REF	ADC_ROUND	BYPASS_EN		
R/W-000			R/W-0	R/W-0	R/W-111		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX_CONV				SINGLE_SWEEP	SW_START	ADC_INT_EN	ADC_EN
R/W-0000				R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-101. ADC Control Register (ADCCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	EXT_TRIG_DLY	R/W	0000 0000	8-bit External ADC Trigger Delay configuration, LSB bit resolution equals period of ADC Clock (High Frequency Oscillator Frequency divided by 4)
23	EXT_TRIG_GPIO_VAL	R/W	0	Output value of ADC_EXT_TRIG pin when configured in GPIO mode 0 = ADC_EXT_TRIG pin driven low (Default) 1 = ADC_EXT_TRIG pin driven high
22	EXT_TRIG_GPIO_DIR	R/W	0	Direction of ADC_EXT_TRIG pin when configured in GPIO mode 0 = ADC_EXT_TRIG pin configured as input (Default) 1 = ADC_EXT_TRIG pin configured as output
21	EXT_TRIG_GPIO_EN	R/W	0	Configuration of ADC_EXT_TRIG pin 0 = ADC_EXT_TRIG pin configured in functional mode (Default) 1 = ADC_EXT_TRIG pin configured in GPIO mode
20	EXT_TRIG_EN	R/W	0	External Trigger Enable, conversions are started using the external trigger as selectable by the EXT_TRIG_SEL bits. 0 = Disable External Trigger capability (Default) 1 = Enable External Trigger capability

Table 4-101. ADC Control Register (ADCCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	EXT_TRIG_SEL	R	0000	Selects which external trigger can start a conversion loop. 0 = HS Loop1 Event 1 (DPWMA Low Resolution Edge) (Default) 1 = HS Loop1 Event 3 (DPWMB Low Resolution Edge) 2 = HS Loop2 Event 1 (DPWMA Low Resolution Edge) 3 = HS Loop2 Event 3 (DPWMB Low Resolution Edge) 4 = HS Loop3 Event 1 (DPWMA Low Resolution Edge) 5 = HS Loop3 Event 3 (DPWMB Low Resolution Edge) 6 = HS Loop4 Event 1 (DPWMA Low Resolution Edge) 7 = HS Loop4 Event 3 (DPWMB Low Resolution Edge) 8 = ADC_EXT_TRIG pin 9 = Analog Comparator A Output A = Analog Comparator B Output B = Analog Comparator C Output C = Analog Comparator D Output D = Analog Comparator E Output E = Analog Comparator F Output F = Analog Comparator G Output
15-13	SAMPLING_SEL	R/W	000	Defines ADC sampling and hold timing setup 111 = 539KS/s 110 = 267KS/s 101 = 530KS/s 100 = 267KS/s 011 = 504KS/s 010 = 453KS/s 001 = 422KS/s 000 = 267KS/s (Default)
12	ADC_SEL_REF	R/W	0	ADC Voltage Reference Select 0= Selects Internal ADC voltage reference (Default) 1 = Selects AVDD as ADC voltage reference
11	ADC_ROUND	R/W	0	Enables rounding of ADC Result to 10 bits 0 = ADC Results are not rounded (Default) 1 = ADC Results are rounded to 10 most significant bits
10-8	BYPASS_EN	R/W	111	Enables dual sample/hold for specific channels. There are only four valid settings: 011 = Dual Sample/Hold enabling on Channel 2 101 = Dual Sample/Hold enabling on Channel 1 110 = Dual Sample/Hold enabling on Channel 0 111 = Dual Sample/Hold Disabled (Default)
7-4	MAX_CONV	R/W	0000	Maximum number of conversion done in one conversion loop 0x0 = 1 conversion selection converted in the loop (Default) 0xF = All 16 conversion selections converted in the loop
3	SINGLE_SWEEP	R/W	0	ADC Conversion Mode 0 = Continuous conversion loop runs (Default) 1 = Single conversion loop run
2	SW_START	R/W	0	Firmware ADC Conversion Start, bit will be cleared automatically by hardware at end of ADC conversion 0 = Conversions not initiated by firmware (Default) 1 = Initiate an ADC conversion loop
1	ADC_INT_EN	R/W	0	End-of-conversion Interrupt Enable 0 = Disable End-of-Conversion Interrupt (Default) 1 = Enable End-of-Conversion Interrupt

Table 4-101. ADC Control Register (ADCCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADC_EN	R/W	0	ADC12 Enable Control 0 = Disables ADC (Default) 1 = Enables ADC

4.7.2 ADC Status Register (ADCSTAT)

Address 00140004

Figure 4-102. ADC Status Register (ADCSTAT)

6 3	2	1	0
CURRENT_CH	ADC_EXT_TRIG_VAL	ADC_INT_RAW	ADC_INT
R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-102. ADC Status Register (ADCSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
6-3	CURRENT_CH	R	0	Register shows the currently converting channel
2	ADC_EXT_TRIG_VAL	R	0	ADC_EXT_TRIG pin value 0 = ADC_EXT_TRIG pin driven low 1 = ADC_EXT_TRIG pin driven high
1	ADC_INT_RAW	R	0	End-of-conversion interrupt flag, raw version 0 = No End-of-conversion interrupt detected 1 = End-of-conversion interrupt found
0	ADC_INT	R	0	End-of-conversion interrupt flag, latched version 0 = No End-of-conversion interrupt detected 1 = End-of-conversion interrupt found

4.7.3 ADC Test Control Register (ADCTSTCTRL)

Address 00140008

Figure 4-103. ADC Test Control Register (ADCTSTCTRL)

1	0
ADC_SH_BUFFER_EN	Reserved
R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-103. ADC Test Control Register (ADCTSTCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
1	ADC_SH_BUFFER_EN	R/W	0	ADC Sample and Hold Buffer Enable 0 = Disable ADC Sample and Hold Buffer (Default) 1 = Enables ADC Sample and Hold Buffer
0	Reserved	R	0	

4.7.4 ADC Sequence Select Register 0 (ADCSEQSEL0)

Address 0014000C

Figure 4-104. ADC Sequence Select Register 0 (ADCSEQSEL0)

28	27 24	23 21	20	19 16
SEQ3_SH	SEQ3	Reserved	SEQ2_SH	SEQ2
R/W-0	R/W-0000	R-000	R/W-0	R/W-0000

15 13	12	11 8	7 5	4	3 0
Reserved	SEQ1_SH	SEQ1	Reserved	SEQ0_SH	SEQ0
R-000	R/W-0	R/W-0000	R-000	R/W-0	R/W-0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-104. ADC Sequence Select Register 0 (ADCSEQSEL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
28	SEQ3_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
27-24	SEQ3	R/W	0000	Channel to be converted fourth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
23-21	Reserved	R	000	
20	SEQ2_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
19-16	SEQ2	R/W	0000	Channel to be converted third 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
15-13	Reserved	R	000	
12	SEQ1_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
11-8	SEQ1	R/W	0000	Channel to be converted second 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
7-5	Reserved	R	000	
4	SEQ0_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
3-0	SEQ0	R/W	0000	Channel to be converted first 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected

4.7.5 ADC Sequence Select Register 1 (ADCSEQSEL1)

Address 00140010

Figure 4-105. ADC Sequence Select Register 1 (ADCSEQSEL1)

28	27–24	23–21	20	19–16
SEQ7_SH	SEQ7	Reserved	SEQ6_SH	SEQ6
R/W-0	R/W-0000	R-000	R/W-0	R/W-0000

15–13	12	11–8	7–5	4	3–0
Reserved	SEQ5_SH	SEQ5	Reserved	SEQ4_SH	SEQ4
R-000	R/W-0	R/W-0000	R-000	R/W-0	R/W-0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-105. ADC Sequence Select Register 1 (ADCSEQSEL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
28	SEQ7_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
27-24	SEQ7	R/W	0000	Channel to be converted eighth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
23-21	Reserved	R	000	
20	SEQ6_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
19-16	SEQ6	R/W	0000	Channel to be converted seventh 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
15-13	Reserved	R	000	
12	SEQ5_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
11-8	SEQ5	R/W	0000	Channel to be converted sixth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
7-5	Reserved	R	000	
4	SEQ4_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
3-0	SEQ4	R/W	0000	Channel to be converted fifth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected

4.7.6 ADC Sequence Select Register 2 (ADCSEQSEL2)

Address 00140014

Figure 4-106. ADC Sequence Select Register 2 (ADCSEQSEL2)

28	27 24	23 21	20	19 16
SEQ11_SH	SEQ11	Reserved	SEQ10_SH	SEQ10
R/W-0	R/W-0000	R-000	R/W-0	R/W-0000

15 13	12	11 8	7 5	4	3 0
Reserved	SEQ9_SH	SEQ9	Reserved	SEQ8_SH	SEQ8
R-000	R/W-0	R/W-0000	R-000	R/W-0	R/W-0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-106. ADC Sequence Select Register 2 (ADCSEQSEL2) Register Field Descriptions

Bit	Field	Type	Reset	Description
28	SEQ11_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
27-24	SEQ11	R/W	0000	Channel to be converted twelfth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
23-21	Reserved	R	000	
20	SEQ10_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
19-16	SEQ10	R/W	0000	Channel to be converted eleventh 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
15-13	Reserved	R	000	
12	SEQ9_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
11-8	SEQ9	R/W	0000	Channel to be converted tenth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
7-5	Reserved	R	000	
4	SEQ8_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
3-0	SEQ8	R/W	0000	Channel to be converted ninth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected

4.7.7 ADC Sequence Select Register 3 (ADCSEQSEL3)

Address 00140018

Figure 4-107. ADC Sequence Select Register 3 (ADCSEQSEL3)

28	27 24	23 21	20	19 16
SEQ15_SH	SEQ15	Reserved	SEQ14_SH	SEQ14
R/W-0	R/W-0000	R-000	R/W-0	R/W-0000

15 13	12	11 8	7 5	4	3 0
Reserved	SEQ13_SH	SEQ13	Reserved	SEQ12_SH	SEQ12
R-000	R/W-0	R/W-0000	R-000	R/W-0	R/W-0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-107. ADC Sequence Select Register 3 (ADCSEQSEL3) Register Field Descriptions

Bit	Field	Type	Reset	Description
28	SEQ15_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
27-24	SEQ15	R/W	0000	Channel to be converted sixteenth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
23-21	Reserved	R	000	
20	SEQ14_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
19-16	SEQ14	R/W	0000	Channel to be converted fifteenth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
15-13	Reserved	R	000	
12	SEQ13_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
11-8	SEQ13	R/W	0000	Channel to be converted fourteenth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected
7-5	Reserved	R	000	
4	SEQ12_SH	R/W	0	Dual channel sequence select 0 = Not selected for Dual Sampling (Default) 1 = Selected for Dual Sampling
3-0	SEQ12	R/W	0000	Channel to be converted thirteenth 0000 = ADC00 selected (Default) 0001 = ADC01 selected ……. 1111 = Temperature Sensor selected

4.7.8 ADC Result Registers 0-15 (ADCRESULTx, x=0:15)

Address 0014001C – ADC Result Register 0

Address 00140020 – ADC Result Register 1

Address 00140024 – ADC Result Register 2

Address 00140028 – ADC Result Register 3

Address 0014002C – ADC Result Register 4

Address 00140030 – ADC Result Register 5

Address 00140034 – ADC Result Register 6

Address 00140038 – ADC Result Register 7

Address 0014003C – ADC Result Register 8

Address 00140040 – ADC Result Register 9

Address 00140044 – ADC Result Register 10

Address 00140048 – ADC Result Register 11

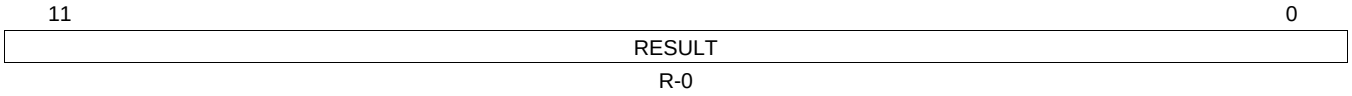
Address 0014004C – ADC Result Register 12

Address 00140050 – ADC Result Register 13

Address 00140054 – ADC Result Register 14

Address 00140058 – ADC Result Register 15

Figure 4-108. ADC Result Registers 0-15 (ADCRESULTx, x=0:15)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-108. ADC Result Registers 0-15 (ADCRESULTx, x=0:15) Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	RESULT	R	0	Each sequence has a dedicated result register.

4.7.9 ADC Averaged Result Registers 0-5 (ADCAVGRESULTx, x=0:15)

Address 0014005C – ADC Averaged Result Register 0

Address 00140060 – ADC Averaged Result Register 1

Address 00140064 – ADC Averaged Result Register 2

Address 00140068 – ADC Averaged Result Register 3

Address 0014006C – ADC Averaged Result Register 4

Address 00140070 – ADC Averaged Result Register 5

Figure 4-109. ADC Averaged Result Registers 0-5 (ADCAVGRESULTx, x=0:15)

11	0
RESULT	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-109. ADC Averaged Result Registers 0-5 (ADCAVGRESULTx, x=0:15) Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	RESULT	R	0	First 6 ADC Results have an averaged result

4.7.10 ADC Digital Compare Limits Register 0-5 (ADCCOMPLIMx, x=0:5)

Address 00140074 – ADC Digital Compare Limits Register 0

Address 00140078 – ADC Digital Compare Limits Register 1

Address 0014007C – ADC Digital Compare Limits Register 2

Address 00140080 – ADC Digital Compare Limits Register 3

Address 00140084 – ADC Digital Compare Limits Register 4

Address 00140088 – ADC Digital Compare Limits Register 5

Figure 4-110. ADC Digital Compare Limits Register 0-5 (ADCCOMPLIMx, x=0:5)

27 16	15 12	11 0
UPPER_LIMIT	Reserved	LOWER_LIMIT
R/W-1111 1111 1111	R-0000	R/W-0000 0000 0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-110. ADC Digital Compare Limits Register 0-5 (ADCCOMPLIMx, x=0:5) Register Field Descriptions

Bit	Field	Type	Reset	Description
27-16	UPPER_LIMIT	R/W	1111 1111 1111	Configures the upper limit value. If the ADC conversion selected is equal or greater than the limit, the Digital Compare Interrupt Flag is set (bit 22 of ADC Control Register 1). Results of comparison can be read from the ADC Digital Compare Results Register (see Section 4.7.12).
15-12	Reserved	R	0000	
11-0	LOWER_LIMIT	R/W	0000 0000 0000	Configures the lower limit value. If the ADC conversion selected is equal or less than the limit, the Digital Compare Interrupt Flag is set (bit 22 of ADC Control Register 1). Results of comparison can be read from the ADC Digital Compare Results Register (see Section 4.7.12).

4.7.11 ADC Digital Compare Enable Register (ADCCOMPEN)

Address 0014008C

Figure 4-111. ADC Digital Compare Enable Register (ADCCOMPEN)

27	26	25	24
COMP5_UP_INT_EN	COMP5_LO_INT_EN	COMP4_UP_INT_EN	COMP4_LO_INT_EN
R/W-0	R/W-0	R/W-0	R/W-0

23	22	21	20	19	18	17	16
COMP3_UP_INT_EN	COMP3_LO_INT_EN	COMP2_UP_INT_EN	COMP2_LO_INT_EN	COMP1_UP_INT_EN	COMP1_LO_INT_EN	COMP0_UP_INT_EN	COMP0_LO_INT_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8
Reserved		COMP5_DATA_SEL	COMP4_DATA_SEL	COMP3_DATA_SEL	COMP2_DATA_SEL	COMP1_DATA_SEL	COMP0_DATA_SEL
R-00		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
Reserved		COMP5_EN	COMP4_EN	COMP3_EN	COMP2_EN	COMP1_EN	COMP0_EN
R-00		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-111. ADC Digital Compare Enable Register (ADCCOMPEN) Register Field Descriptions

Bit	Field	Type	Reset	Description
27	COMP5_UP_INT_EN	R/W	0	Digital Comparator 5 Upper Limit Interrupt Enable 0 = Interrupt generation disabled on result above upper limit (Default) 1 = Interrupt generation enabled on result above upper limit
26	COMP5_LO_INT_EN	R/W	0	Digital Comparator 5 Lower Limit Interrupt Enable 0 = Interrupt generation disabled on result below lower limit (Default) 1 = Interrupt generation enabled on result below lower limit
25	COMP4_UP_INT_EN	R/W	0	Digital Comparator 4 Upper Limit Interrupt Enable 0 = Interrupt generation disabled on result above upper limit (Default) 1 = Interrupt generation enabled on result above upper limit
24	COMP4_LO_INT_EN	R/W	0	Digital Comparator 4 Lower Limit Interrupt Enable 0 = Interrupt generation disabled on result below lower limit (Default) 1 = Interrupt generation enabled on result below lower limit
23	COMP3_UP_INT_EN	R/W	0	Digital Comparator 3 Upper Limit Interrupt Enable 0 = Interrupt generation disabled on result above upper limit (Default) 1 = Interrupt generation enabled on result above upper limit
22	COMP3_LO_INT_EN	R/W	0	Digital Comparator 3 Lower Limit Interrupt Enable 0 = Interrupt generation disabled on result below lower limit (Default) 1 = Interrupt generation enabled on result below lower limit
21	COMP2_UP_INT_EN	R/W	0	Digital Comparator 2 Upper Limit Interrupt Enable 0 = Interrupt generation disabled on result above upper limit (Default) 1 = Interrupt generation enabled on result above upper limit
20	COMP2_LO_INT_EN	R/W	0	Digital Comparator 2 Lower Limit Interrupt Enable 0 = Interrupt generation disabled on result below lower limit (Default) 1 = Interrupt generation enabled on result below lower limit
19	COMP1_UP_INT_EN	R/W	0	Digital Comparator 1 Upper Limit Interrupt Enable 0 = Interrupt generation disabled on result above upper limit (Default) 1 = Interrupt generation enabled on result above upper limit
18	COMP1_LO_INT_EN	R/W	0	Digital Comparator 1 Lower Limit Interrupt Enable 0 = Interrupt generation disabled on result below lower limit (Default) 1 = Interrupt generation enabled on result below lower limit

Table 4-111. ADC Digital Compare Enable Register (ADCCOMPEN) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	COMP0_UP_INT_EN	R/W	0	Digital Comparator 0 Upper Limit Interrupt Enable 0 = Interrupt generation disabled on result above upper limit (Default) 1 = Interrupt generation enabled on result above upper limit
16	COMP0_LO_INT_EN	R/W	0	Digital Comparator 0 Lower Limit Interrupt Enable 0 = Interrupt generation disabled on result below lower limit (Default) 1 = Interrupt generation enabled on result below lower limit
15-14	Reserved	R	00	
13	COMP5_DATA_SEL	R/W	0	Digital Comparator 5 Data Select 0 = Raw ADC Result 5 used for comparison (Default) 1 = Averaged ADC Result 5 used for comparison
12	COMP4_DATA_SEL	R/W	0	Digital Comparator 4 Data Select 0 = Raw ADC Result 4 used for comparison (Default) 1 = Averaged ADC Result 4 used for comparison
11	COMP3_DATA_SEL	R/W	0	Digital Comparator 3 Data Select 0 = Raw ADC Result 3 used for comparison (Default) 1 = Averaged ADC Result 3 used for comparison
10	COMP2_DATA_SEL	R/W	0	Digital Comparator 2 Data Select 0 = Raw ADC Result 2 used for comparison (Default) 1 = Averaged ADC Result 2 used for comparison
9	COMP1_DATA_SEL	R/W	0	Digital Comparator 1 Data Select 0 = Raw ADC Result 1 used for comparison (Default) 1 = Averaged ADC Result 1 used for comparison
8	COMP0_DATA_SEL	R/W	0	Digital Comparator 0 Data Select 0 = Raw ADC Result 0 used for comparison (Default) 1 = Averaged ADC Result 0 used for comparison
7-6	Reserved	R	00	
5	COMP5_EN	R/W	0	Digital Comparator 5 Enable 0 = Comparator Disabled (Default) 1 = Comparator Enabled
4	COMP4_EN	R/W	0	Digital Comparator 4 Enable 0 = Comparator Disabled (Default) 1 = Comparator Enabled
3	COMP3_EN	R/W	0	Digital Comparator 3 Enable 0 = Comparator Disabled (Default) 1 = Comparator Enabled
2	COMP2_EN	R/W	0	Digital Comparator 2 Enable 0 = Comparator Disabled (Default) 1 = Comparator Enabled
1	COMP1_EN	R/W	0	Digital Comparator 1 Enable 0 = Comparator Disabled (Default) 1 = Comparator Enabled
0	COMP0_EN	R/W	0	Digital Comparator 0 Enable 0 = Comparator Disabled (Default) 1 = Comparator Enabled

4.7.12 ADC Digital Compare Results Register (ADCCOMPRESULT)

Address 00140090

Figure 4-112. ADC Digital Compare Results Register (ADCCOMPRESULT)

27	26	25	24
DCOMP5_UP_RAW	DCOMP5_LO_RAW	DCOMP4_UP_RAW	DCOMP4_LO_RAW
R-0	R-0	R-0	R-0

23	22	21	20	19	18	17	16
DCOMP3_UP_RAW	DCOMP3_LO_RAW	DCOMP2_UP_RAW	DCOMP2_LO_RAW	DCOMP1_UP_RAW	DCOMP1_LO_RAW	DCOMP0_UP_RAW	DCOMP0_LO_RAW
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

15	12	11	10	9	8
Reserved		DCOMP5_UP_INT	DCOMP5_LO_INT	DCOMP4_UP_INT	DCOMP4_LO_INT
R-0000		R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
DCOMP3_UP_INT	DCOMP3_LO_INT	DCOMP2_UP_INT	DCOMP2_LO_INT	DCOMP1_UP_INT	DCOMP1_LO_INT	DCOMP0_UP_INT	DCOMP0_LO_INT
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-112. ADC Digital Compare Results Register (ADCCOMPRESULT) Register Field Descriptions

Bit	Field	Type	Reset	Description
27	DCOMP5_UP_RAW	R	0	Digital Comparator 5 Upper Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
26	DCOMP5_LO_RAW	R	0	Digital Comparator 5 Lower Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
25	DCOMP4_UP_RAW	R	0	Digital Comparator 4 Upper Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
24	DCOMP4_LO_RAW	R	0	Digital Comparator 4 Lower Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
23	DCOMP3_UP_RAW	R	0	Digital Comparator 3 Upper Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
22	DCOMP3_LO_RAW	R	0	Digital Comparator 3 Lower Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
21	DCOMP2_UP_RAW	R	0	Digital Comparator 2 Upper Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
20	DCOMP2_LO_RAW	R	0	Digital Comparator 2 Lower Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
19	DCOMP1_UP_RAW	R	0	Digital Comparator 1 Upper Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded

Table 4-112. ADC Digital Compare Results Register (ADCCOMPRESULT) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	DCOMP1_LO_RAW	R	0	Digital Comparator 1 Lower Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
17	DCOMP0_UP_RAW	R	0	Digital Comparator 0 Upper Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
16	DCOMP0_LO_RAW	R	0	Digital Comparator 0 Lower Limit Raw Result 0 = Limit not exceeded 1 = Limit exceeded
15-12	Reserved	R	0000	
11	DCOMP5_UP_INT	R	0	Digital Comparator 5 Upper Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
10	DCOMP5_LO_INT	R	0	Digital Comparator 5 Lower Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
9	DCOMP4_UP_INT	R	0	Digital Comparator 4 Upper Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
8	DCOMP4_LO_INT	R	0	Digital Comparator 4 Lower Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
7	DCOMP3_UP_INT	R	0	Digital Comparator 3 Upper Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
6	DCOMP3_LO_INT	R	0	Digital Comparator 3 Lower Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
5	DCOMP2_UP_INT	R	0	Digital Comparator 2 Upper Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
4	DCOMP2_LO_INT	R	0	Digital Comparator 2 Lower Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
3	DCOMP1_UP_INT	R	0	Digital Comparator 1 Upper Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
2	DCOMP1_LO_INT	R	0	Digital Comparator 1 Lower Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
1	DCOMP0_UP_INT	R	0	Digital Comparator 0 Upper Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded
0	DCOMP0_LO_INT	R	0	Digital Comparator 0 Lower Limit Interrupt Result, cleared on read 0 = Limit not exceeded 1 = Limit exceeded

4.7.13 ADC Averaging Control Register (ADCAVGCTRL)

Address 00140094

Figure 4-113. ADC Averaging Control Register (ADCAVGCTRL)

22	21	20	19	18	17	16
AVG5_CONFIG		AVG5_EN	Reserved	AVG4_CONFIG		AVG4
R/W-00		R/W-0	R-0	R/W-00		R/W-0
15	14	13	12	11	10	9	8
Reserved	AVG3_CONFIG		AVG3_EN	Reserved	AVG2_CONFIG		AVG2
R-0	R/W-00		R/W-0	R-0	R/W-00		R/W-0
7	6	5	4	3	2	1	0
Reserved	AVG1_CONFIG		AVG1_EN	Reserved	AVG0_CONFIG		AVG0
R-0	R/W-00		R/W-0	R-0	R/W-00		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-113. ADC Averaging Control Register (ADCAVGCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
22-21	AVG5_CONFIG	R/W	00	ADC Averaging Module 5 Configuration 0 = Moving average of 4 samples (Default) 1 = Moving average of 8 samples 2 = Moving average of 16 samples 3 = Moving average of 32 samples
20	AVG5_EN	R/W	0	ADC Averaging Module 5 Enable 0 = ADC Averaging Disabled (Default) 1 = ADC Averaging Enabled
19	Reserved	R	0	
18-17	AVG4_CONFIG	R/W	00	ADC Averaging Module 4 Configuration 0 = Moving average of 4 samples (Default) 1 = Moving average of 8 samples 2 = Moving average of 16 samples 3 = Moving average of 32 samples
16	AVG4_EN	R/W	0	ADC Averaging Module 4 Enable 0 = ADC Averaging Disabled (Default) 1 = ADC Averaging Enabled
15	Reserved	R	0	
14-13	AVG3_CONFIG	R/W	00	ADC Averaging Module 3 Configuration 0 = Moving average of 4 samples (Default) 1 = Moving average of 8 samples 2 = Moving average of 16 samples 3 = Moving average of 32 samples
12	AVG3_EN	R/W	0	ADC Averaging Module 3 Enable 0 = ADC Averaging Disabled (Default) 1 = ADC Averaging Enabled
11	Reserved	R	0	
10-9	AVG2_CONFIG	R/W	00	ADC Averaging Module 2 Configuration 0 = Moving average of 4 samples (Default) 1 = Moving average of 8 samples 2 = Moving average of 16 samples 3 = Moving average of 32 samples
8	AVG2_EN	R/W	0	ADC Averaging Module 4 Enable 0 = ADC Averaging Disabled (Default) 1 = ADC Averaging Enabled

Table 4-113. ADC Averaging Control Register (ADCAVGCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	Reserved	R	0	
6-5	AVG1_CONFIG	R/W	00	ADC Averaging Module 1 Configuration 0 = Moving average of 4 samples (Default) 1 = Moving average of 8 samples 2 = Moving average of 16 samples 3 = Moving average of 32 samples
4	AVG1_EN	R/W	0	ADC Averaging Module 1 Enable 0 = ADC Averaging Disabled (Default) 1 = ADC Averaging Enabled
3	Reserved	R	0	
2-1	AVG0_CONFIG	R/W	00	ADC Averaging Module 0 Configuration 0 = Moving average of 4 samples (Default) 1 = Moving average of 8 samples 2 = Moving average of 16 samples 3 = Moving average of 32 samples
0	AVG0_EN	R/W	0	ADC Averaging Module 0 Enable 0 = ADC Averaging Disabled (Default) 1 = ADC Averaging Enabled

4.8 DPWM 0-3 Registers Reference

4.8.1 DPWM Control Register 0 (DPWMCTRL0)

Address 00150000 – DPWM 3 Control Register 0

Address 00170000 – DPWM 2 Control Register 0

Address 001A0000 – DPWM 1 Control Register 0

Address 001D0000 – DPWM 0 Control Register 0

Figure 4-114. DPWM Control Register 0 (DPWMCTRL0)

31	30	29	28	27	26	25	24
PWM_B_INTRA_MUX				PWM_A_INTR4_MUX			
R/W-0000				R/W-0000			
23	22	21	20	19	18	17	16
CBC_PWM_C_EN	RESERVED		CBC_PWM_AB_EN	CBC_ADV_CNT_EN	MIN_DUTY_MODE		RESERVED
R/W-000	R-0		R/W-0	R/W-0	R/W-00		R-0
15	14	13	12	11	10	9	8
MSYNC_SLAVE_EN	D_ENABLE	RESERVED	RESON_MODE_FIXED_DUTY_EN	PWM_B_FLT_POL	PWM_A_FLT_POL	BLANK_B_EN	BLANK_A_EN
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
PWM_MODE				PWM_B_INV	PWM_A_INV	CLA_EN	PWM_EN
R/W-0010				R/W-0	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-114. DPWM Control Register 0 (DPWMCTRL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PWM_B_INTRA_MUX	R/W	0000	Interchanges DPWM signals post edge generation 0 = Pass-through (Default) 1 = Edge-gen output, this module 2 = PWM-C, this module 3 = Crossover, this module 4 = Pass-through below A 5 = Pass-through below B 6 = Pass-through below C 7 = Pass-through below level-2 C 8 = Pass-through below level-3 C
27-24	PWM_A_INTR4_MUX	R/W	0000	Combines DPWM signals are prior to HR module 0 = Pass-through (Default) 1 = Edge-gen output, this module 2 = PWM-C, this module 3 = Crossover, this module 4 = Pass-through below A 5 = Pass-through below B 6 = Pass-through below C 6 = Pass-through below C 7 = Pass-through below level-2 C 8 = Pass-through below level-3 C
23	CBC_PWM_C_EN	R/W	000	Sets if Fault CBC changes output waveform for PWM-C 0 = PWM-C unaffected by Fault CBC (Default) 1 = PWM-C affected by Fault CBC
22-21	RESERVED	R	0	

Table 4-114. DPWM Control Register 0 (DPWMCTRL0) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	CBC_PWM_AB _EN	R/W	0	Sets if Fault CBC changes output waveform for PWM-A and PWM-B 0 = PWM-A and PWM-B unaffected by Fault CBC (Default) 1 = PWM-A and PWM-B affected by Fault CBC
19	CBC_ADV_CNT _EN	R/W	0	Selects cycle-by-cycle of operation **Normal Mode** 0 = CBC disabled (Default) 1 = CBC enabled **Multi and Resonant Modes** 0 = PWM-A and PWM-B operate independently (Default) 1 = PWM-A and PWM-B pulse matching enabled
18-17	MIN_DUTY _MODE	R/W	00	Minimum Duty Cycle Mode 00 = Suppression of minimum duty cycles is disabled (Default) 01 = CLA value is clamped to zero when below input value is less than MIN_DUTY_LOW 10 = CLA value is clamped to MIN_DUTY_LOW register value when input value is less than MIN_DUTY_LOW
16	RESERVED	R	0	
15	MSYNC_SLAVE _EN	R/W	0	Multi-Sync Slave Mode Control 0 = PWM not synchronized to another PWM channel (Default) 1 = Enable Multi-Sync Slave Mode, current channel will be slaved from corresponding channel
14	D_ENABLE	R/W	0	Converts CLA duty value to DPWM as period-CLA duty value 0 = Value used for event calculations if CLA Duty (Default) 1 = Value used for event calculations is period minus CLA duty value
13	RESERVED	R	0	
12	RESON_MODE _FIXED_DUTY _EN	R/W	0	Configures how duty cycle is controlled in Resonance Mode 0 = Resonant mode duty cycle set by Filter duty (Default) 1 = Resonant mode duty cycle set by Auto Switch High Register
11	PWM_B_FLT_POL	R/W	0	Sets the fault output polarity during a disable condition (i.e. fault or module disabled) 0 = PWM B fault output polarity is set to low (Default) 1 = PWM B fault output polarity is set to high
10	PWM_A_FLT_POL	R/W	0	Sets the fault output polarity during a disable condition (i.e. fault or module disabled) 0 = PWM A fault output polarity is set to low (Default) 1 = PWM A fault output polarity is set to high
9	BLANK_B_EN	R/W	0	Comparator Blanking Window B Enable 0 = Comparator Blanking Window for PWM-B Disabled (Default) 1 = Comparator Blanking Window for PWM-B Enabled
8	BLANK_A_EN	R/W	0	Comparator Blanking Window A Enable 0 = Comparator Blanking Window for PWM-A Disabled (Default) 1 = Comparator Blanking Window for PWM-B Enabled
7-4	PWM_MODE	R/W	0010	DPWM Mode 0 = Normal Mode 1 = Resonant Mode 2 = Multi-Output Mode (Default) 3 = Triangular Mode 4 = Leading Mode
3	PWM_B_INV	R/W	0	PWM B Output Polarity Control 0 = Non-inverted PWM B output (Default) 1 = Inverts PWM B output

Table 4-114. DPWM Control Register 0 (DPWMCTRL0) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PWM_A_INV	R/W	0	PWM A Output Polarity Control 0 = Non-inverted PWM A output (Default) 1 = Inverted PWM A output
1	CLA_EN	R/W	1	CLA Processing Enable 0 = Generate PWM waveforms from PWM Register values 1 = Enable CLA input (Default)
0	PWM_EN	R/W	0	PWM Processing Enable 0 = Disable PWM module, outputs zero (Default) 1 = Enable PWM operation

4.8.2 DPWM Control Register 1 (DPWMCTRL1)

Address 00150004 – DPWM 3 Control Register 1

Address 00170004 – DPWM 2 Control Register 1

Address 001A0004 – DPWM 1 Control Register 1

Address 001D0004 – DPWM 0 Control Register 1

Figure 4-115. DPWM Control Register 1 (DPWMCTRL1)

31	30	29	28	27	26	25	24
PRESET_EN	SYNC_FET_EN	BURST_EN	CLA_DUTY_ADJ_EN	SYNC_OUT_DIV_SEL			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0000			
23	22	21	20	19	18	17	16
CLA_SCALE			EXT_SYNC_EN	CBC_BSIDE_ACTIVE EN	AUTO_MODE_SEL	RESERVED	EVENT_UP_SEL
R/W-000			R/W-0	R/W-0	R/W-0	R-0	R/W-1
15	14	13	12	11	10	9	8
CHECK_OVERRIDE	GLOBAL_PERIOD_EN	PWM_B_OE	PWM_A_OE	GPIO_B_VAL	GPIO_B_EN	GPIO_A_VAL	GPIO_A_EN
R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
PWM_HR_MULTI_OUT_EN	SFRAME_EN	PWM_B_PROT_DIS	PWM_A_PROT_DIS	HIRES_SCALE		ALL_PHASE_CLK_ENA	HIRES_DIS
R/W-0	R/W-0	R/W-0	R/W-0	R/W-00		R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-115. DPWM Control Register 1 (DPWMCTRL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESET_EN	R/W	0	Counter Preset Enable 0 = Counter reset to 0 upon detection of sync (Default) 1 = Counter preset to Preset Count Value upon detection of sync
30	SYNC_FET_EN	R/W	0	SyncFET Mode Enabled 0 = SyncFET Mode Disabled (Default) 1 = SyncFET Mode Enabled (Default)
29	BURST_EN	R/W	0	Burst (Light Load) Mode Detection Enable 0 = Burst Mode (Light Load) Detection disabled (Default) 1 = Burst Mode (Light Load) Detection enabled
28	CLA_DUTY_ADJ_EN	R/W	0	Enables CLA Duty Adjust from Current/Flux Balancing 0 = CLA Duty Adjust not enabled (Default) 1 = CLA Duty Adjust enabled
27-24	SYNC_OUT_DIV_SEL	R/W	0000	Sets the divider for generating the Sync Out pulse. 0000 = Sync Out generated on every switching cycle (Default) 0001 = Sync Out generated once every 2 switching cycles 0010 = Sync Out generated once every 3 switching cycles ……. 1111 = Sync Out generated once every 16 switching cycles

Table 4-115. DPWM Control Register 1 (DPWMCTRL1) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-21	CLA_SCALE	R/W	000	Scaling for CLA Input Data 000 = CLA Value (Default) 001 = CLA Value multiplied by 2 010 = CLA Value divided by 2 011 = CLA Value multiplied by 4 100 = CLA Value divided by 4 101 = CLA Value multiplied by 8 110 = CLA Value divided by 8 111 = CLA Value
20	EXT_SYNC_EN	R/W	0	Slave DPWM to external sync 0 = DPWM not synchronized to external sync (Default) 1 = Slave DPWM to external sync
19	CBC_BSIDE _ACTIVE_EN	R/W	0	Sets if CBC responds to Fault CBC when PWM-B is active, only available in Multi and Reson modes 0 = Response to Fault CBC when PWM-A active (Default) 1 = Response to Fault CBC when PWM-A or PWM-B active
18	AUTO_MODE _SEL	R/W	0	Auto Switching Mode Select 0 = Auto Switching Mode disabled (Default) 1 = Auto Switching Mode enabled
17	RESERVED	R	0	
16	EVENT_UP_SEL	R/W	01	Update End Period Mode 0 = Events updated anytime 1 = Events updated at End of Period (Default)
15	CHECK _OVERRIDE	R/W	0	PWM Check Override 0 = DPWM checks mathematical settings within module, correct placement of Event settings/period settings. Invalid configurations are not allowed. 1 = Overrides checking for invalid configurations and turns off PWM mathematical checking functions (Default)
14	GLOBAL_PERIOD _ENGLOBAL _PERIOD_EN	R/W	0	0 = Event calculations use DPWM Period register (Default) 1 = Event calculations use Global Period register
13	PWM_B_OE	R/W	0	Direction for PWM B pin 0 = PWM B configured as output (Default) 1 = PWM B configured as input
12	PWM_A_OE	R/W	0	Direction for PWM A pin 0 = PWM A configured as output (Default) 1 = PWM A configured as input
11	GPIO_B_VAL	R/W	0	Sets value of PWM B output in GPIO mode 0 = PWM B driven low in GPIO mode (Default) 1 = PWM B driven high in GPIO mode
10	GPIO_B_EN	R/W	0	Enables GPIO mode for PWM B output 0 = PWM B in DPWM mode (Default) 1 = PWM B in GPIO mode
9	GPIO_A_VAL	R/W	0	Sets value of PWM A output in GPIO mode 0 = PWM A driven low in GPIO mode (Default) 1 = PWM A driven high in GPIO mode
8	GPIO_A_EN	R/W	0	Enables GPIO mode for PWM A output 0 = PWM A in DPWM mode (Default) 1 = PWM A in GPIO mode
7	PWM_HR_MULTI _OUT_EN	R/W	0	Control bit for Hi-Res Block 0 = Disabled (Default) 1 = Enabled

Table 4-115. DPWM Control Register 1 (DPWMCTRL1) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SFRAME_EN	R/W	0	PWM Single Step Frame Mode Enable 0 = Disable Single Frame Mode (Default) 1 = Enable Single Step Frame Mode. One EADC sample is requested, CLA then Filters, then one PWM duty cycle performed, then wait on Single Frame Trigger toggle before advancing to next frame.
5	PWM_B_PROT_DIS	R/W	0	PWM B Asynchronous Protection Disable 0 = Allows asynchronous protection to turn off PWM B Output (Default) 1 = Disables asynchronous protection from turning off PWM B Output
4	PWM_A_PROT_DIS	R/W	0	PWM A Asynchronous Protection Disable 0 = Allows asynchronous protection to turn off PWM A Output (Default) 1 = Disables asynchronous protection from turning off PWM A Output
3-2	HIRES_SCALE	R/W	00	Determines resolution of high resolution steps 00 = Resolution of 16 phases. Full resolution enabled. Resolution step = PCLK/16 (Default) 11 = Resolution of 2 phases. Resolution step = PCLK/2 10 = Resolution of 4 phases. Resolution step = PCLK/4 01 = Resolution of 8 phases. Resolution step = PCLK/8 00 = Resolution of 16 phases. Full Resolution enabled. Resolution step = PCLK/16
1	ALL_PHASE_CLK_ENA	R/W	1	High Speed Oscillator Phase Enable 0 = Enables only required phases of clock when needed 1 = Enables all phases of high resolution clock from oscillator (Default)
0	HIRES_DIS	R/W	0	PWM High Resolution Disable 0 = Enable High Resolution logic (Default) 1 = Disable High Resolution logic

4.8.3 DPWM Control Register 2 (DPWMCTRL2)

Address 00150008 – DPWM 3 Control Register 2

Address 00170008 – DPWM 2 Control Register 2

Address 001A0008 – DPWM 1 Control Register 2

Address 001D0008 – DPWM 0 Control Register 2

Figure 4-116. DPWM Control Register 2 (DPWMCTRL2)

19	18	17	16
DTC_MODE		DTC_EN	BLANK_PCM_EN
R/W-00		R/W-0	R/W-0

15	14	13	12	11	10	9	8
SYNC_IN_DIV_RATIO				Reserved		FILTER_DUTY_SEL	
R/W-0000				R-0		R/W-00	

7	6	5	4	3	2	1	0
IDE_DUTY_B_EN	Reserved	SAMPLE_TRIG1_OVERSAMPLE		SAMPLE_TRIG1_MODE		SAMPLE_TRIG_2_EN	SAMPLE_TRIG_1_EN
R/W-0	R-0	R/W-00		R/W-00		R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-116. DPWM Control Register 2 (DPWMCTRL2) Register Field Descriptions

Bit	Field	Type	Reset	Description
19-18	DTC_MODE	R/W	00	DTC Mode Select 00 = Only DTC phase adjust A utilized in edge adjustments (Default) 01 = Only DTC phase adjust B utilized in edge adjustments 10 = Both DTC phase adjust A and B utilized in edge adjustments 11 = Reserved
17	DTC_EN	R/W	0	Enables Dead Time Compensation Mode 0 = Disabled (Default) 1 = Enabled
16	BLANK_PCM_EN	R/W	0	Comparator Blanking Window B Enable for PCM 0 = Comparator Blanking A Window Disabled (Default) 1 = Comparator Blanking A Window for PWM-B Enabled
15-12	SYNC_IN_DIV_RATIO	R/W	0000	Sets the number of syncs to be masked before a resync
11-10	Reserved	R	0	
9-8	FILTER_DUTY_SEL	R/W	00	Sets which register is sent to the Resonant Duty input of the Filter. Settings of 0 and 1 enable the 16 bit signed value of the Resonant Duty register to be added to the Filter Period value for period adjustment in resonant mode. 0 = PWM Period Register (Default) 1 = Event 2 2 = DPWM Resonant Duty Register (Bits 13:0)
7	IDE_DUTY_B_EN	R/W	0	IDE Duty Cycle Side B Enable 0 = Disabled (Default) 1 = Enabled
6	Reserved	R	0	

Table 4-116. DPWM Control Register 2 (DPWMCTRL2) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	SAMPLE_TRIG1_OVERSAMPLE	R/W	00	Oversample Select for Sample Trigger 1 00 = Trigger an EADC Sample at PWM Sample Trig Register value (Default) 01 = Trigger EADC samples at (1* DPWMSAMPTRIG1) and at ((1/2)*DPWMSAMPTRIG1) 10 = Trigger EADC samples at (1* DPWMSAMPTRIG1) , ((3/4)*DPWMSAMPTRIG1), ((1/2)*DPWMSAMPTRIG1) and at ((1/4)*DPWMSAMPTRIG1) 11 = Trigger EADC samples at (1* DPWMSAMPTRIG1) , ((7/8)*DPWMSAMPTRIG1), ((3/4)*DPWMSAMPTRIG1), ((5/8)*DPWMSAMPTRIG1) , ((1/2)* DPWMSAMPTRIG1) , ((3/8)*DPWMSAMPTRIG1), ((1/4)*DPWMSAMPTRIG1) and at ((1/8)*DPWMSAMPTRIG1)
3-2	SAMPLE_TRIG1_MODE	R/W	00	Mode select for Sample Trigger 1 00 = Trigger value is set using PWM Sample Trig Register value (Default) 01 = Trigger value is adaptive midpoint (EV1+CLA_DUTY/2 + Adaptive Offset) and uses current CLA value at update event 10 = Trigger value is adaptive midpoint (EV1+CLA_DUTY + Adaptive Offset) and uses current CLA value at update event 11 = Trigger value is adaptive based on previous CBC location + Adaptive Offset
1	SAMPLE_TRIG_2_EN	R/W	0	Sample Trigger 2 Enable 0 = Disable Sample Trigger 2 (Default) 1 = Enable Sample Trigger 2
0	SAMPLE_TRIG_1_EN	R/W	1	Sample Trigger 1 Enable 0 = Disable Sample Trigger 1 1 = Enable Sample Trigger 1 (Default)

4.8.4 DPWM Period Register (DPWMPRD)

Address 0015000C – DPWM 3 Period Register

Address 0017000C – DPWM 2 Period Register

Address 001A000C – DPWM 1 Period Register

Address 001D000C – DPWM 0 Period Register

Figure 4-117. DPWM Period Register (DPWMPRD)

17	4	3	0
PRD		Reserved	
R/W-00 0000 0111 1101		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-117. DPWM Period Register (DPWMPRD) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	PRD	R/W	00 0000 0111 1101	PWM Period. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0	

4.8.5 DPWM Event 1 Register (DPWMEV1)

Address 00150010 – DPWM 3 Event 1 Register

Address 00170010 – DPWM 2 Event 1 Register

Address 001A0010 – DPWM 1 Event 1 Register

Address 001D0010 – DPWM 0 Event 1 Register

Figure 4-118. DPWM Event 1 Register (DPWMEV1)

17	4	3	0
EVENT1		Reserved	
R/W-00 0000 0001 0100		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-118. DPWM Event 1 Register (DPWMEV1) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	EVENT1	R/W	00 0000 0001 0100	Configures the location of Event 1. Low resolution register, last 4 bits are unused.
3-0	Reserved	R	0	

4.8.6 DPWM Event 2 Register (DPWMEV2)

Address 00150014 – DPWM 3 Event 2 Register

Address 00170014 – DPWM 2 Event 2 Register

Address 001A0014 – DPWM 1 Event 2 Register

Address 001D0014 – DPWM 0 Event 2 Register

Figure 4-119. DPWM Event 2 Register (DPWMEV2)

17		0
EVENT2		
R/W-0 0000 0011 0000 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-119. DPWM Event 2 Register (DPWMEV2) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-0	EVENT2	R/W	0 0000 0011 0000 0000	Configures the location of Event 2. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0 (dependent on Bits 3:2 of DPWM Control Register 2).

4.8.7 DPWM Event 3 Register (DPWMEV3)

Address 00150018 – Loop 4 DPWM Event 3 Register

Address 00170018 – Loop 3 DPWM Event 3 Register

Address 001A0018 – Loop 2 DPWM Event 3 Register

Address 001D0018 – Loop 1 DPWM Event 3 Register

Figure 4-120. DPWM Event 3 Register (DPWMEV3)

17		0
EVENT3		
R/W-00 0000 0011 1110 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-120. DPWM Event 3 Register (DPWMEV3) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-0	EVENT3	R/W	00 0000 0011 1110 0000	Configures the location of Event 3. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0.

4.8.8 DPWM Event 4 Register (DPWMEV4)

Address 0015001C – Loop 4 DPWM Event 4 Register

Address 0017001C – Loop 3 DPWM Event 4 Register

Address 001A001C – Loop 2 DPWM Event 4 Register

Address 001D001C – Loop 1 DPWM Event 4 Register

Figure 4-121. DPWM Event 4 Register (DPWMEV4)

17		0
EVENT4		
R/W-00 0000 0111 0000 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-121. DPWM Event 4 Register (DPWMEV4) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-0	EVENT4	R/W	00 0000 0111 0000 0000	Configures the location of Event 4. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0.

4.8.9 DPWM Sample Trigger 1 Register (DPWMSAMPTRIG1)

Address 00150020 – DPWM 3 Sample Trigger 1 Register

Address 00170020 – DPWM 2 Sample Trigger 1 Register

Address 001A0020 – DPWM 1 Sample Trigger 1 Register

Address 001D0020 – DPWM 0 Sample Trigger 1 Register

Figure 4-122. DPWM Sample Trigger 1 Register (DPWMSAMPTRIG1)

17	6	5	0
SAMPLE_TRIGGER		Reserved	
R/W-0000 0000 0100		R-00 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-122. DPWM Sample Trigger 1 Register (DPWMSAMPTRIG1) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-6	SAMPLE_ TRIGGER	R/W	0000 0000 0100	Configures the location of the sample trigger within a PWM period. Value equals the number of PCLK clock periods. Enables start of conversion for EADC. Low resolution register, last 6 bits are read-only.
5-0	Reserved	R	00 0000	

4.8.10 DPWM Sample Trigger 2 Register (DPWMSAMPTRIG2)

Address 00150024 – DPWM 3 Sample Trigger 2 Register

Address 00170024 – DPWM 2 Sample Trigger 2 Register

Address 001A0024 – DPWM 1 Sample Trigger 2 Register

Address 001D0024 – DPWM 0 Sample Trigger 2 Register

Figure 4-123. DPWM Sample Trigger 2 Register (DPWMSAMPTRIG2)

17	6	5	0
SAMPLE_TRIGGER		Reserved	
R/W-0000 0000 0100		R-00 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-123. DPWM Sample Trigger 2 Register (DPWMSAMPTRIG2) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-6	SAMPLE_ TRIGGER	R/W	0000 0000 0100	Configures the location of the sample trigger within a PWM period. Value equals the number of PCLK clock periods. Enables start of conversion for EADC. Low resolution register, last 6 bits are read-only.
5-0	Reserved	R	00 0000	

4.8.11 DPWM Phase Trigger Register (DPWMPHASETRIG)

Address 00150028 – DPWM 3 Phase Trigger Register

Address 00170028 – DPWM 2 Phase Trigger Register

Address 001A0028 – DPWM 1 Phase Trigger Register

Address 001D0028 – DPWM 0 Phase Trigger Register

Figure 4-124. DPWM Phase Trigger Register (DPWMPHASETRIG)

17	4	3	0
PHASE_TRIGGER		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-124. DPWM Phase Trigger Register (DPWMPHASETRIG) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	PHASE_TRIGGER	R/W	00 0000 0000 0000	Configures the phase trigger delay from start of DPWM period to sync ouput to slave DPWM. Value equals the number of PCLK clock periods. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.12 DPWM Cycle Adjust A Register (DPWMCYCADJA)

Address 0015002C – DPWM 3 Cycle Adjust A Register

Address 0017002C – DPWM 2 Cycle Adjust A Register

Address 001A002C – DPWM 1 Cycle Adjust A Register

Address 001D002C – DPWM 0 Cycle Adjust A Register

Figure 4-125. DPWM Cycle Adjust A Register (DPWMCYCADJA)

15	0
CYCLE_ADJUST_A	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-125. DPWM Cycle Adjust A Register (DPWMCYCADJA) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CYCLE_ADJUST_A	R/W	0000 0000 0000 0000	Adjusts PWM A output signal. 16-bit signed number allows output signal to be delayed or sped up.

4.8.13 DPWM Cycle Adjust B Register (DPWMCYCADJB)

Address 00150030 – DPWM 3 Cycle Adjust B Register

Address 00170030 – DPWM 2 Cycle Adjust B Register

Address 001A0030 – DPWM 1 Cycle Adjust B Register

Address 001D0030 – DPWM 0 Cycle Adjust B Register

Figure 4-126. DPWM Cycle Adjust B Register (DPWMCYCADJB)

15	0
CYCLE_ADJUST_B	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-126. DPWM Cycle Adjust B Register (DPWMCYCADJB) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CYCLE_ADJUST_B	R/W	0000 0000 0000 0000	Adjusts the PWM B output signal. 16-bit signed number allows output signal to be delayed or sped up.

4.8.14 DPWM Resonant Duty Register (DPWMRESDUTY)

Address 00150034 – DPWM 3 Resonant Duty Register

Address 00170034 – DPWM 2 Resonant Duty Register

Address 001A0034 – DPWM 1 Resonant Duty Register

Address 001D0034 – DPWM 0 Resonant Duty Register

Figure 4-127. DPWM Resonant Duty Register (DPWMRESDUTY)

15	0
RESONANT_DUTY	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-127. DPWM Resonant Duty Register (DPWMRESDUTY) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESONANT _DUTY	R/W	0000 0000 0000 0000	Controls the DPWM duty. 16-bit signed number is used as a Filter Output Multiplier in Resonant Mode.

4.8.15 DPWM Fault Control Register (DPWMFLTCTRL)

Address 00150038 – DPWM 3 Fault Control Register

Address 00170038 – DPWM 2 Fault Control Register

Address 001A0038 – DPWM 1 Fault Control Register

Address 001D0038 – DPWM 0 Fault Control Register

Figure 4-128. DPWM Fault Control Register (DPWMFLTCTRL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FLT_RESTART	ALL_FAULT_EN	CBC_FAULT_EN	CBC_FAULT_MODE	CBC_MAX_COUNT							AB_MAX_COUNT				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0							R/W-0				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AB_MAX_COUNT		B_MAX_COUNT							A_MAX_COUNT						
R/W-0		R/W-0							R/W-0						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-128. DPWM Fault Control Register (DPWMFLTCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FLT_RESTART	R/W	0	Enables DPWM after Fault. 1->0 = Enables DPWM on Falling Edge Transition of Bit. Does nothing otherwise.
30	ALL_FAULT_EN	R/W	0	DPWM Fault Module enable 0 = All DPWM Fault Modules disabled (Default) 1 = All DPWM Fault Modules enabled
29	CBC_FAULT_EN	R/W	0	CBC Fault Module enable 0 = All CBC Fault Modules disabled (Default) 1 = All CBC Fault Modules enabled
28	CBC_FAULT_MODE	R/W	0	CBC Fault Mode 0 = CBC Fault input set to raw CBC fault 1 = CBC Fault input set to output of CBC module
27-21	CBC_MAX_COUNT	R/W	0	Cycle-by-Cycle Fault Count, sets the number of received sequential faults on Cycle-by-Cycle Fault input before asserting the fault
20-14	AB_MAX_COUNT	R/W	0	Fault AB Count, sets the number of received sequential faults on Fault AB input before asserting the fault
13-7	B_MAX_COUNT	R/W	0	Fault B Count, sets the number of received sequential faults on Fault B input before asserting the fault
6-0	A_MAX_COUNT	R/W	0	Fault A Count, sets the number of received sequential faults on Fault A input before asserting the fault

4.8.16 DPWM Overflow Register (DPWMOVERFLOW)

Address 0015003C – DPWM 3 Overflow Register

Address 0017003C – DPWM 2 Overflow Register

Address 001A003C – DPWM 1 Overflow Register

Address 001D003C – DPWM 0 Overflow Register

Figure 4-129. DPWM Overflow Register (DPWMOVERFLOW)

7	6	5	4	3 ... 0
PWM_B_CHECK	PWM_A_CHECK	GPIO_B_IN	GPIO_A_IN	OVERFLOW
R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-129. DPWM Overflow Register (DPWMOVERFLOW) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM_B_CHECK	R	0	Value of PWM B internal check 0 = Passed checks 1 = Failed checks (override required to enable output)
6	PWM_A_CHECK	R	0	Value of PWM B input 0 = Passed check 1 = Failed check (override required to enable output)
5	GPIO_B_IN	R	0	Value of PWM B input 0 = Low signal on PWM B 1 = High signal on PWM B
4	GPIO_A_IN	R	0	Value of PWM A input 0 = Low signal on PWM A 1 = High value on PWM A
3-0	OVERFLOW	R	0	PWM Event 4 Overflow Status 0 = CLA Event 4 has not overflowed 1 = Overflow condition found on CLA Event 4 OVERFLOW[2] – CLA Event 4 Overflow Status 0 = PWM Event 4 has not overflowed 1 = Overflow condition found on PWM Event 4 OVERFLOW[1] – CLA Event 3 Overflow Status 0 = CLA Event 3 has not overflowed 1 = Overflow condition found on CLA Event 3 OVERFLOW[0] – CLA Event 2 Overflow Status 0 = CLA Event 2 has not overflowed 1 = Overflow condition found on CLA Event 2

4.8.17 DPWM Interrupt Register (DPWMINT)

Address 00150040 – DPWM 3 Interrupt Register

Address 00170040 – DPWM 2 Interrupt Register

Address 001A0040 – DPWM 1 Interrupt Register

Address 001D0040 – DPWM 0 Interrupt Register

Figure 4-130. DPWM Interrupt Register (DPWMINT)

23	22	21	20	19	18	17	16
DTC_DISABLE	MODE_SWITCH	FLT_A	FLT_B	FLT_AB	FLT_CBC	PRD	INT
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15			12	11	10	9	8
Reserved				MODE_SWITCH_FLAG_CLR	MODE_SWITCH_FLAG_EN	MODE_SWITCH_INT_EN	FLT_A_INT_EN
R/W-0000				R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3			0
FLT_B_INT_EN	FLT_AB_INT_EN	FLT_CBC_INT_EN	PRD_INT_EN	PRD_INT_SCALE			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1111			

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-130. DPWM Interrupt Register (DPWMINT) Register Field Descriptions

Bit	Field	Type	Reset	Description
23	DTC_DISABLE	R	0	DTC Disabled Flag 0 = Flag is not asserted 1 = Flag is set
22	MODE_SWITCH	R	0	Mode Switching Flag 0 = Flag is not asserted 1 = Flag is set
21	FLT_A	R	0	Fault A Flag 0 = Flag is not asserted 1 = Flag is set
20	FLT_B	R	0	Fault B Flag 0 = Flag is not asserted 1 = Flag is set
19	FLT_AB	R	0	Fault AB Flag 0 = Flag is not asserted 1 = Flag is set
18	FLT_CBC	R	0	Fault Cycle-by-Cycle Flag 0 = Flag is not asserted 1 = Flag is set
17	PRD	R	0	PWM Period Interrupt Flag 0 = PWM Period Interrupt Flag is not asserted 1 = PWM Period Interrupt Flag is set
16	INT	R	0	Interrupt Out 0 = INT is not asserted 1 = INT is set
15-12	Reserved	R	0000	
11	MODE_SWITCH_FLAG_CLR	R/W	0	Mode Switching Flag Clear 0 = (Default) 1 = Rising edge. 0-1 clears MODE_SWITCH bit.

Table 4-130. DPWM Interrupt Register (DPWMINT) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MODE_SWITCH_FLAG_EN	R/W	0	Mode Switching Flag Enable 0 = Disables generation of flag for Mode Switching (Default) 1 = Enables generation of flag for Mode Switching
9	MODE_SWITCH_INT_EN	R/W	0	Mode Switching Interrupt Enable 0 = Interrupt is not enabled (Default) 1 = Interrupt is enabled
8	FLT_A_INT_EN	R/W	0	Fault A Flag Interrupt Enable 0 = Interrupt is not enabled (Default) 1 = Interrupt is enabled
7	FLT_B_INT_EN	R/W	0	Fault B Flag Interrupt Enable 0 = Interrupt is not enabled (Default) 1 = Interrupt is enabled
6	FLT_AB_INT_EN	R/W	0	Fault AB Flag Interrupt Enable 0 = Interrupt is not enabled (Default) 1 = Interrupt is enabled
5	FLT_CBC_INT_EN	R/W	0	Fault Cycle-by-Cycle Flag Interrupt Enable 0 = Interrupt is not enabled (Default) 1 = Interrupt is enabled
4	PRD_INT_EN	R/W	0	PWM Period Interrupt Enable 0 = Disables generation of periodic PWM interrupt (Default) 1 = Enables generation of periodic PWM interrupt
3-0	PRD_INT_SCALE	R/W	1111	This value scales the period interrupt signal from an interrupt every switching cycle to 256 switching cycles 0000 = Period Interrupt generated every switching cycle (Default) 0001 = Period Interrupt generated once every 2 switching cycles 0010 = Period Interrupt generated once every 4 switching cycles 0011 = Period Interrupt generated once every 6 switching cycles 0100 = Period Interrupt generated once every 8 switching cycles 0101 = Period Interrupt generated once every 16 switching cycles 0110 = Period Interrupt generated once every 32 switching cycles 0111 = Period Interrupt generated once every 48 switching cycles 1000 = Period Interrupt generated once every 64 switching cycles 1001 = Period Interrupt generated once every 80 switching cycles 1010 = Period Interrupt generated once every 96 switching cycles 1011 = Period Interrupt generated once every 128 switching cycles 1100 = Period Interrupt generated once every 160 switching cycles 1101 = Period Interrupt generated once every 192 switching cycles 1110 = Period Interrupt generated once every 224 switching cycles 1111 = Period Interrupt generated once every 256 switching cycles

4.8.18 DPWM Counter Preset Register (DPWMCNTPRE)

Address 00150044 – DPWM 3 Counter Preset Register

Address 00170044 – DPWM 2 Counter Preset Register

Address 001A0044 – DPWM 1 Counter Preset Register

Address 001D0044 – DPWM 0 Counter Preset Register

Figure 4-131. DPWM Counter Preset Register (DPWMCNTPRE)

17	4	3	0
PRESET		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-131. DPWM Counter Preset Register (DPWMCNTPRE) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	PRESET	R/W	00 0000 0000 0000	Counter preset value, counter reset to this value upon detection of sync when PRESET_EN bit in DPWMCTRL2 is enabled. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.19 DPWM Blanking A Begin Register (DPWMBLKABEG)

Address 00150048 – DPWM 3 Blanking A Begin Register

Address 00170048 – DPWM 2 Blanking A Begin Register

Address 001A0048 – DPWM 1 Blanking A Begin Register

Address 001D0048 – DPWM 0 Blanking A Begin Register

Figure 4-132. DPWM Blanking A Begin Register (DPWMBLKABEG)

17	4	3	0
BLANK_A_BEGIN		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-132. DPWM Blanking A Begin Register (DPWMBLKABEG) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	BLANK_A_BEGIN	R/W	00 0000 0000 0000	Configures start of Comparator Blanking Window A. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.20 DPWM Blanking A End Register (DPWMBLKAEND)

Address 0015004C – DPWM 3 Blanking A End Register

Address 0017004C – DPWM 2 Blanking A End Register

Address 001A004C – DPWM 1 Blanking A End Register

Address 001D004C – DPWM 0 Blanking A End Register

Figure 4-133. DPWM Blanking A End Register (DPWMBLKAEND)

17	4	3	0
BLANK_A_END		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-133. DPWM Blanking A End Register (DPWMBLKAEND) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	BLANK_A_END	R/W	00 0000 0000 0000	Configures end of Comparator Blanking Window A. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.21 DPWM Blanking B Begin Register (DPWMBLKBBEG)

Address 00150050 – DPWM 3 Blanking B Begin Register

Address 00170050 – DPWM 2 Blanking B Begin Register

Address 001A0050 – DPWM 1 Blanking B Begin Register

Address 001D0050 – DPWM 0 Blanking B Begin Register

Figure 4-134. DPWM Blanking B Begin Register (DPWMBLKBBEG)

17	4	3	0
BLANK_B_BEGIN		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-134. DPWM Blanking B Begin Register (DPWMBLKBBEG) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	BLANK_B_BEGIN	R/W	00 0000 0000 0000	Configures start of Comparator Blanking Window B. Low resolution register, last 4 bits are read-only. Can also define the start of the DPWMC pulse.
3-0	Reserved	R	0000	

4.8.22 DPWM Blanking B End Register (DPWMBLKBEND)

Address 00150054 – DPWM 3 Blanking B End Register

Address 00170054 – DPWM 2 Blanking B End Register

Address 001A0054 – DPWM 1 Blanking B End Register

Address 001D0054 – DPWM 0 Blanking B End Register

Figure 4-135. DPWM Blanking B End Register (DPWMBLKBEND)

17	4	3	0
BLANK_B_END		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-135. DPWM Blanking B End Register (DPWMBLKBEND) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	BLANK_B_END	R/W	00 0000 0000 0000	Configures end of Comparator Blanking Window B. Low resolution register, last 4 bits are read-only. Can also define the end of the DPWMC pulse.
3-0	Reserved	R	0000	

4.8.23 DPWM Minimum Duty Cycle High Register (DPWMMINDUTYHI)

Address 00150058 – DPWM 3 Minimum Duty Cycle High Register

Address 00170058 – DPWM 2 Minimum Duty Cycle High Register

Address 001A0058 – DPWM 1 Minimum Duty Cycle High Register

Address 001D0058 – DPWM 0 Minimum Duty Cycle High Register

Figure 4-136. DPWM Minimum Duty Cycle High Register (DPWMMINDUTYHI)

17	4	3	0
MIN_DUTY_HIGH		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-136. DPWM Minimum Duty Cycle High Register (DPWMMINDUTYHI) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	MIN_DUTY_HIGH	R/W	00 0000 0000 0000	Configures upper threshold for minimum duty cycle logic. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.24 DPWM Minimum Duty Cycle Low Register (DPWMMINDUTYLO)

Address 0015005C – DPWM 3 Minimum Duty Cycle Low Register

Address 0017005C – DPWM 2 Minimum Duty Cycle Low Register

Address 001A005C – DPWM 1 Minimum Duty Cycle Low Register

Address 001D005C – DPWM 0 Minimum Duty Cycle Low Register

Figure 4-137. DPWM Minimum Duty Cycle Low Register (DPWMMINDUTYLO)

17	4	3	0
MIN_DUTY_LOW		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-137. DPWM Minimum Duty Cycle Low Register (DPWMMINDUTYLO) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	MIN_DUTY_LOW	R/W	00 0000 0000 0000	Configures lower threshold for minimum duty cycle logic. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.25 DPWM Adaptive Sample Register (DPWMADAPTIVE)

Address 00150060 – DPWM 3 Adaptive Sample Register

Address 00170060 – DPWM 2 Adaptive Sample Register

Address 001A0060 – DPWM 1 Adaptive Sample Register

Address 001D0060 – DPWM 0 Adaptive Sample Register

Figure 4-138. DPWM Adaptive Sample Register (DPWMADAPTIVE)

11	0
ADAPT_SAMP	
R/W-0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-138. DPWM Adaptive Sample Register (DPWMADAPTIVE) Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	ADAPT_SAMP	R/W	0000 0000 0000	Configures Adaptive Sample Adjust

4.8.26 DPWM Fault Status (DPWMFLTSTAT)

Address 00150064 – DPWM 3 Fault Input Status Register

Address 00170064 – DPWM 2 Fault Input Status Register

Address 001A0064 – DPWM 1 Fault Input Status Register

Address 001D0064 – DPWM 0 Fault Input Status Register

Figure 4-139. DPWM Fault Status (DPWMFLTSTAT)

5	4	3	2	1	0
BURST	IDE_DETECT	FLT_A	FLT_B	FLT_AB	FLT_CBC
R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-139. DPWM Fault Status (DPWMFLTSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
5	BURST	R	0	Burst Mode Detection Status 0 = Burst Mode Detection is not asserted 1 = Burst Mode Detection is set
4	IDE_DETECT	R	0	IDE Detection Status (from Analog Comparators) 0 = IDE Detection is not asserted 1 = IDE Detection is set
3	FLT_A	R	0	Fault A Detection Status 0 = Fault A Detection is not asserted 1 = Fault A Detection is set
2	FLT_B	R	0	Fault B Detection Status 0 = Fault B Detection is not asserted 1 = Fault B Detection is set
1	FLT_AB	R	0	Fault AB Detection Statu 0 = Fault AB Detection is not asserted 1 = Fault AB Detection is set
0	FLT_CBC	R	0	Current Limit Detection Status 0 = Current Limit Detection is not asserted 1 = Current Limit Detection is set

4.8.27 DPWM Auto Switch High Upper Thresh Register (DPWMAUTOSWHIUPTHRESH)

Address 00150068 – DPWM 3 Auto Switch High Upper Thresh Register

Address 00170068 – DPWM 2 Auto Switch High Upper Thresh Register

Address 001A0068 – DPWM 1 Auto Switch High Upper Thresh Register

Address 001D0068 – DPWM 0 Auto Switch High Upper Thresh Register

Figure 4-140. DPWM Auto Switch High Upper Thresh Register (DPWMAUTOSWHIUPTHRESH)

17	4	3	0
AUTO_SWITCH_HIGH_UPPER		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-140. DPWM Auto Switch High Upper Thresh Register (DPWMAUTOSWHIUPTHRESH) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	AUTO_SWITCH _HIGH_UPPER	R/W	00 0000 0000 0000	Configures upper threshold for Auto Switch Mode High operation. Mode switching does not occur between Auto Switch High Upper and Auto Switch High Lower thresholds. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.28 DPWM Auto Switch High Lower Thresh Register (DPWMAUTOSWHILOWTHRESH)

Address 0015006C – DPWM 3 Auto Switch High Lower Thresh Register

Address 0017006C – DPWM 2 Auto Switch High Lower Thresh Register

Address 001A006C – DPWM 1 Auto Switch High Lower Thresh Register

Address 001D006C – DPWM 0 Auto Switch High Lower Thresh Register

Figure 4-141. DPWM Auto Switch High Lower Thresh Register (DPWMAUTOSWHILOWTHRESH)

17	4	3	0
AUTO_SWITCH_HIGH_LOWER		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-141. DPWM Auto Switch High Lower Thresh Register (DPWMAUTOSWHILOWTHRESH) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	AUTO_SWITCH _HIGH_UPPER	R/W	00 0000 0000 0000	Configures lower threshold for Auto Switch Mode High operation. Mode switching does not occur between Auto Switch High Upper and Auto Switch High Lower thresholds. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.29 DPWM Auto Switch Low Upper Thresh Register (DPWMAUTOSWLOUPTHRESH)

Address 00150070 – DPWM 3 Auto Switch Low Upper Thresh Register

Address 00170070 – DPWM 2 Auto Switch Low Upper Thresh Register

Address 001A0070 – DPWM 1 Auto Switch Low Upper Thresh Register

Address 001D0070 – DPWM 0 Auto Switch Low Upper Thresh Register

Figure 4-142. DPWM Auto Switch Low Upper Thresh Register (DPWMAUTOSWLOUPTHRESH)

17	4	3	0
AUTO_SWITCH_LOW_UPPER		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-142. DPWM Auto Switch Low Upper Thresh Register (DPWMAUTOSWLOUPTHRESH) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	AUTO_SWITCH _LOW_UPPER	R/W	00 0000 0000 0000	Configures upper threshold for Auto Switch Mode Low operation. Mode switching does not occur between Auto Switch Low Upper and Auto Switch Low Lower thresholds. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.30 DPWM Auto Switch Low Lower Thresh Register (DPWMAUTOSWLOLOWTHRESH)

Address 00150074 – DPWM 3 Auto Switch Low Lower Thresh Register

Address 00170074 – DPWM 2 Auto Switch Low Lower Thresh Register

Address 001A0074 – DPWM 1 Auto Switch Low Lower Thresh Register

Address 001D0074 – DPWM 0 Auto Switch Low Lower Thresh Register

Figure 4-143. DPWM Auto Switch Low Lower Thresh Register (DPWMAUTOSWLOLOWTHRESH)

17	4	3	0
AUTO_SWITCH_LOW_LOWER		Reserved	
R/W-00 0000 0000 0000		R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-143. DPWM Auto Switch Low Lower Thresh Register (DPWMAUTOSWLOLOWTHRESH) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-4	AUTO_SWITCH _LOW_LOWER	R/W	00 0000 0000 0000	Configures lower threshold for Auto Switch Mode Low operation. Mode switching does not occur between Auto Switch Low Upper and Auto Switch Low Lower thresholds. Low resolution register, last 4 bits are read-only.
3-0	Reserved	R	0000	

4.8.31 DPWM Auto Config Max Register (DPWMAUTOMAX)

Address 00150078 – DPWM 3 Auto Config Max Register

Address 00170078 – DPWM 2 Auto Config Max Register

Address 001A0078 – DPWM 1 Auto Config Max Register

Address 001D0078 – DPWM 0 Auto Config Max Register

Figure 4-144. DPWM Auto Config Max Register (DPWMAUTOMAX)

31	30	29	28	27	26	25	24
PWM_B_INTRA_MUX				PWM_A_INTRA_MUX			
R/W-000				R/W-000			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CBC_PWM_C_EN	Reserved		CBC_PWM_AB_EN	CBC_ADV_CNT_EN	Reserved		
R/W-000	R-0		R/W-0	R/W-0	R-0		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			RESON_MODE_FIXED_DUTY_EN	Reserved			
R-0			R/W-0	R-0000 0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	PWM_MODE			Reserved		CLA_EN	Reserved
R-0000 0	R/W-00			R-00		R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-144. DPWM Auto Config Max Register (DPWMAUTOMAX) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PWM_B_INTRA_MUX	R/W	000	Interchanges DPWM signals post edge generation 0 = Pass-through (Default) 1 = Edge-gen output, this module 2 = PWM-C, this module 3 = Crossover, this module 4 = Pass-through below A 5 = Pass-through below B 6 = Pass-through below C 7 = Pass-through below level-2 C 8 = Pass-through below level-3 C
27-24	PWM_A_INTRA_MUX	R/W	000	Combines DPWM signals are prior to HR module 0 = Pass-through (Default) 1 = Edge-gen output, this module 2 = PWM-C, this module 3 = Crossover, this module 4 = Pass-through below A 5 = Pass-through below B 6 = Pass-through below C 7 = Pass-through below level-2 C 8 = Pass-through below level-3 C
23	CBC_PWM_C_EN	R/W	000	Sets if Fault CBC changes output waveform for PWM-C 0 = PWM-C unaffected by Fault CBC (Default) 1 = PWM-C affected by Fault CBC
22-21	Reserved	R	0	
20	CBC_PWM_AB_EN	R/W	0	Sets if Fault CBC changes output waveform for PWM-A and PWM-B 0 = PWM-A and PWM-B unaffected by Fault CBC (Default) 1 = PWM-A and PWM-B affected by Fault CBC

Table 4-144. DPWM Auto Config Max Register (DPWMAUTOMAX) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CBC_ADV_CNT _EN	R/W	0	Selects cycle-by-cycle of operation **Normal Mode** 0 = CBC disabled (Default) 1 = CBC enabled **Multi and Resonant Modes** 0 = PWM-A and PWM-B operate independently (Default) 1 = PWM-A and PWM-B pulse matching enabled
18-13	Reserved	R	0	
12	RESON_MODE _FIXED_DUTY _EN	R/W	0	Configures how duty cycle is controlled in Resonance Mode 0 = Resonant mode duty cycle set by Filter duty (Default) 1 = Resonant mode duty cycle set by Auto Switch High Register
11-7	Reserved	R	0000 0	
6-4	PWM_MODE	R/W	000	DPWM Mode 0 = Normal Mode (Default) 1 = Resonant Mode 2 = Multi-Output Mode 3 = Triangular Mode 4 = Leading Mode
3-2	Reserved	R	00	
1	CLA_EN	R/W	0	CLA Processing Enable 0 = Generate PWM waveforms from PWM Register values (Default) 1 = Enable CLA input
0	Reserved	R	0	

4.8.32 DPWM Auto Config Mid Register (DPWMAUTOMID)

Address 0015007C – DPWM 3 Auto Config Mid Register

Address 0017007C – DPWM 2 Auto Config Mid Register

Address 001A007C – DPWM 1 Auto Config Mid Register

Address 001D007C – DPWM 0 Auto Config Mid Register

Figure 4-145. DPWM Auto Config Mid Register (DPWMAUTOMID)

31	30	29	28	27	26	25	24
PWM_B_INTRA_MUX				PWM_A_INTRA_MUX			
R/W-000				R/W-000			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CBC_PWM_C_EN	Reserved		CBC_PWM_AB_EN	CBC_ADV_CNT_EN	Reserved		
R/W-0	R-0		R/W-0	R/W-0	R-0		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			RESON_MODE_FIXED_DUTY_EN	Reserved			
R-0			R/W-0	R-0000 0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	PWM_MODE			Reserved		CLA_EN	Reserved
R-0000 0	R/W-000			R-00		R/W-1	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-145. DPWM Auto Config Mid Register (DPWMAUTOMID) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PWM_B_INTRA_MUX	R/W	000	Interchanges DPWM signals post edge generation 0 = Pass-through (Default) 1 = Edge-gen output, this module 2 = PWM-C, this module 3 = Crossover, this module 4 = Pass-through below A 5 = Pass-through below B 6 = Pass-through below C 7 = Pass-through below level-2 C 8 = Pass-through below level-3 C
27-24	PWM_A_INTRA_MUX	R/W	000	Combines DPWM signals are prior to HR module 0 = Pass-through (Default) 1 = Edge-gen output, this module 2 = PWM-C, this module 3 = Crossover, this module 4 = Pass-through below A 5 = Pass-through below B 6 = Pass-through below C 7 = Pass-through below level-2 C 8 = Pass-through below level-3 C
23	CBC_PWM_C_EN	R/W	000	Sets if Fault CBC changes output waveform for PWM-C 0 = PWM-C unaffected by Fault CBC (Default) 1 = PWM-C affected by Fault CBC
22-21	Reserved	R	0	
20	CBC_PWM_AB_EN	R/W	0	Sets if Fault CBC changes output waveform for PWM-A and PWM-B 0 = PWM-A and PWM-B unaffected by Fault CBC (Default) 1 = PWM-A and PWM-B affected by Fault CBC

Table 4-145. DPWM Auto Config Mid Register (DPWMAUTOMID) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	CBC_ADV_CNT _EN	R/W	0	Selects cycle-by-cycle of operation **Normal Mode** 0 = CBC disabled (Default) 1 = CBC enabled **Multi and Resonant Modes** 0 = PWM-A and PWM-B operate independently (Default) 1 = PWM-A and PWM-B pulse matching enabled
18-13	Reserved	R	0	
12	RESON_MODE _FIXED_DUTY _EN	R/W	0	Configures how duty cycle is controlled in Resonance Mode 0 = Resonant mode duty cycle set by Filter duty (Default) 1 = Resonant mode duty cycle set by Auto Switch High Register
11-7	Reserved	R	0000 0	
6-4	PWM_MODE	R/W	000	DPWM Mode 0 = Normal Mode (Default) 1 = Resonant Mode 2 = Multi-Output Mode 3 = Triangular Mode 4 = Leading Mode
3-2	Reserved	R	00	
1	CLA_EN	R/W	1	CLA Processing Enable 0 = Generate PWM waveforms from PWM Register values 1 = Enable CLA input (Default)
0	Reserved	R	0	

4.8.33 DPWM Edge PWM Generation Control Register (DPWMEDGEGEN)

Address 00150080 – DPWM 3 Edge PWM Generation Control Register

Address 00170080 – DPWM 2 Edge PWM Generation Control Register

Address 001A0080 – DPWM 1 Edge PWM Generation Control Register

Address 001D0080 – DPWM 0 Edge PWM Generation Control Register

Figure 4-146. DPWM Edge PWM Generation Control Register (DPWMEDGEGEN)

16	15	14	13	12	11	10	9	8
EDGE_EN	Reserved	A_ON_EDGE			Reserved	A_OFF_EDGE		
R/W-0	R-0	R/W-000			R-0	R/W-001		
7	6	5	4	3	2	1	0	
Reserved	B_ON_EDGE			Reserved	B_OFF_EDGE			
R-0	R/W-010			R-0	R/W-011			

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-146. DPWM Edge PWM Generation Control Register (DPWMEDGEGEN) Register Field Descriptions

Bit	Field	Type	Reset	Description
16	EDGE_EN	R/W	0	Enables edge generate module. When combining dpwm's, all modules must have this bit enabled.
15	Reserved	R	0	
14-12	A_ON_EDGE	R/W	000	Select input edge to trigger A ON output edge 0 = Current DPWM posedge A 1 = Current DPWM negedge A 2 = Current DPWM posedge B 3 = Current DPWM negedge B 4 = Below (n+1) DPWM posedge A 5 = Below (n+1) DPWM negedge A 6 = Below (n+1) DPWM posedge B 7 = Below (n+1) DPWM negedge B
11	Reserved	R	0	
10-8	A_OFF_EDGE	R/W	001	Select input edge to trigger A OFF output edge 0 = Current DPWM posedge A 1 = Current DPWM negedge A 2 = Current DPWM posedge B 3 = Current DPWM negedge B 4 = Below (n+1) DPWM posedge A 5 = Below (n+1) DPWM negedge A 6 = Below (n+1) DPWM posedge B 7 = Below (n+1) DPWM negedge B
7	Reserved	R	0	
6-4	B_ON_EDGE	R/W	010	Select input edge to trigger B ON output edge 0 = Current DPWM posedge A = Current DPWM posedge A 1 = Current DPWM negedge A 2 = Current DPWM posedge B 3 = Current DPWM negedge B 4 = Below (n+1) DPWM posedge A 5 = Below (n+1) DPWM negedge A 6 = Below (n+1) DPWM posedge B 7 = Below (n+1) DPWM negedge B
3	Reserved	R	0	

Table 4-146. DPWM Edge PWM Generation Control Register (DPWMEDGEGEN) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	B_OFF_EDGE	R/W	011	Select input edge to trigger B OFF output edge 0 = Current DPWM posedge A 1 = Current DPWM negedge A 2 = Current DPWM posedge B 3 = Current DPWM negedge B 4 = Below (n+1) DPWM posedge A 5 = Below (n+1) DPWM negedge A 6 = Below (n+1) DPWM posedge B 7 = Below (n+1) DPWM negedge B

4.8.34 DPWM Filter Duty Read Register (DPWMFILTERDUTYREAD)

Address 00150084 – DPWM 3 Filter Duty Read Register

Address 00170084 – DPWM 2 Filter Duty Read Register

Address 001A0084 – DPWM 1 Filter Duty Read Register

Address 001D0084 – DPWM 0 Filter Duty Read Register

Figure 4-147. DPWM Filter Duty Read Register (DPWMFILTERDUTYREAD)

17	0
FILTER_DUTY	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-147. DPWM Filter Duty Read Register (DPWMFILTERDUTYREAD) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-0	FILTER_DUTY	R	0	Filter Duty value received by DPWM Module

4.8.35 DPWM CBC Location (DPWMCBCLOCATION)

Address 00150088 – DPWM 3 CBC Location Register

Address 00170088 – DPWM 2 CBC Location Register

Address 001A0088 – DPWM 1 CBC Location Register

Address 001D0088 – DPWM 0 CBC Location Register

Figure 4-148. DPWM CBC Location (DPWMCBCLOCATION)

13														0
CBC_LOCATION														
R-X														

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-148. DPWM CBC Location (DPWMCBCLOCATION) Register Field Descriptions

Bit	Field	Type	Reset	Description
13-0	CBC_LOCATION	R	X	Holds counter value of last CBC event.

4.9 Filter Registers Reference

Registers for Filter Modules 0-2 are identical in their bit definitions.

4.9.1 Filter Status Register (FILTERSTATUS)

Address 00160000 – Filter 2 Status Register

Address 00190000 – Filter 1 Status Register

Address 001C0000 – Filter 0 Status Register

Figure 4-149. Filter Status Register (FILTERSTATUS)

4	3	2	1	0
FILTER_BUSY	YN_LOW_CLAMP	YN_HIGH_CLAMP	KI_YN_LOW_CLAMP	KI_YN_HIGH_CLAMP
R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-149. Filter Status Register (FILTERSTATUS) Register Field Descriptions

Bit	Field	Type	Reset	Description
4	FILTER_BUSY	R	0	Filter Busy Indicator 0 = Filter is waiting for new data 1= Filter busy calculating
3	YN_LOW_CLAMP	R	0	PID Output Low Rail Indicator 0 = PID Output not equal to low rail 1 = PID Output equal to low rail
2	YN_HIGH_ CLAMP	R	0	PID Output High Rail Indicator 0 = PID Output not equal to high rail 1 = PID Output equal to high rail
1	KI_YN_LOW_ CLAMP	R	0	KI Feedback Low Rail Indicator 0 = KI Feedback not equal to low rail 1 = KI Feedback equal to low rail
0	KI_YN_HIGH_CLA MP	R	0	KI Feedback High Rail Indicator 0 = KI Feedback not equal to high rail 1 = KI Feedback equal to high rail

4.9.2 Filter Control Register (FILTERCTRL)

Address 00160004 – Filter 2 Control Register

Address 00190004 – Filter 1 Control Register

Address 001C0004 – Filter 0 Control Register

Figure 4-150. Filter Control Register (FILTERCTRL)

15	14	13	12	11	9	8
KI_ADDER_MODE	PERIOD_MULT_SEL	OUTPUT_MULT_SEL		YN_SCALE		NL_MODE
R/W-1	R/W-0	R/W-00		R/W-000		R/W-0

7	6	5	4	3	2	1	0
KD_STALL	KI_STALL	KP_OFF	KD_OFF	KI_OFF	FORCE_START	USE_CPU_SAMPLE	FILTER_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-150. Filter Control Register (FILTERCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	KI_ADDER_MODE	R/W	1	Configures addition of Xn and Xn-1 in Integral branch 0 = Only Xn used for addition (Xn + 0) 1 = Xn + Xn-1 used for addition (Default)
14	PERIOD_MULT_SEL	R/W	0	Selects output multiplicand used for multiplying with filter output to calculate DPWM Period value in Resonant Mode 0 = Switching period received from Loop Mux module (Default) 1 = KComp received from Loop Mux module
13-12	OUTPUT_MULT_SEL	R/W	00	Selects output multiplicand used for multiplying with filter output to calculate DPWM Duty value 0 = KComp received from Loop Mux module (Default) 1 = Switching period received from Loop Mux module 2 = Feed-Forward value received from Loop Mux module 3 = Resonant Duty value received from DPWM Module
11-9	YN_SCALE	R/W	000	Controls scaling of Yn value to compensate for filter coefficient scaling -4 = Filter output (Yn) left shifted by 4 -3 = Filter output (Yn) left shifted by 3 -2 = Filter output (Yn) left shifted by 2 -1 = Filter output (Yn) left shifted by 1 0 = Filter output (Yn) not scaled (Default) 1 = Filter output (Yn) right shifted by 1 2 = Filter output (Yn) right shifted by 2 3 = Filter output (Yn) right shifted by 3
8	NL_MODE	R/W	0	Sets non-linear gain table configuration. Coefficient Bin mapping is controlled by Coefficient Configuration Register. Limit configuration is controlled by the Filter Nonlinear Limit Registers 0 = Non-symmetric mode (Default) 1 = Symmetric mode
7	KD_STALL	R/W	0	Freezes KD Branch, KD_YN remains at current value 0 = KD_YN recalculated on each filter update (Default) 1 = KD_YN stalled at present value
6	KI_STALL	R/W	0	Freezes KI Branch, KI_YN remains at current value 0 = KI_YN recalculated on each filter update (Default) 1 = KI_YN stalled at present value

Table 4-150. Filter Control Register (FILTERCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	KP_OFF	R/W	0	Turns off the KP branch 0 = KP branch calculating new outputs (Default) 1 = KP branch turned off
4	KD_OFF	R/W	0	Turns off the KD branch, KD_YN cleared to zero 0 = KD branch calculating new outputs (Default) 1 = KD branch turned off
3	KI_OFF	R/W	0	Turns off the KI branch, KI_YN cleared to zero 0 = KI branch calculating new outputs (Default) 1 = KI branch halted
2	FORCE_START	R/W	0	Initiates a filter calculation under firmware control 0 = No calculation started (Default) 1 = Calculation started
1	USE_CPU _SAMPLE	R/W	0	Forces filter to use error sample from CPU XN register () 0 = Filter Mode, input data received from EADC (Default) 1 = CPU Mode, input data based on CPU XN register
0	FILTER_EN	R/W	1	Filter Enable 0 = Disables Filter operation 1 = Enables Filter operation (Default)

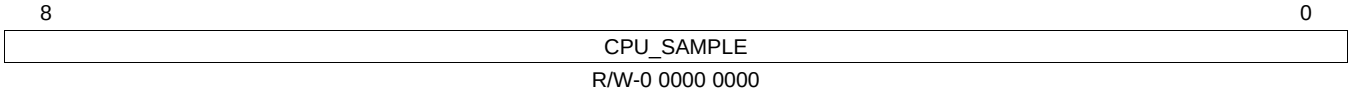
4.9.3 CPU XN Register (CPUXN)

Address 00160008 – Filter 2 CPU XN Register

Address 00190008 – Filter 1 CPU XN Register

Address 001C0008 – Filter 0 CPU XN Register

Figure 4-151. CPU XN Register (CPUXN)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-151. CPU XN Register (CPUXN) Register Field Descriptions

Bit	Field	Type	Reset	Description
8-0	CPU_SAMPLE	R/W	0 0000 0000	Forced Xn value, allows processor to use filter as ALU. Set Bit 2 of Filter Control Register to '1' to force CPU_SAMPLE as input to Filter.

4.9.4 Filter XN Read Register (FILTERXNREAD)

Address 0016000C – Filter 2 XN Read Register

Address 0019000C – Filter 1 XN Read Register

Address 001C000C – Filter 0 XN Read Register

Figure 4-152. Filter XN Read Register (FILTERXNREAD)

24	16	15	9	8	0
XN_M1		Reserved		XN	
R-0		R-000 0000		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-152. Filter XN Read Register (FILTERXNREAD) Register Field Descriptions

Bit	Field	Type	Reset	Description
24-16	XN_M1	R	0	9-bit signed XN_M1 register value, read-only
15-9	Reserved	R	000 0000	
8-0	XN	R	0	9-bit signed XN register value, read-only

4.9.5 Filter KI_YN Read Register (FILTERKIYNREAD)

Address 00160010 – Filter 2 KI_YN Read Register

Address 00190010 – Filter 1 KI_YN Read Register

Address 001C0010 – Filter 0 KI_YN Read Register

Figure 4-153. Filter KI_YN Read Register (FILTERKIYNREAD)

23		0
KI_YN		
R-0		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-153. Filter KI_YN Read Register (FILTERKIYNREAD) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	KI_YN	R	0	24-bit signed KI_YN register value, read-only

4.9.6 Filter KD_YN Read Register (FILTERKDYNREAD)

Address 00160014 – Filter 2 KD_YN Register

Address 00190014 – Filter 1 KD_YN Register

Address 001C0014 – Filter 0 KD_YN Register

Figure 4-154. Filter KD_YN Read Register (FILTERKDYNREAD)

23		0
KD_YN		
R-0		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-154. Filter KD_YN Read Register (FILTERKDYNREAD) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	KD_YN	R	0	24-bit signed KD_YN register value, read-only

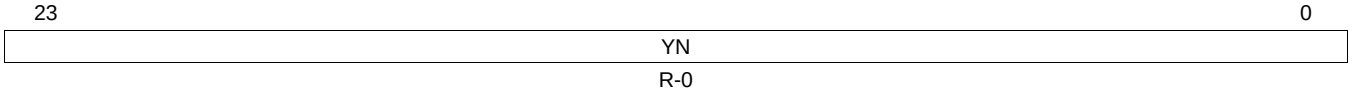
4.9.7 Filter YN Read Register (FILTERYNREAD)

Address 00160018 – Filter YN Read Register

Address 00190018 – Filter YN Read Register

Address 001C0018 – Filter YN Read Register

Figure 4-155. Filter YN Read Register (FILTERYNREAD)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-155. 9.7 Filter YN Read Register (FILTERYNREAD) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	YN	R	0	24-bit signed YN register value, read-only

4.9.8 Coefficient Configuration Register (COEFCONFIG)

Address 0016001C – Filter 2 Coefficient Configuration Register

Address 0019001C – Filter 1 Coefficient Configuration Register

Address 001C001C – Filter 0 Coefficient Configuration Register

Figure 4-156. Coefficient Configuration Register (COEFCONFIG)

27	26						24
BIN6_ALPHA	BIN6_CONFIG						
R/W-0	R/W-000						
23	22			20	19	18	16
BIN5_ALPHA	BIN5_CONFIG				BIN4_ALPHA	BIN4_CONFIG	
R/W-0	R/W-000				R/W-0	R/W-000	
15	14			12	11	10	8
BIN3_ALPHA	BIN3_CONFIG				BIN2_ALPHA	BIN2_CONFIG	
R/W-0	R/W-000				R/W-0	R/W-000	
7	6	5	4		3	2	1	0
BIN1_ALPHA	BIN1_CONFIG				BIN0_ALPHA	BIN0_CONFIG	
R/W-0	R/W-000				R/W-0	R/W-000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-156. Coefficient Configuration Register (COEFCONFIG) Register Field Descriptions

Bit	Field	Type	Reset	Description
27	BIN6_ALPHA	R/W	0	Selects which alpha value to use in Bin 6 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample 0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default) 1 = Bank 1 KD Alpha (KD_ALPHA_1) selected
26-24	BIN6_CONFIG	R/W	000	Selects which coefficient set to place in Bin 6 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample. 0 = Coefficient Set A Selected (Default) 1 = Coefficient Set B Selected 2 = Coefficient Set C Selected 3 = Coefficient Set D Selected 4 = Coefficient Set E Selected 5 = Coefficient Set F Selected 6 = Coefficient Set G Selected
23	BIN5_ALPHA	R/W	0	Selects which alpha value to use in Bin 5 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample 0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default) 1 = Bank 1 KD Alpha (KD_ALPHA_1) selected
22-20	BIN5_CONFIG	R/W	000	Selects which coefficient set to place in Bin 5 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample. 0 = Coefficient Set A Selected (Default) 1 = Coefficient Set B Selected 2 = Coefficient Set C Selected 3 = Coefficient Set D Selected 4 = Coefficient Set E Selected 5 = Coefficient Set F Selected 6 = Coefficient Set G Selected
19	BIN4_ALPHA	R/W	0	Selects which alpha value to use in Bin 4 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample 0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default) 1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Table 4-156. Coefficient Configuration Register (COEFCONFIG) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-16	BIN4_CONFIG	R/W	000	Selects which coefficient set to place in Bin 4 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample. 0 = Coefficient Set A Selected (Default) 1 = Coefficient Set B Selected 2 = Coefficient Set C Selected 3 = Coefficient Set D Selected 4 = Coefficient Set E Selected 5 = Coefficient Set F Selected 6 = Coefficient Set G Selected
15	BIN3_ALPHA	R/W	0	Selects which alpha value to use in Bin 3 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample 0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default) 1 = Bank 1 KD Alpha (KD_ALPHA_1) selected
14-12	BIN3_CONFIG	R/W	000	Selects which coefficient set to place in Bin 3 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample. 0 = Coefficient Set A Selected (Default) 1 = Coefficient Set B Selected 2 = Coefficient Set C Selected 3 = Coefficient Set D Selected 4 = Coefficient Set E Selected 5 = Coefficient Set F Selected 6 = Coefficient Set G Selected
11	BIN2_ALPHA	R/W	0	Selects which alpha value to use in Bin 2 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample 0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default) 1 = Bank 1 KD Alpha (KD_ALPHA_1) selected
10-8	BIN2_CONFIG	R/W	000	Selects which coefficient set to place in Bin 2 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample. 0 = Coefficient Set A Selected (Default) 1 = Coefficient Set B Selected 2 = Coefficient Set C Selected 3 = Coefficient Set D Selected 4 = Coefficient Set E Selected 5 = Coefficient Set F Selected 6 = Coefficient Set G Selected
7	BIN1_ALPHA	R/W	0	Selects which alpha value to use in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample 0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default) 1 = Bank 1 KD Alpha (KD_ALPHA_1) selected
6-4	BIN1_CONFIG	R/W	000	Selects which coefficient set to place in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample. 0 = Coefficient Set A Selected (Default) 1 = Coefficient Set B Selected 2 = Coefficient Set C Selected 3 = Coefficient Set D Selected 4 = Coefficient Set E Selected 5 = Coefficient Set F Selected 6 = Coefficient Set G Selected
3	BIN0_ALPHA	R/W	0	Selects which alpha value to use in Bin 0 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample 0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default) 1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Table 4-156. Coefficient Configuration Register (COEFCONFIG) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BIN0_CONFIG	R/W	000	Selects which coefficient set to place in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample. 0 = Coefficient Set A Selected (Default) 1 = Coefficient Set B Selected 2 = Coefficient Set C Selected 3 = Coefficient Set D Selected 4 = Coefficient Set E Selected 5 = Coefficient Set F Selected 6 = Coefficient Set G Selected

4.9.9 Filter KP Coefficient 0 Register (FILTERKPCOEF0)

Address 00160020 – Filter 2 KP Coefficient 0 Register

Address 00190020 – Filter 1 KP Coefficient 0 Register

Address 001C0020 – Filter 0 KP Coefficient 0 Register

Figure 4-157. Filter KP Coefficient 0 Register (FILTERKPCOEF0)

31	16	15	0
KP_COEF_1		KP_COEF_0	
R/W-0000 0000 0000 0000		R/W-0100 0010 0011 0100	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-157. Filter KP Coefficient 0 Register (FILTERKPCOEF0) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KP_COEF_1	R/W	0000 0000 0000 0000	KP Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
15-0	KP_COEF_0	R/W	0100 0010 0011 0100	KP Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

4.9.10 Filter KP Coefficient 1 Register (FILTERKPCOEF1)

Address 00160024 – Filter 2 KP Coefficient 1 Register

Address 00190024 – Filter 1 KP Coefficient 1 Register

Address 001C0024 – Filter 0 KP Coefficient 1 Register

Figure 4-158. Filter KP Coefficient 1 Register (FILTERKPCOEF1)

15	0
KP_COEF_2	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-158. Filter KP Coefficient 1 Register (FILTERKPCOEF1) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	KP_COEF_2	R/W	0000 0000 0000 0000	KP Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

4.9.11 Filter KI Coefficient 0 Register (FILTERKICOEF0)

Address 00160028 – Filter 2 KI Coefficient 0 Register

Address 00190028 – Filter 1 KI Coefficient 0 Register

Address 001C0028 – Filter 0 KI Coefficient 0 Register

Figure 4-159. Filter KI Coefficient 0 Register (FILTERKICOEF0)

31	16	15	0
KI_COEF_1		KI_COEF_0	
R/W-0000 0000 0000 0000		R/W-0010 0100 0001 0010	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-159. Filter KI Coefficient 0 Register (FILTERKICOEF0) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KI_COEF_1	R/W	0000 0000 0000 0000	KI Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
15-0	KI_COEF_0	R/W	0010 0100 0001 0010	KI Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

4.9.12 Filter KI Coefficient 1 Register (FILTERKICOEF1)

Address 0016002C – Filter 2 KI Coefficient 1 Register

Address 0019002C – Filter 1 KI Coefficient 1 Register

Address 001C002C – Filter 0 KI Coefficient 1 Register

Figure 4-160. Filter KI Coefficient 1 Register (FILTERKICOEF1)

31	16	15	0
KI_COEF_3		KI_COEF_2	
R/W-0000 0000 0000 0000		R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-160. Filter KI Coefficient 1 Register (FILTERKICOEF1) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KI_COEF_3	R/W	0000 0000 0000 0000	KI Coefficient 3, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
15-0	KI_COEF_2	R/W	0000 0000 0000 0000	KI Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

4.9.13 Filter KD Coefficient 0 Register (FILTERKDCOEF0)

Address 00160030 – Filter 2 KD Coefficient 0 Register

Address 00190030 – Filter 1 KD Coefficient 0 Register

Address 001C0030 – Filter 0 KD Coefficient 0 Register

Figure 4-161. Filter KD Coefficient 0 Register (FILTERKDCOEF0)

31	16	15	0
KD_COEF_1		KD_COEF_0	
R/W-0000 0000 0000 0000		R/W-1100 0100 0000 0001	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-161. Filter KD Coefficient 0 Register (FILTERKDCOEF0) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KD_COEF_1	R/W	0000 0000 0000 0000	KD Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
15-0	KD_COEF_0	R/W	1100 0100 0000 0001	KD Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

4.9.14 Filter KD Coefficient 1 Register (FILTERKDCOEF1)

Address 00160034 – Filter 2 KD Coefficient 1 Register

Address 00190034 – Filter 1 KD Coefficient 1 Register

Address 001C0034 – Filter 0 KD Coefficient 1 Register

Figure 4-162. Filter KD Coefficient 1 Register (FILTERKDCOEF1)

15	0
KD_COEF_2	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-162. Filter KD Coefficient 1 Register (FILTERKDCOEF1) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	KD_COEF_2	R/W	0000 0000 0000 0000	KD Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

4.9.15 Filter KD Alpha Register (FILTERKDALPHA)

Address 00160038 – Filter 2 KD Alpha Register

Address 00190038 – Filter 1 KD Alpha Register

Address 001C0038 – Filter 0 KD Alpha Register

Figure 4-163. Filter KD Alpha Register (FILTERKDALPHA)

24	16	15	9	8	0
KD_ALPHA_1		Reserved		KD_ALPHA_0	
R/W-0 0000 0000		R-0		R/W-0 0101 0010	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-163. Filter KD Alpha Register (FILTERKDALPHA) Register Field Descriptions

Bit	Field	Type	Reset	Description
24-16	KD_ALPHA_1	R/W	0 0000 0000	Bank 1 KD Alpha, 9-bit signed value, configurable to any bin using the Coefficient Control Register
15-9	Reserved	R	0	
8-0	KD_ALPHA_0	R/W	0 0101 0010	Bank 0 KD Alpha, 9-bit signed value, configurable to any bin using the Coefficient Control Register

4.9.16 Filter Nonlinear Limit Register 0 (FILTERNL0)

Address 0016003C – Filter 2 Nonlinear Limit Register 0

Address 0019003C – Filter 1 Nonlinear Limit Register 0

Address 001C003C – Filter 0 Nonlinear Limit Register 0

Figure 4-164. Filter Nonlinear Limit Register 0 (FILTERNL0)

24	16	15	9	8	0
LIMIT1		Reserved		LIMIT0	
R/W-0 0000 0000		R-0		R/W-0 1111 1111	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-164. Filter Nonlinear Limit Register 0 (FILTERNL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
24-16	LIMIT1	R/W	0 0000 0000	Configures LIMIT1 in Nonlinear Coefficient tables
15-9	Reserved	R	0	
8-0	LIMIT0	R/W	0 1111 1111	Configures LIMIT0 in Nonlinear Coefficient tables

4.9.17 Filter Nonlinear Limit Register 1 (FILTERNL1)

Address 00160040 – Filter 2 Nonlinear Limit Register 1

Address 00190040 – Filter 1 Nonlinear Limit Register 1

Address 001C0040 – Filter 0 Nonlinear Limit Register 1

Figure 4-165. Filter Nonlinear Limit Register 1 (FILTERNL1)

24	16	15	9	8	0
LIMIT3		Reserved		LIMIT2	
R/W-0 0000 0000		R-0		R/W-0 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-165. Filter Nonlinear Limit Register 1 (FILTERNL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
24-16	LIMIT3	R/W	0 0000 0000	Configures LIMIT3 in Nonlinear Coefficient tables
15-9	Reserved	R	0	
8-0	LIMIT2	R/W	0 0000 0000	Configures LIMIT2 in Nonlinear Coefficient tables

4.9.18 Filter Nonlinear Limit Register 2 (FILTERNL2)

Address 00160044 – Filter 2 Nonlinear Limit Register 2

Address 00190044 – Filter 1 Nonlinear Limit Register 2

Address 001C0044 – Filter 0 Nonlinear Limit Register 2

Figure 4-166. Filter Nonlinear Limit Register 2 (FILTERNL2)

24	16	15	9	8	0
LIMIT5		Reserved		LIMIT4	
R/W-0 0000 0000		R-0		R/W-0 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-166. Filter Nonlinear Limit Register 2 (FILTERNL2) Register Field Descriptions

Bit	Field	Type	Reset	Description
24-16	LIMIT5	R/W	0 0000 0000	Configures LIMIT5 in Nonlinear Coefficient tables
15-9	Reserved	R	0	
8-0	LIMIT4	R/W	0 0000 0000	Configures LIMIT4 in Nonlinear Coefficient tables

4.9.19 Filter KI Feedback Clamp High Register (FILTERKICLPHI)

Address 00160048 – Filter 2 KI Feedback Clamp High Register

Address 00190048 – Filter 1 KI Feedback Clamp High Register

Address 001C0048 – Filter 0 KI Feedback Clamp High Register

Figure 4-167. Filter KI Feedback Clamp High Register (FILTERKICLPHI)

23	0
KI_CLAMP_HIGH	
R/W-0111 1111 1111 1111 1111 1111	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-167. Filter KI Feedback Clamp High Register (FILTERKICLPHI) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	KI_CLAMP_HIGH	R/W	0111 1111 1111 1111 1111 1111	Sets the upper limit of KI_YN value. If calculated KI_YN exceeds this threshold, the KI_YN register will be set to KI_CLAMP_HIGH

4.9.20 Filter KI Feedback Clamp Low Register (FILTERKICLPLO)

Address 0016004C – Filter 2 KI Feedback Clamp Low Register

Address 0019004C – Filter 1 KI Feedback Clamp Low Register

Address 001C004C – Filter 0 KI Feedback Clamp Low Register

Figure 4-168. Filter KI Feedback Clamp Low Register (FILTERKICLPLO)

23	0
KI_CLAMP_LOW	
R/W-0000 0000 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-168. Filter KI Feedback Clamp Low Register (FILTERKICLPLO) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	KI_CLAMP_LOW	R/W	0000 0000 0000 0000 0000 0000	Sets the lower limit of KI_YN value. If calculated KI_YN falls below this threshold, the KI_YN register will be set to KI_CLAMP_LOW

4.9.21 Filter YN Clamp High Register (FILTERYNCLPHI)

Address 00160050 – Filter 2 YN Clamp High Register

Address 00190050 – Filter 1 YN Clamp High Register

Address 001C0050 – Filter 0 YN Clamp High Register

Figure 4-169. Filter YN Clamp High Register (FILTERYNCLPHI)

23		0
YN_CLAMP_HIGH		
R/W-0111 1111 1111 1111 1111 1111		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-169. Filter YN Clamp High Register (FILTERYNCLPHI) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	YN_CLAMP_HIGH	R/W	0111 1111 1111 1111 1111 1111	Sets the upper limit of YN value. If calculated YN exceeds this threshold, the YN register will be set to YN_CLAMP_HIGH

4.9.22 Filter YN Clamp Low Register (FILTERYNCLPLO)

Address 00160054 – Filter 2 YN Clamp Low Register

Address 00190054 – Filter 1 YN Clamp Low Register

Address 001C0054 – Filter 0 YN Clamp Low Register

Figure 4-170. Filter YN Clamp Low Register (FILTERYNCLPLO)

23		0
YN_CLAMP_LOW		
R/W-0000 0000 0000 0000 0000 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-170. Filter YN Clamp Low Register (FILTERYNCLPLO) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	YN_CLAMP_LOW	R/W	0000 0000 0000 0000 0000 0000	Sets the lower limit of YN value. If calculated YN falls below this threshold, the YN register will be set to YN_CLAMP_LOW

4.9.23 Filter Output Clamp High Register (FILTEROCLPHI)

Address 00160058 – Filter 2 Output Clamp High Register

Address 00190058 – Filter 1 Output Clamp High Register

Address 001C0058 – Filter 0 Output Clamp High Register

Figure 4-171. Filter Output Clamp High Register (FILTEROCLPHI)

23																							0
OUTPUT_CLAMP_HIGH																							
R/W-11 1111 1111 1111 1111																							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-171. Filter Output Clamp High Register (FILTEROCLPHI) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	OUTPUT_CLAMP_HIGH	R/W	11 1111 1111 1111 1111	Sets the upper limit of filter output value. If calculated filter output exceeds this threshold, the filter output will be set to OUTPUT_CLAMP_HIGH

4.9.24 Filter Output Clamp Low Register (FILTEROCLPLO)

Address 0016005C – Filter 2 Output Clamp Low Register

Address 0019005C – Filter 1 Output Clamp Low Register

Address 001C005C – Filter 0 Output Clamp Low Register

Figure 4-172. Filter Output Clamp Low Register (FILTEROCLPLO)

17	0
OUTPUT_CLAMP_LOW	
R/W-00 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-172. Filter Output Clamp Low Register (FILTEROCLPLO) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-0	OUTPUT_CLAMP_LOW	R/W	00 0000 0000 0000 0000	Sets the lower limit of filter output value. If calculated filter output falls below this threshold, the filter output will be set to OUTPUT_CLAMP_LOW

4.9.25 Filter Preset Register (FILTERPRESET)

Address 00160060 – Filter 2 Filter Preset Register

Address 00190060 – Filter 1 Filter Preset Register

Address 001C0060 – Filter 0 Filter Preset Register

Figure 4-173. Filter Preset Register (FILTERPRESET)

27	26 24	23 16
PRESET_EN	PRESET_REG_SEL	PRESET_VALUE
R/W-00	R/W-000	R/W-0000 0000 0000 0000 0000 0000

15 0
PRESET_VALUE
R/W-0000 0000 0000 0000 0000 0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-173. Filter Preset Register (FILTERPRESET) Register Field Descriptions

Bit	Field	Type	Reset	Description
27	PRESET_EN	R/W	00	Set to '1' to initiate write of internal filter register (Self cleared by hardware after successful programming)
26-24	PRESET_REG_SEL	R/W	000	Selects internal filter register to preset by processor 0 = XN_M1 Register (only bits 10:0 of PRESET_VALUE will be programmed into register) 1 = KI_YN Register 2 = KD_YN Register 3 = YN Register 4 = 18-bit Filter Data Register (after multiplication)
23-0	PRESET_VALUE	R/W	0000 0000 0000 0000 0000 0000	Value to preset into selected register

4.10 Front End Control Registers

Registers for Front End Control modules 0-2 are identical in their bit definitions.

4.10.1 Ramp Control Register (RAMPCTRL)

Address 0x0018_0000 – Front End Control 2 Ramp Control Register

Address 0x001B_0000 – Front End Control 1 Ramp Control Register

Address 0x001E_0000 – Front End Control 0 Ramp Control Register

Figure 4-174. Ramp Control Register (RAMPCTRL)

29															16
SYNC_FET_RAMP_START															
R/W-00 0000 0000 0000															
15				13	12	11	10	9	8						
Reserved					RAMP_SAT_EN	RAMP_COMP_INT_EN	RAMP_DLY_INT_EN	PREBIAS_INT_EN	PCM_START_SEL						
R-00					R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
7		6		5	4	3	2	1	0						
SYNC_FET_EN		MASTER_SEL			SLAVE_COMP_EN	SLAVE_DELAY_EN	CONTROL_EN	FIRMWARE_START	RAMP_EN						
R/W-0		R/W-00			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-174. Ramp Control Register (RAMPCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
29-16	SYNC_FET_RAMP_START	R/W	00 0000 0000 0000	Provides the starting value for the SyncFET Ramp with a resolution of High Frequency Oscillator Period/bit
15-13	Reserved	R	00	
12	RAMP_SAT_EN	R/W	0	Enables addition or subtraction of DAC Saturation Step when EADC is in saturation. 0 = DAC Saturation Step logic is disabled, DAC incremented/decremented by value calculated by Ramp logic when EADC is in saturation (Default) 1 = DAC Saturation Step logic is enabled, DAC incremented/decremented by value stored in DAC Saturation Step register when EADC is in saturation
11	RAMP_COMP_INT_EN	R/W	0	Enables Ramp I/F Interrupt when soft-start/power-down ramp procedure is complete 0 = Soft-start/Power-Down Ramp Complete Interrupt is disabled (Default) 1 = Soft-start/Power-Down Ramp Complete Interrupt is enabled
10	RAMP_DLY_INT_EN	R/W	0	Enables Ramp I/F Interrupt when ramp delay procedure is complete 0 = Soft-start/Power-Down Ramp Delay Complete Interrupt is disabled (Default) 1 = Soft-start/Power-Down Ramp Delay Complete Interrupt is enabled
9	PREBIAS_INT_EN	R/W	0	Enables Ramp I/F Interrupt when Pre-Bias procedure is completed 0 = Pre-bias Complete Interrupt is disabled (Default) 1 = Pre-bias Complete Interrupt is enabled
8	PCM_START_SEL	R/W	0	Peak Current Mode Ramp Start Value Select 0 = Ramp starts from value programmed in DAC_VALUE bits in EADC_DAC_VALUE Register (Default) 1 = Ramp starts from filter output selected by PCM_FILTER_SEL bits in Loop Mux register PCMCTRL
7	SYNC_FET_EN	R/W	0	Enables SyncFET Ramp Operation 0 = SyncFET Ramp Operation disabled (Default) 1 = SyncFET Ramp Operation enabled

Table 4-174. Ramp Control Register (RAMPCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	MASTER_SEL	R/W	00	Selects Master Ramp I/F in slave mode 0 = Front End Control 0 acts as master (Default) 1 = Front End Control 1 acts as master 2 = Front End Control 2 acts as master
4	SLAVE_COMP_EN	R/W	0	Enables syncing of ramp start to Master Ramp I/F Complete pulse 0 = Ramp initiated by Master Ramp Complete pulse disabled (Default) 1 = Ramp initiated by Master Ramp Complete pulse enabled
3	SLAVE_DELAY_EN	R/W	0	Enables syncing of ramp start to Master Ramp I/F Delay Complete pulse 0 = Ramp initiated by Master Ramp Delay Complete pulse disabled (Default) 1 = Ramp initiated by Master Ramp Delay Complete pulse enabled
2	CONTROL_EN	R/W	0	Enables PMBus Control line to initiate ramp 0 = PMBus Control does not initiate ramp (Default) 1 = PMBus Control initiates ramp
1	FIRMWARE_START	R/W	0	Ramp start bit, self-clearing by ramp logic 0 = No ramp sequence initiated by firmware (Default) 1 = Ramp sequence initiated by firmware
0	RAMP_EN	R/W	0	Enable Ramp Logic (Pre-biasing should be disabled before asserting ramp, bit 16 of Pre-Bias Control Register) 0 = No soft start or power-down ramp controlled by hardware (Default) 1 = Enables hardware control of soft start or power-down ramp

4.10.2 Ramp Status Register (RAMPSTAT)

Address 0x0018_0004 – Front End Control 2 Ramp Status Register

Address 0x001B_0004 – Front End Control 1 Ramp Status Register

Address 0x001E_0004 – Front End Control 0 Ramp Status Register

Figure 4-175. Ramp Status Register (RAMPSTAT)

11	10	9	8
EADC_DONE_RAW	RAMP_COMP_INT_STATUS	RAMP_DLY_INT_STATUS	PREBIAS_INT_STATUS
R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
EADC_SAT_HIGH	EADC_SAT_LOW	EADC_EOC	PREBIAS_BUSY	RAMP_BUSY	RAMP_COMP_STATUS	RAMP_DLY_STATUS	PREBIAS_STATUS
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-175. Ramp Status Register (RAMPSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
11	EADC_DONE_RAW	R	0	EADC Conversion Done Raw Status 0 = EADC Conversion has not completed 1 = EADC Conversion has completed
10	RAMP_COMP_INT_STATUS	R	0	Ramp Delay Complete latched status – clear on read 0 = No Ramp Delay Complete has been declared 1 = Ramp Delay Complete has been declared
9	RAMP_DLY_INT_STATUS	R	0	Ramp Delay Complete latched status – clear on read 0 = No Ramp Delay Complete has been declared 1= Ramp Delay Complete has been declared
8	PREBIAS_INT_STATUS	R	0	Pre-Bias Complete latched status – clear on read 0 = No Pre-Bias Complete has been declared 1 = Pre-Bias Complete has been declared
7	EADC_SAT_HIGH	R	0	EADC Saturation High Indicator 0 = EADC output is not saturated at high limit 1 = EADC output is saturated at high limit
6	EADC_SAT_LOW	R	0	EADC Saturation Low Indicator 0 = EADC output is not saturated at low limit 1 = EADC output is saturated at low limit
5	EADC_EOC	R	0	Indicates EADC end of conversion
4	PREBIAS_BUSY	R	0	Pre-Bias Busy 0 = Pre-Bias is not in progress 1 = Pre-Bias in progress
3	RAMP_BUSY	R	0	Ramp Busy 0 = Soft-Start/Power-Down Ramp is not in progress 1 = Soft-Start/Power-Down Ramp is in progress
2	RAMP_COMP_STATUS	R	0	Ramp Complete, Raw Status 0 = Ramp procedure is not complete 1 = Ramp procedure is complete
1	RAMP_DLY_STATUS	R	0	Ramp Delay Complete, Raw Status 0 = Ramp delay procedure is not complete 1 = Ramp delay procedure is complete
0	PREBIAS_STATUS	R	0	Pre-Bias Complete, Raw Status 0 = Pre-Bias is not completed 1 = Pre-Bias is completed

4.10.3 Ramp Cycle Register (RAMPCYCLE)

Address 0x0018_0008 – Front End Control 2 Ramp Cycle Register

Address 0x001B_0008 – Front End Control 1 Ramp Cycle Register

Address 0x001E_0008 – Front End Control 0 Ramp Cycle Register

Figure 4-176. Ramp Cycle Register (RAMPCYCLE)

23								8
DELAY_CYCLES								
R/W-0000 0000 0000 0000								
7	6							0
Reserved	SWITCH_CYC_PER_STEP							
R-0	R/W-000 0000							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-176. Ramp Cycle Register (RAMPCYCLE) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-8	DELAY_CYCLES	R/W	0000 0000 0000 0000	Configures the number of delay cycles before an initiation of ramp sequence. Each delay cycle consists of n switching cycles, as specified by SWITCH_CYC_PER_STEP (Bits 6-0). Number of delay cycles can vary from 0 to 65535 0 = Ramp starts without delay (Default) 1 = Ramp starts after (1*SWITCH_CYC_PER_STEP) switching cycles 2 = Ramp starts after (2*SWITCH_CYC_PER_STEP) switching cycles ……. 65535 = Ramp starts after (65535*SWITCH_CYC_PER_STEP) switching cycles
7	Reserved	R	0	
6-0	SWITCH_CYC_PER_STEP	R/W	000 0000	Selects number of switching cycles per DAC step. Number of subcycles can vary from 1 to 128. 0 = 1 switching cycle per step (Default) 1 = 2 subcycles per cycle 2 = 3 subcycles per cycle ……. 127 = 128 subcycles per cycle

4.10.4 EADC DAC Value Register (EADCDAC)

Address 0x0018_000C – Front End Control 2 EADC DAC Value Register

Address 0x001B_000C – Front End Control 1 EADC DAC Value Register

Address 0x001E_000C – Front End Control 0 EADC DAC Value Register

Figure 4-177. EADC DAC Value Register (EADCDAC)

16	15	14	13 ... 0
DAC_DITHER_ON_SAMPLE	DAC_DITHER_EN	Reserved	DAC_VALUE
R/W-0	R/W-0	R-0	R/W-00 1111 1111 0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-177. EADC DAC Value Register (EADCDAC) Register Field Descriptions

Bit	Field	Type	Reset	Description
16	DAC_DITHER_ON_SAMPLE	R/W	0	DAC Dithering on based on Sample Trigger 0 = DAC Dithering disabled on input sample trigger (Default) 1 = DAC Dithering enabled on input sample trigger
15	DAC_DITHER_EN	R/W	0	DAC Dithering Enable 0 = DAC Dithering disabled (Default) 1 = DAC Dithering enabled
14	Reserved	R	0	
13-0	DAC_VALUE	R/W	00 1111 1111 0000	Programmable DAC Value, effective LSB equals 0.09765625mV

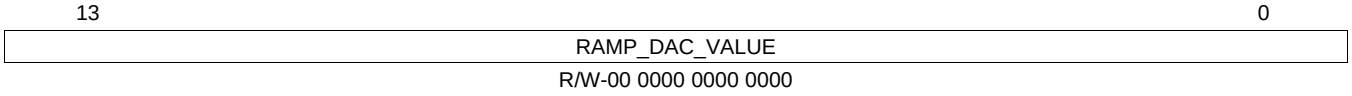
4.10.5 Ramp DAC Ending Value Register (RAMPDACEND)

Address 0x0018_0010 – Front End Control 2 Ramp DAC Ending Register

Address 0x001B_0010 – Front End Control 1 Ramp DAC Ending Register

Address 0x001E_0010 – Front End Control 0 Ramp DAC Ending Register

Figure 4-178. Ramp DAC Ending Value Register (RAMPDACEND)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-178. Ramp DAC Ending Value Register (RAMPDACEND) Register Field Descriptions

Bit	Field	Type	Reset	Description
13-0	RAMP_DAC _VALUE	R/W	00 0000 0000 0000	Programmable Ramp Ending DAC Value, LSB equals 0.09765625mV

4.10.6 DAC Step Register (DACSTEP)

Address 0x0018_0014 – Front End Control 2 DAC Step Register

Address 0x001B_0014 – Front End Control 1 DAC Step Register

Address 0x001E_0014 – Front End Control 0 DAC Step Register

Figure 4-179. DAC Step Register (DACSTEP)

17		0
DAC_STEP		
R/W-00 0000 0000 0000 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-179. DAC Step Register (DACSTEP) Register Field Descriptions

Bit	Field	Type	Reset	Description
17-0	DAC_STEP	R/W	00 0000 0000 0000 0000	Programmable 18-bit unsigned DAC Step. Bits 17:10 represent the real portion of the DAC Step (0-255 DAC counts at bit resolution of 0.09765625mV). Bits 9:0 represent the fractional portion of the DAC Step.

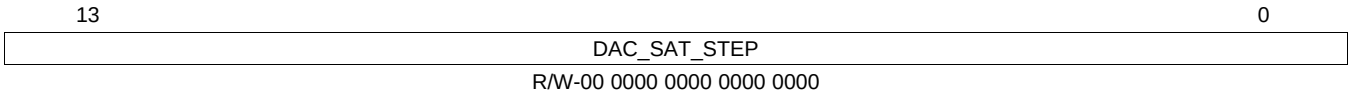
4.10.7 DAC Saturation Step Register (DACSATSTEP)

Address 0x0018_0018 – Front End Control 2 DAC Saturation Step Register

Address 0x001B_0018 – Front End Control 1 DAC Saturation Step Register

Address 0x001E_0018 – Front End Control 0 DAC Saturation Step Register

Figure 4-180. DAC Saturation Step Register (DACSATSTEP)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-180. DAC Saturation Step Register (DACSATSTEP) Register Field Descriptions

Bit	Field	Type	Reset	Description
13-0	DAC_SAT_STEP	R/W	00 0000 0000 0000	Programmable DAC Saturation Step, LSB equals 0.009765625mV 0 = DAC not adjusted on EADC saturation during ramp (Default) 1 = DAC adjusted by 1 DAC count on EADC saturation during ramp ….. 1023 = DAC adjusted by 1023 DAC counts on EADC saturation during ramp

4.10.8 EADC Control Register (EADCCTRL)

Address 0x0018_0020 – Front End Control 2 EADC Control Register

Address 0x001B_0020 – Front End Control 1 EADC Control Register

Address 0x001E_0020 – Front End Control 0 EADC Control Register

Figure 4-181. EADC Control Register (EADCCTRL)

28	27	26	25	24
D2S_COMP_EN	EN_HYST_HIGH	EN_HYST_LOW	SAMP_TRIG_SCALE	
R/W-0	R/W-0	R/W-0	R/W-0000	

23	22	21	20	19	16
SAMP_TRIG_SCALE		FRAME_SYNC_EN	SCFE_CNT_RST	SCFE_CNT_INIT	
R/W-0000		R/W-0	R/W-0	R/W-0000	

15	14	13	12	11	10	9	8
EADC_INV	AUTO_GAIN_SHIFT_MODE	AUTO_GAIN_SHIFT_EN	AVG_WEIGHT_EN	AVG_SPATIAL_EN	AVG_MODE_SEL		EADC_MODE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-00		R/W-000

7	6	5	4	3	2	1	0
EADC_MODE		AFE_GAIN		SCFE_GAIN_FILTER_SEL	SCFE_CLK_DIV_2	SCFE_ENA	EADC_ENA
R/W-000		R/W-11		R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-181. EADC Control Register (EADCCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
28	D2S_COMP_EN	R/W	0	Analog Front End Ramp Comparator Enable 0 = Analog Front End Ramp Comparator disabled (Default) 1 = Analog Front End Ramp Comparator enabled
27	EN_HYST_HIGH	R/W	0	Increase comparator trip point by ~70mV 0 = Disables increase of ramp comparator trip point (Default) 1 = Enables increase of ramp comparator trip point
26	EN_HYST_LOW	R/W	0	Decrease comparator trip point by ~70mV 0 = Disables decrease of ramp comparator trip point (Default) 1 = Enables decrease of ramp comparator trip point
25-22	SAMP_TRIG_SCALE	R/W	0000	Provides capability to mask incoming sample triggers to Front End Control 0 = EADC conversion initiated on every received sample trigger (Default) 1 = EADC conversion initiated once every 2 received sample triggers 2 = EADC conversion initiated once every 3 received sample triggers …. 15 = EADC conversion initiated once every 16 received sample triggers
21	FRAME_SYNC_EN	R/W	0	Enable synchronization of switched cap front end counter to Switching Cycle Frame boundary 0 = Switch Cap Front End Counter not synchronized to frame (Default) 1 = Switch Cap Front End Counter synchronized to frame boundary
20	SCFE_CNT_RST	R/W	0	Force reset of Switched Cap Front End Counter 0 = Switch Cap Front End Counter operational (Default) 1 = Switch Cap Front End Counter reset
19-16	SCFE_CNT_INIT	R/W	0000	Configures initial Switched Cap Front End Counter value out of reset or at start of switching cycle in Peak Current mode
15	EADC_INV	R/W	0	Enables EADC Data Inversion on data to filter module 0 = EADC Data is not inverted (Default) 1 = EADC Data Inverted

Table 4-181. EADC Control Register (EADCCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	AUTO_GAIN _SHIFT_MODE	R/W	0	Configures Automatic Gain Shifting mode 0 = Fixed mode, gain shifting dependent on saturation of EADC for decreasing gain and less than 1/4 of dynamic range for increasing gain (Default) 1 = NL mode, gain shifting dependent on Non-Linear limit thresholds
13	AUTO_GAIN _SHIFT_EN	R/W	0	Enables Automatic Gain Shifting mode 0 = Automatic Gain Shifting Mode disabled (Default) 1 = Automatic Gain Shifting Mode enabled
12	AVG_WEIGHT _EN	R/W	0	Enables weighted averaging in EADC averaging mode, only applicable in 4x and 8x averaging mode. For 4x averaging, two oldest samples are each weighted by 1/8, the next oldest sample has a weight of ¼ and the newest sample is weighted by ½. For 8x averaging, the four oldest samples are each weighted by 1/16, the next 2 oldest samples are weighted by 1/8, and the two newest samples are weighted by 1/4. 0 = Weighted averaging disabled (Default) 1 = Weighted averaging enabled
11	AVG_SPATIAL _EN	R/W	0	Enables spatial mode in EADC averaging mode 0 = Each sample trigger from a DPWM triggers 2, 4, or 8 EADC conversions then sends the average to the filter. 1 = Each sample trigger from DPWM triggers one EADC conversion. After 2, 4, or 8 conversions the average is sent to the filter
10-9	AVG_MODE_SEL	R/W	00	Averaging Mode Configuration 0 = 2x Averaging (Default) 1 = 4x Averaging 2 = 8x Averaging
8-6	EADC_MODE	R/W	000	Selects EADC Mode Operation 0 = Standard mode, EADC samples based on sample triggers from DPWM module (Default) 1 = Averaging Mode, configured by AVG_MODE_SEL 2 = Non-continuous SAR Mode 3 = Continuous SAR Mode 4 = Reserved 5 = Peak Current Mode 6 = Constant Power/Constant Current Control Mode (CPCC module controls switching between Standard Mode and Non-Continuous SAR Mode) 7 = Constant Power/Constant Current Control 2 Mode (CPCC module controls switching between Standard mode and Continuous SAR Mode)
5-4	AFE_GAIN	R/W	11	AFE Front End Gain Setting 0 = 1x Gain, 8mV/LSB 1 = 2x Gain, 4mV/LSB 2 = 4x Gain, 2mV/LSB 3 = 8x Gain, 1mV/LSB (Default)
3	SCFE_GAIN _FILTER_SEL	R/W	1	Switched Cap Noise Filter Enable 0 = Disables Switch Cap Noise Filter 1 = Enables Switch Cap Noise Filter (Default)
2	SCFE_CLK_DIV_2	R/W	1	Switched Cap Front End Clock Divider Select 0 = Switch Cap Period divide by 1 (128 ns nominal sample period) 1 = Switch Cap Period divide by 2 (Default – 64 ns nominal sample period)
1	SCFE_ENA	R/W	1	Switch Cap Front Enable 0 = Disables Switch Cap Front End logic 1 = Enables Switch Cap Front End logic (Default)
0	EADC_ENA	R/W	1	EADC Enable 0 = Disables EADC 1 = Enables EADC (Default)

4.10.9 Pre-Bias Control Register 0 (PREBIASCTRL0)

Address 0x0018_0028 – Front End Control 2 Pre-Bias Control Register 0

Address 0x001B_0028 – Front End Control 1 Pre-Bias Control Register 0

Address 0x001E_0028 – Front End Control 0 Pre-Bias Control Register 0

Figure 4-182. Pre-Bias Control Register 0 (PREBIASCTRL0)

17	16	15 8	7 0
PRE_BIAS_POL	PRE_BIAS_EN	PRE_BIAS_RANGE	PRE_BIAS_LIMIT
R/W-0	R/W-0	R/W-1111 1111	R/W-0000 0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-182. Pre-Bias Control Register 0 (PREBIASCTRL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
17	PRE_BIAS_POL	R/W	0	Configures polarity of received error voltage 0 = Error equals Vref-Vin (Default) 1 = Error equals Vin-Vref
16	PRE_BIAS_EN	R/W	0	Enable Pre-Biasing of Error ADC (Ramp should be disabled during pre-biasing, bit 0 of Ramp Control Register) 0 = Pre-Biasing has not been initiated (Default) 1 = Pre-Biasing by hardware has been enabled
15-8	PRE_BIAS_RANGE	R/W	1111 1111	Sets the acceptable range around the zero error point. If Error ADC value stays in range for number of samples specified by PRE_BIAS_LIMIT (Bits 7:0), PREBIAS_STATUS (Bit 0 of Ramp Status Register) is enabled. Range will be +/- PRE_BIAS_RANGE around zero error point.
7-0	PRE_BIAS_LIMIT	R/W	0000 0000	Sets the acceptable number of samples in which the Error ADC value stays in range before asserting PREBIAS_STATUS (Bit 0 of Ramp Status Register). Counter limit ranges from 0 to 255. If PREBIAS_STATUS is set, it will take PRE_BIAS_LIMIT samples outside of acceptable range before clearing PREBIAS_STATUS.

4.10.10 Pre-Bias Control Register 1 (PREBIASCTRL1)

Address 0x0018_002C – Front End Control 2 Pre-Bias Control Register 1

Address 0x001B_002C – Front End Control 1 Pre-Bias Control Register 1

Address 0x001E_002C – Front End Control 0 Pre-Bias Control Register 1

Figure 4-183. Pre-Bias Control Register 1 (PREBIASCTRL1)

23	16	15	14
SAMPLES_PER_ADJ		Reserved	
R/W-0000 0000		R-00	

13	0
MAX_DAC_ADJ	
R/W-00 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-183. Pre-Bias Control Register 1 (PREBIASCTRL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-16	SAMPLES_PER_ADJ	R/W	0000 0000	Configures the number of EADC samples between Pre-Bias DAC setpoint adjustments 0 = DAC Setpoint adjustment on each EADC sample 1 = DAC Setpoint adjustment after2 EADC sample 2 = DAC Setpoint adjustment after 3 EADC samples ……. 255 = DAC Setpoint adjustment after 256 EADC samples
15-14	Reserved	R	00	
13-0	MAX_DAC_ADJ	R/W	00 0000 0000 0000	Configures the maximum DAC setpoint adjustment step

4.10.11 SAR Control Register (SARCTRL)

Address 0x0018_0030 – Front End Control 2 SAR Control Register

Address 0x001B_0030 – Front End Control 1 SAR Control Register

Address 0x001E_0030 – Front End Control 0 SAR Control Register

Figure 4-184. SAR Control Register (SARCTRL)

31	24
EADC_WINDOW_2	
R/W-0010 1000	
23	16
EADC_WINDOW_1	
R/W-0110 0000	
15	8
SAR_RANGE	
R/W-0000 0000	

7	2	1	0
Reserved		SAR_RESOLUTION	
R-0000 00		R/W-00	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-184. SAR Control Register (SARCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	EADC_WINDOW_2	R/W	0010 1000	Configures acceptable range of error values to transition to AFE Gain of 2 during SAR process
23-16	EADC_WINDOW_1	R/W	0110 0000	Configures acceptable range of error values to transition to AFE Gain of 1 during SAR process
15-8	SAR_RANGE	R/W	0000 0000	Configures acceptable range of error values before declaring SAR completion
7-2	Reserved	R	0000 00	
1-0	SAR_ RESOLUTION	R/W	00	Configures the final resolution for SAR Conversions 0 = 8mV Resolution, 1x AFE Gain 1 = 4mV Resolution, 2x AFE Gain 2 = 2mV Resolution, 4x AFE Gain 3 = 1mV Resolution, 8x AFE Gain

4.10.12 SAR Timing Register (SARTIMING)

Address 0x0018_0034 – Front End Control 2 SAR Timing Register

Address 0x001B_0034– Front End Control 1 SAR Timing Register

Address 0x001E_0034 – Front End Control 0 SAR Timing Register

Figure 4-185. SAR Timing Register (SARTIMING)

10							8
SAR_TIMING_UPPER							
R/W-100							
7	6	5	4	3	2	1	0
Reserved	SAR_TIMING_MID			Reserved	SAR_TIMING_LOWER		
R-0	R/W-011			R-0	R/W-010		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-185. SAR Timing Register (SARTIMING) Register Field Descriptions

Bit	Field	Type	Reset	Description
10-8	SAR_TIMING _UPPER	R/W	100	Configures timing for Bits 9:8 of DAC setpoint for SAR Algorithm
7	Reserved	R	0	
6-4	SAR_TIMING_MID	R/W	011	Configures timing for Bits 7:6 of DAC setpoint for SAR Algorithm
3	Reserved	R	0	
2-0	SAR_TIMING _LOWER	R/W	010	Configures timing for Bits 5:0 of DAC setpoint for SAR Algorithm

4.10.13 EADC Value Register (EADCVALUE)

Address 0x0018_0038 – Front End Control 2 EADC Value Register

Address 0x001B_0038 – Front End Control 1 EADC Value Register

Address 0x001E_0038 – Front End Control 0 EADC Value Register

Figure 4-186. EADC Value Register (EADCVALUE)

25															16
ABS_VALUE															
R-0															
15	14	13												9	8
EADC_SAT_HIGH	EADC_SAT_LOW	Reserved													ERROR_VALUE
R-0	R-0	R-0													R-0
7															0
ERROR_VALUE															
R-0															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-186. EADC Value Register (EADCVALUE) Register Field Descriptions

Bit	Field	Type	Reset	Description
25-16	ABS_VALUE	R	0	10-bit Absolute Value calculated by Front End Control Module with a resolution of 1.5625mV/bit
15	EADC_SAT_HIGH	R	0	EADC Saturation High Indicator 0 = EADC output is not saturated at high limit 1 = EADC output is saturated at high limit
14	EADC_SAT_LOW	R	0	EADC Saturation Low Indicator 0 = EADC output is not saturated at low limit 1 = EADC output is saturated at low limit
13-9	Reserved	R	00 000	
8-0	ERROR_VALUE	R	0	Signed 9-bit Error value measured by Front End Control Module with a resolution of 1mV/bit

4.10.14 EADC Raw Value Register (EADCRAWVALUE)

Address 0x0018_003C – Front End Control 2 EADC Raw Value Register

Address 0x001B_003C – Front End Control 1 EADC Raw Value Register

Address 0x001E_003C – Front End Control 0 EADC Raw Value Register

Figure 4-187. EADC Raw Value Register (EADCRAWVALUE)

8	0
RAW_ERROR_VALUE	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-187. EADC Raw Value Register (EADCRAWVALUE) Register Field Descriptions

Bit	Field	Type	Reset	Description
8-0	RAW_ERROR _VALUE	R	0	Signed 9-bit Error value measured by Front End Control Module with a resolution of 1mV/bit. Value is raw EADC data before averaging.

4.10.15 DAC Status Register (DACSTAT)

Address 0x0018_0040 – Front End Control 2 DAC Status Register

Address 0x001B_0040 – Front End Control 1 DAC Status Register

Address 0x001E_0040 – Front End Control 0 DAC Status Register

Figure 4-188. DAC Status Register (DACSTAT)

9									0
DAC_VALUE									
R-00 0000 0000									

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-188. DAC Status Register (DACSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
9-0	DAC_VALUE	R	00 0000 0000	Current 10-bit Value sent to DAC

4.11 Miscellaneous Analog Control Registers

4.11.1 Clock Trim Register (CLKTRIM)

Address FFF7F000

Figure 4-189. Clock Trim Register (CLKTRIM)

16	15	0
RESET_DISABLE	Reserved	
R/W-0	R-X	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-189. Clock Trim Register (CLKTRIM) Register Field Descriptions

Bit	Field	Type	Reset	Description
16	RESET_DISABLE	R/W	0	Firmware disable of RESET pin
15-0	Reserved	R	X	The Reserved section in CLKTRIM is not reset to zero. It is set with trim values that are custom for each chip. They must be left in their existing state or the clock speed will be inaccurate.

4.11.2 Package ID Register (PKGID)

Address FFF7F010

Figure 4-190. Package ID Register (PKGID)

1	0
PKG_ID	
R/W-00	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-190. Package ID Register (PKGID) Register Field Descriptions

Bit	Field	Type	Reset	Description
1-0	PKG_ID	R/W	00	Represents package type of device 0 = 80-pin package (Default) 1 = Not used currently. Reserved for future expansion.

4.11.3 Brownout Register (BROWNOUT)

Address FFF7F014

Figure 4-191. Brownout Register (BROWNOUT)

2	1	0
INT	INT_EN	COMP_EN
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-191. Brownout Register (BROWNOUT) Register Field Descriptions

Bit	Field	Type	Reset	Description
2	INT	R	0	Brownout Interrupt Status 0 = No Brownout Condition observed 1 = Brownout Condition observed
1	INT_EN	R/W	0	Brownout Interrupt Enable 0 = Brownout Interrupt disabled (Default) 1 = Brownout Interrupt enabled
0	COMP_EN	R/W	0	Brownout Comparator Enable 0 = Brownout comparator logic disabled (Default) 1 = Brownout comparator logic enabled

4.11.4 Global I/O EN Register (GLBIOEN)

Address FFF7F018

Figure 4-192. Global I/O EN Register (GLBIOEN)

31	0
GLOBAL_IO_EN	

R/W-0000 0000 0000 0000 0000 0000 0000 0000

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-192. Global I/O EN Register (GLBIOEN) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GLOBAL_IO_EN	R/W	0000 0000 0000 0000 0000 0000 0000 0000	This register enables the global control of digital I/O pins 0 = Control of IO is done by the functional block assigned to the IO (Default) 1 = Control of IO is done by Global IO registers. Bit assignment is done by the following table:

BIT	PIN_NAME
31	TMR_PWM2_IO_EN
30	TMR_PWM3_IO_EN
29	FAULT3_IO_EN
28	ADC_EXT_TRIG_IO_EN
27	TCK_IO_EN
26	TDO_IO_EN
25	TMS_IO_EN
24	TDI_IO_EN
23	SCI_TX1_IO_EN
22	SCI_TX0_IO_EN
21	SCI_RX1_IO_EN
20	SCI_RX0_IO_EN
19	TMR_CAP0_IO_EN
18	TMR_PWM1_IO_EN
17	TMR_PWM0_IO_EN
16	TMR_CAP1_IO_EN
15	I2C_DATA_IO_EN
14	CONTROL_IO_EN
13	ALERT_IO_EN
12	EXT_INT_IO_EN
11	FAULT2_IO_EN
10	FAULT1_IO_EN
9	FAULT0_IO_EN
8	SYNC_IO_EN
7	DPWM3B_IO_EN
6	DPWM3A_IO_EN
5	DPWM2B_IO_EN
4	DPWM2A_IO_EN
3	DPWM1B_IO_EN
2	DPWM1A_IO_EN
1	DPWM0B_IO_EN

BIT	PIN_NAME
0	DPWM0A_IO_EN

4.11.5 Global I/O OE Register (GLBIOOE)

Address FFF7F01C

Figure 4-193. Global I/O OE Register (GLBIOOE)

31	0
GLOBAL_IO_OE	
R/W-0000 0000 0000 0000 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-193. Global I/O OE Register (GLBIOOE) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GLOBAL_IO_OE	R/W	0000 0000 0000 0000 0000 0000 0000 0000	This register controls the output enable signals for all digital I/O pins 0 = Input (Default) 1 = Output Bit assignment is done by the following table:

BIT	PIN_NAME
31	TMR_PWM2_IO_OE
30	TMR_PWM3_IO_OE
29	FAULT3_IO_OE
28	ADC_EXT_TRIG_IO_OE
27	TCK_IO_OE
26	TDO_IO_OE
25	TMS_IO_OE
24	TDI_IO_OE
23	SCI_TX1_IO_OE
22	SCI_TX0_IO_OE
21	SCI_RX1_IO_OE
20	SCI_RX0_IO_OE
19	TMR_CAP0_IO_OE
18	TMR_PWM1_IO_OE
17	TMR_PWM0_IO_OE
16	TMR_CAP1_IO_OE
15	I2C_DATA_IO_OE
14	CONTROL_IO_OE
13	ALERT_IO_OE
12	EXT_INT_IO_OE
11	FAULT2_IO_OE
10	FAULT1_IO_OE
9	FAULT0_IO_OE
8	SYNC_IO_OE
7	DPWM3B_IO_OE
6	DPWM3A_IO_OE
5	DPWM2B_IO_OE
4	DPWM2A_IO_OE
3	DPWM1B_IO_OE
2	DPWM1A_IO_OE
1	DPWM0B_IO_OE

BIT	PIN_NAME
0	DPWM0A_IO_OE

4.11.6 Global I/O Open Drain Control Register (GLBIOOD)

Address FFF7F020

Figure 4-194. Global I/O Open Drain Control Register (GLBIOOD)

31	0
GLOBAL_IO_OD	
R/W-0000 0000 0000 0000 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-194. Global I/O Open Drain Control Register (GLBIOOD) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GLOBAL_IO_OD	R/W	0000 0000 0000 0000 0000 0000 0000 0000	This register controls if the global IO is configured as an open drain. This bit multiplexes the GLOBAL_IO_VALUE register to the OE signals 0 = Normal I/O (Default) 1 = Open Drain Bit assignment is done by the following table:

BIT	PIN_NAME
31	TMR_PWM2_IO_OD
30	TMR_PWM3_IO_OD
29	FAULT3_IO_OD
28	ADC_EXT_TRIG_IO_OD
27	TCK_IO_OD
26	TDO_IO_OD
25	TMS_IO_OD
24	TDI_IO_OD
23	SCI_TX1_IO_OD
22	SCI_TX0_IO_OD
21	SCI_RX1_IO_OD
20	SCI_RX0_IO_OD
19	TMR_CAP0_IO_OD
18	TMR_PWM1_IO_OD
17	TMR_PWM0_IO_OD
16	TMR_CAP1_IO_OD
15	I2C_DATA_IO_OD
14	CONTROL_IO_OD
13	ALERT_IO_OD
12	EXT_INT_IO_OD
11	FAULT2_IO_OD
10	FAULT1_IO_OD
9	FAULT0_IO_OD
8	SYNC_IO_OD
7	DPWM3B_IO_OD
6	DPWM3A_IO_OD
5	DPWM2B_IO_OD
4	DPWM2A_IO_OD
3	DPWM1B_IO_OD
2	DPWM1A_IO_OD
1	DPWM0B_IO_OD

BIT	PIN_NAME
0	DPWM0A_IO_OD

4.11.7 Global I/O Value Register (GLBIOVAL)

Address FFF7F024

Figure 4-195. Global I/O Value Register (GLBIOVAL)

31	0
GLOBAL_IO_VALUE	
R/W-0000 0000 0000 0000 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-195. Global I/O Value Register (GLBIOVAL) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GLOBAL_IO_VALUE	R/W	0000 0000 0000 0000 0000 0000 0000 0000	This register set the output value of the digital I/O pins when configured as outputs 0 = Digital I/O pin configured as low in output mode (Default) 1 = Digital I/O pin configured as high in output mode Bit assignment is done by the following table:

BIT	PIN_NAME
31	TMR_PWM2_IO_VALUE
30	TMR_PWM3_IO_VALUE
29	FAULT3_IO_VALUE
28	ADC_EXT_TRIG_IO_VALUE
27	TCK_IO_VALUE
26	TDO_IO_VALUE
25	TMS_IO_VALUE
24	TDI_IO_VALUE
23	SCI_TX1_IO_VALUE
22	SCI_TX0_IO_VALUE
21	SCI_RX1_IO_VALUE
20	SCI_RX0_IO_VALUE
19	TMR_CAP0_IO_VALUE
18	TMR_PWM1_IO_VALUE
17	TMR_PWM0_IO_VALUE
16	TMR_CAP1_IO_VALUE
15	I2C_DATA_IO_VALUE
14	CONTROL_IO_VALUE
13	ALERT_IO_VALUE
12	EXT_INT_IO_VALUE
11	FAULT2_IO_VALUE
10	FAULT1_IO_VALUE
9	FAULT0_IO_VALUE
8	SYNC_IO_VALUE
7	DPWM3B_IO_VALUE
6	DPWM3A_IO_VALUE
5	DPWM2B_IO_VALUE
4	DPWM2A_IO_VALUE
3	DPWM1B_IO_VALUE
2	DPWM1A_IO_VALUE
1	DPWM0B_IO_VALUE

BIT	PIN_NAME
0	DPWM0A_IO_VALUE

4.11.8 Global I/O Read Register (GLBIOREAD)

Address FFF7F028

Figure 4-196. Global I/O Read Register (GLBIOREAD)

31	0
GLOBAL_IO_READ	
R-X	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-196. Global I/O Read Register (GLBIOREAD) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GLOBAL_IO_READ	R	X	This register provides the value on these signals after I/O muxing 0 = Digital I/O pin low (Default) 1 = Digital I/O pin high Bit assignment is done by the following table:

BIT	PIN_NAME
31	TMR_PWM2_IO_READ
30	TMR_PWM3_IO_READ
29	FAULT3_IO_READ
28	ADC_EXT_TRIG_IO_READ
27	TCK_IO_READ
26	TDO_IO_READ
25	TMS_IO_READ
24	TDI_IO_READ
23	SCI_TX1_IO_READ
22	SCI_TX0_IO_READ
21	SCI_RX1_IO_READ
20	SCI_RX0_IO_READ
19	TMR_CAP0_IO_READ
18	TMR_PWM1_IO_READ
17	TMR_PWM0_IO_READ
16	TMR_CAP1_IO_READ
15	I2C_DATA_IO_READ
14	CONTROL_IO_READ
13	ALERT_IO_READ
12	EXT_INT_IO_READ
11	FAULT2_IO_READ
10	FAULT1_IO_READ
9	FAULT0_IO_READ
8	SYNC_IO_READ
7	DPWM3B_IO_READ
6	DPWM3A_IO_READ
5	DPWM2B_IO_READ
4	DPWM2A_IO_READ
3	DPWM1B_IO_READ
2	DPWM1A_IO_READ
1	DPWM0B_IO_READ
0	DPWM0A_IO_READ

4.11.9 I/O Mux Control Register (IOMUX)

Address FFF7F030

Figure 4-197. I/O Mux Control Register (IOMUX)

9	8	7	6	5	4	3	2	1	0
TPWM0_MUX_SEL	Reserved	TCAP1_MUX_SEL		TCAP0_MUX_SEL		Reserved	JTAG_MUX_SEL	RTC_CLK_IN_SEL	RTC_CLK_OUT_SEL
R/W-0	R-0	R/W-0		R/W-0		R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-197. I/O Mux Control Register (IOMUX) Register Field Descriptions

Bit	Field	Type	Reset	Description
9	TPWM0_MUX_SEL	R/W	0	Pin Mux Select 0 = TMR_PWM_0 via the TMR_PWM_0 (Default) 1 = SYNC via the TMR_PWM_0
8	Reserved	R	0	
7-6	TCAP1_MUX_SEL	R/W	0	Pin Mux Select 0 = MR_CAP_1 function utilized via the TMR_CAP_1 pin (Default) 1 = MR_CAP_1 function utilized via the TDI pin 2 = MR_CAP_1 function utilized via the TDO pin 3 = MR_CAP_1 function utilized via the TMR_CAP_0 pin
5-4	TCAP0_MUX_SEL	R/W	0	Pin Mux Select 0 = MR_CAP_0 via the TMR_CAP_0 (Default) 1 = MR_CAP_0 via the TDI 2 = TMR_CAP_0 via the TDO 3 = MR_CAP_0 via the TMR_CAP_1
3	Reserved	R	0	
2	JTAG_MUX_SEL	R/W	0	Pin Mux Select 0 = JTAG pins function as JTAG port. TCK/TMS/TDI/TDO 1 = JTAG pins disabled JTAG port functions as SPI port in this mode. TCK -> SPI_CLK TMS -> SPI_CS TDI -> SPI_MISO TDO -> SPI_MOSI (default) Note: This bit is left set at reset if the pflash checksum is valid to disable JTAG for flash code protection. If code protection is desired, and SPI is also desired, it should be left set, and the JTAG pins should be used for SPI. If the pflash checksum is not valid, the bit is cleared to permit JTAG use.] JTAG can also be disabled by the other IOMUX bits which affect the JTAG pins instead. Setting 2 bits which affect the same pin will have unpredictable results.
1	RTC_CLK_IN_SEL	R/W	0	Pin Mux Select 0 = Input to RTC module clock connected to XTAL_CLK_IN (default) 1 = Input to RTC module clock connected to TCK
0	RTC_CLK_OUT_SEL	R/W	0	Pin Mux Select 0 = Output of RTC reference clock disabled (default) 1 = Output of RTC reference clock connected to TCK

4.11.10 Current Sharing Control Register (CSCTRL)

Address FFF7F038

Figure 4-198. Current Sharing Control Register (CSCTRL)

23 16	15 8	7 4	3 0
DPWM_DUTY	DPWM_PERIOD	Reserved	TEST_MODE
R/W-0000 0000	R/W-0000 0000	R-0000	R/W-0000

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-198. Current Sharing Control Register (CSCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-16	DPWM_DUTY	R/W	0000 0000	Configures Pulse Width/Duty Cycle for DPWM output to Current Sharing circuit. Resolution of LSB equals period of MCLK clock (32 ns).
15-8	DPWM_PERIOD	R/W	0000 0000	Configures Period for DPWM output to Current Sharing circuit. Output period equals DPWM_PERIOD+1 * LSB resolution. Resolution of LSB equals period of MCLK clock
7-4	Reserved	R/W	0000	
3-0	TEST_MODE	R/W	0000	Controls Current Sharing Operation

Table 4-199.

Current Sharing Mode	CSCTRL.bit.TEST_MODE	Switch θ1	Switch θ2	Digital-PWM
Tri-state or Slave mode	0	OFF	OFF	OFF
PWM average current Bus	1	ON	OFF	ACTIVE
Analog average current Bus or Master mode	3	OFF	ON	OFF

4.11.11 Temperature Reference Register (TEMPREF)

Address FFF7F03C

Figure 4-199. Temperature Reference Register (TEMPREF)

11	0
TEMP_REF	
R/W-0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-200. Temperature Reference Register (TEMPREF) Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	TEMP_REF	R/W	0000 0000 0000	Reference measurement taken during factory trim, ADC12 measurement of the internal temperature sensor at room temperature for use in offset calibration

4.11.12 Power Disable Control Register (PWRDISCTRL)

Address FFF7F040

Figure 4-200. Power Disable Control Register (PWRDISCTRL)

22	21	20	19	18	17	16
DTC_CLK_EN	Reserved	RTC_CLK_EN	I2C_CLK_EN	SPI_CLK_EN	PCM_CLK_EN	CPCC_CLK_EN
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
15	14	13	12	11	10	9	8
FILTER2_CLK_EN	FILTER1_CLK_EN	FILTER0_CLK_EN	FE_CTRL2_CLK_EN	FE_CTRL1_CLK_EN	FE_CTRL0_CLK_EN	DPWM3_CLK_EN	DPWM2_CLK_EN
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
7	6	5	4	3	2	1	0
DPWM1_CLK_EN	DPWM0_CLK_EN	SCI1_CLK_EN	SCI0_CLK_EN	ADC12_CLK_EN	PMBUS_CLK_EN	GIO_CLK_EN	TIMER_CLK_EN
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-201. Power Disable Control Register (PWRDISCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
22	DTC_CLK_EN	R/W	1	Clock Enable for DTC Module 0 = Disables clocks to DTC Module 1 = Enables clocks to DTC Module (Default)
21	Reserved	R/W	1	
20	RTC_CLK_EN	R/W	1	Clock Enable for RTC Module 0 = Disables clocks to RTC Module 1 = Enables clocks to RTC Module (Default)
19	I2C_CLK_EN	R/W	1	Clock Enable for I2C Module 0 = Disables clocks to I2C Module 1 = Enables clocks to I2C Module (Default)
18	SPI_CLK_EN	R/W	1	Clock Enable for SPI Module 0 = Disables clocks to SPI Module 1 = Enables clocks to SPI Module (Default)
17	PCM_CLK_EN	R/W	1	Clock Enable for Digital Peak Current Control Module 0 = Disables clocks to Digital Peak Current Control Module 1 = Enables clocks to Digital Peak Current Control Module (Default)
16	CPCC_CLK_EN	R/W	1	Clock Enable for Constant Power/Constant Current Module 0 = Disables clocks to Constant Power/Constant Current Module 1 = Enables clocks to Constant Power/Constant Current Module (Default)
15	FILTER2_CLK_EN	R/W	1	Clock Enable for Filter 2 Module 0 = Disables clocks to Filter 2 Module 1 = Enables clocks to Filter 2 Module (Default)
14	FILTER1_CLK_EN	R/W	1	Clock Enable for Filter 1 Module 0 = Disables clocks to Filter 1 Module 1 = Enables clocks to Filter 1 Module (Default)
13	FILTER0_CLK_EN	R/W	1	Clock Enable for Filter 0 Module 0 = Disables clocks to Filter 0 Module 1 = Enables clocks to Filter 0 Module (Default)
12	FE_CTRL2_CLK_EN	R/W	1	Clock Enable for Front End Control 2 Module 0 = Disables clocks to Front End Control 2 Module 1 = Enables clocks to Front End Control 2 Module (Default)

Table 4-201. Power Disable Control Register (PWRDISCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	FE_CTRL1_CLK_EN	R/W	1	Clock Enable for Front End Control 1 Module 0 = Disables clocks to Front End Control 1 Module 1 = Enables clocks to Front End Control 1 Module (Default)
10	FE_CTRL0_CLK_EN	R/W	1	Clock Enable for Front End Control 0 Module 0 = Disables clocks to Front End Control 0 Module 1 = Enables clocks to Front End Control 0 Module (Default)
9	DPWM3_CLK_EN	R/W	1	Clock Enable for DPWM 3 Module 0 = Disables clocks to DPWM 3 Module 1 = Enables clocks to DPWM 3 Module (Default)
8	DPWM2_CLK_EN	R/W	1	Clock Enable for DPWM 2 Module 0 = Disables clocks to DPWM 2 Module 1 = Enables clocks to DPWM 2 Module (Default)
7	DPWM1_CLK_EN	R/W	1	Clock Enable for DPWM 1 Module 0 = Disables clocks to DPWM 1 Module 1 = Enables clocks to DPWM 1 Module (Default)
6	DPWM0_CLK_EN	R/W	1	Clock Enable for SCI/UART 1 Module 0 = Disables clocks to SCI/UART 1 Module 1 = Enables clocks to SCI/UART 1 Module (Default)
5	SCI1_CLK_EN	R/W	1	Clock Enable for SCI/UART 1 Module 0 = Disables clocks to SCI/UART 1 Module 1 = Enables clocks to SCI/UART 1 Module (Default)
4	SCI0_CLK_EN	R/W	1	Clock Enable for SCI/UART 0 Module 0 = Disables clocks to SCI/UART 0 Module 1 = Enables clocks to SCI/UART 0 Module (Default)
3	ADC12_CLK_EN	R/W	1	Clock Enable for ADC12 Control Module 0 = Disables clocks to ADC12 Control Module 1 = Enables clocks to ADC12 Control Module (Default)
2	PMBUS_CLK_EN	R/W	1	Clock Enable for PMBus Interface Module 0 = Disables clocks to PMBus Interface Module 1 = Enables clocks to PMBus Interface Module (Default)
1	GIO_CLK_EN	R/W	1	Clock Enable for GIO Module 0 = Disables clocks to GIO Module 1 = Enables clocks to GIO Module (Default)
0	TIMER_CLK_EN	R/W	1	Clock Enable for Timer Module 0 = Disables clocks to Timer Module 1 = Enables clocks to Timer Module (Default)

4.11.13 DTC UART Pin Mux Select Register (DTCUARTSEL)

Address FFF7F048

Figure 4-201. DTC UART Pin Mux Select Register (DTCUARTSEL)

1	0
UART1_RX_SEL	UART0_RX_SEL
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-202. DTC UART Pin Mux Select Register (DTCUARTSEL) Register Field Descriptions

Bit	Field	Type	Reset	Description
1	UART1_RX_SEL	R/W	0	UART 1 RX Mux 0 = UART 1 RX input from UART 1 RX pin 1 = UART 1 RX input from UART 0 RX pin
0	UART0_RX_SEL	R/W	0	UART 0 RX Mux 0 = UART 0 RX input from UART 0 RX pin 1 = UART 0 RX input from UART 1 RX pin

4.11.14 LFO Clock Select Register (LFOCLKSEL)

Address FFF7F050

Figure 4-202. LFO Clock Select Register (LFOCLKSEL)

3	2	1	0
WD_VLK_SEL	RTC_CLK_CEL	Reserved	
R/W-0	R/W-0	R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-203. LFO Clock Select Register (LFOCLKSEL) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	WD_VLK_SEL	R/W	0	WD CLK SEL MUX 0 = WD module operates off LFO CLK 1 = WD module operates off XTAL CLK
2	RTC_CLK_CEL	R/W	0	RTC CLK SEL MUX 0 = RTC module operates off (XTAL or TCK pin CLK) (Recommended for high accuracy applications) 1 = RTC module operates off LFO CLK
1-0	Reserved	R	0	

4.12 PMBus Interface Registers Reference

4.12.1 PMBUS Control Register 1 (PMBCTRL1)

PMBusRegs - Address FFF7F600

PMBusRegs1 - Address FFF7F700

Figure 4-203. PMBUS Control Register 1 (PMBCTRL1)

20	19	18	17	16
PRC_CALL	GRP_CMD	PEC_ENA	EXT_CMD	CMD_ENA
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTE_COUNT								SLAVE_ADDR							RW
R/W-0000 0000								R/W-000 0000							R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-204. PMBUS Control Register 1 (PMBCTRL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
20	PRC_CALL	R/W	0	Master Process Call Message Enable 0 = Default state for all messages besides Process Call message (Default) 1 = Enables transmission of Process Call message
19	GRP_CMD	R/W	0	Master Group Command Message Enable 0 = Default state for all messages besides Group Command message (Default) 1 = Enables transmission of Group Command message
18	PEC_ENA	R/W	0	Master PEC Processing Enable 0 = Disables PEC processing (Default) 1 = Enables PEC byte transmission/reception
17	EXT_CMD	R/W	0	Master Extended Command Code Enable 0 = Use 1 byte for Command Code (Default) 1 = Use 2 bytes for Command Code
16	CMD_ENA	R/W	0	Master Command Code Enable 0 = Disables use of command code on Master initiated messages (Default) 1 = Enables use of command code on Master initiated messages
15-8	BYTE_COUNT	R/W	0000 0000	Indicates number of data bytes transmitted in current message. Byte count does not include any device addresses, command words or block lengths in block messages. In block messages, the PMBus Interface automatically inserts the block length into the message based on the byte count setting. The firmware only needs to load the address, command words and data to be transmitted. PMBus Interface supports byte writes up to 255 bytes.
7-1	SLAVE_ADDR	R/W	000 0000	Specifies the address of the slave to which the current message is directed towards.
0	RW	R/W	0	Indicates if current Master initiated message is read operation or write operation. 0 = Message is a write transaction (data from Master to Slave) (Default) 1 = Message is a read transaction (data from Slave to Master)

4.12.2 PMBus Transmit Data Buffer (PMBTXBUF)

PMBusRegs - Address FFF7F604

PMBusRegs1 - Address FFF7F704

Figure 4-204. PMBus Transmit Data Buffer (PMBTXBUF)

31 24	23 16	15 8	7 0
BYTE3	BYTE2	BYTE1	BYTE0
R/W-0000 0000	R/W-0000 0000	R/W-0000 0000	R/W-0000 0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-205. PMBus Transmit Data Buffer (PMBTXBUF) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BYTE3	R/W	0000 0000	Last data byte transmitted from Transmit Data Buffer
23-16	BYTE2	R/W	0000 0000	Third data byte transmitted from Transmit Data Buffer
15-8	BYTE1	R/W	0000 0000	Second data byte transmitted from Transmit Data Buffer
7-0	BYTE0	R/W	0000 0000	First data byte transmitted from Transmit Data Buffer

4.12.3 PMBus Receive Data Register (PMBRXBUF)

PMBusRegs - Address FFF7F608

PMBusRegs1 - Address FFF7F708

Figure 4-205. PMBus Receive Data Register (PMBRXBUF)

31 24	23 16	15 8	7 0
BYTE3	BYTE2	BYTE1	BYTE0
R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-206. PMBus Receive Data Register (PMBRXBUF) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BYTE3	R	0	Last data byte received in Receive Data Buffer
23-16	BYTE2	R	0	Third data byte received in Receive Data Buffer
15-8	BYTE1	R	0	Second data byte received in Receive Data Buffer
7-0	BYTE0	R	0	First data byte received in Receive Data Buffer

4.12.4 PMBus Acknowledge Register (PMBACK)

PMBusRegs - Address FFF7F60C

PMBusRegs1 - Address FFF7F70C

Figure 4-206. PMBus Acknowledge Register (PMBACK)

0
ACK
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-207. PMBus Acknowledge Register (PMBACK) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	ACL	R/W	0	Allows firmware to acknowledge or not acknowledge received data 0 = NACK received data (Default) 1 = Acknowledge received data, bit clears upon issue of ACK on PMBus

4.12.5 PMBus Status Register (PMBST)

PMBusRegs - Address FFF7F610

PMBusRegs1 - Address FFF7F710

Figure 4-207. PMBus Status Register (PMBST)

21	20	19	18	17	16
SCL_RAW	SDA_RAW	CONTROL_RAW	ALERT_RAW	CONTROL_EDGE	ALERT_EDGE
R-0	R-0	R-0	R-0	R-0	R-0

15	14	13	12	11	10	9	8
MASTER	LOST_ARB	BUS_FREE	UNIT_BUSY	RPT_START	SLAVE_ADDR _READY	CLK_HIGH_ TIMEOUT	CLK_LOW_ TIMEOUT
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
PEC_VALID	NACK	EOM	DATA_ REQUEST	DATA_READY	RD_BYTE_COUNT		
R-0	R-0	R-0	R-0	R-0	R-0		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-208. PMBus Status Register (PMBST) Register Field Descriptions

Bit	Field	Type	Reset	Description
21	SCL_RAW	R	0	PMBus Clock Pin Real Time Status 0 = PMBus clock pin observed at logic level low 1 = PMBus clock pin observed at logic level high
20	SDA_RAW	R	0	PMBus Data Pin Real Time Status 0 = PMBus data pin observed at logic level low 1 = PMBus data pin observed at logic level high
19	CONTROL_RAW	R	0	Control Pin Real Time Status 0 = Control pin observed at logic level low 1 = Control pin observed at logic level high Note: CONTROL_RAW bit is not active for PMBusRegs1.
18	ALERT_RAW	R	0	Alert Pin Real Time Status 0 = Alert pin observed at logic level low 1 = Alert pin observed at logic level high Note: ALERT_RAW bit is not active for PMBusRegs1.
17	CONTROL_EDGE	R	0	Control Edge Detection Status 0 = Control pin has not transitioned 1 = Control pin has been asserted by another device on PMBus Note: CONTROL_EDGE bit is not active for PMBusRegs1.
16	ALERT_EDGE	R	0	Alert Edge Detection Status 0 = Alert pin has not transitioned 1 = Alert pin has been asserted by another device on PMBus
15	MASTER	R	0	Master Indicator 0 = PMBus Interface in Slave Mode or Idle Mode 1 = PMBus Interface in Master Mode
14	LOST_ARB	R	0	Lost Arbitration Flag 0 = Master has attained control of PMBus 1 = Master has lost arbitration and control of PMBus
13	BUS_FREE	R	0	PMBus Free Indicator 0 = PMBus processing current message 1 = PMBus available for new message

Table 4-208. PMBus Status Register (PMBST) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	UNIT_BUSY	R	0	PMBus Busy Indicator 0 = PMBus Interface is idle, ready to transmit/receive message 1 = PMBus Interface is busy, processing current message
11	RPT_START	R	0	Repeated Start Flag 0 = No Repeated Start received by interface 1 = Repeated Start condition received by interface
10	SLAVE_ADDR_ READY	R	0	Slave Address Ready 0 = Indicates no slave address is available for reading 1 = Slave address ready to be read from Receive Data Register (Bits 6:0)
9	CLK_HIGH_ TIMEOUT	R	0	Clock High Detection Status 0 = No Clock High condition detected 1 = Clock High exceeded 50us during message
8	CLK_LOW_ TIMEOUT	R	0	Clock Low Timeout Status 0 = No clock low timeout detected 1 = Clock low timeout detected, clock held low for greater than 35ms
7	PEC_VALID	R	0	PEC Valid Indicator 0 = Received PEC not valid (if EOM is asserted) 1 = Received PEC is valid
6	NACK	R	0	Not Acknowledge Flag Status 0 = Data transmitted has been accepted by receiver 1 = Receiver has not accepted transmitted data
5	EOM	R	0	End of Message Indicator 0 = Message still in progress or PMBus in idle state. 1 = End of current message detected
4	DATA_REQUEST	R	0	Data Request Flag 0 = No data needed by PMBus Interface 1 = PMBus Interface request additional data. PMBus clock stretching enabled to stall bus until firmware provides transmit data.
3	DATA_READY	R	0	Data Ready Flag 0 = No data available for reading by processor 1 = PMBus Interface read buffer full, firmware required to read data prior to further bus activity. PMBus clock stretching enabled to stall bus until data is read by firmware.
2-0	RD_BYTE_ COUNT	R	0	Number of Data Bytes available in Receive Data Register 0 = No received data 1 = 1 byte received. Data located in Receive Data Register, Bits 7-0 2 = 2 bytes received. Data located in Receive Data Register, Bits 15-0 3 = 3 bytes received. Data located in Receive Data Register, Bits 23-0 4 = 4 bytes received. Data located in Receive Data Register, Bits 31-0

4.12.6 PMBus Interrupt Mask Register (PMBINTM)

PMBusRegs - Address FFF7F614

PMBusRegs1 - Address FFF7F714

Figure 4-208. PMBus Interrupt Mask Register (PMBINTM)

9	8	7	6	5	4	3	2	1	0
CLK_HIGH_DETECT	LOST_ARB	CONTROL	ALERT	EOM	SLAVE_ADDR_READY	DATA_REQUEST	DATA_READY	BUS_LOW_TIMEOUT	BUS_FREE
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-209. PMBus Interrupt Mask Register (PMBINTM) Register Field Descriptions

Bit	Field	Type	Reset	Description
9	CLK_HIGH_DETECT	R/W	1	Clock High Detection Interrupt Mask 0 = Generates interrupt if clock high exceeds 50us during message 1 = Disables interrupt generation for Clock High detection (Default)
8	LOST_ARB	R/W	1	Lost Arbitration Interrupt Mask 0 = Generates interrupt upon assertion of Lost Arbitration flag 1 = Disables interrupt generation upon assertion of Lost Arbitration flag (Default)
7	CONTROL	R/W	1	Control Detection Interrupt Mask 0 = Generates interrupt upon assertion of Control flag 1 = Disables interrupt generation upon assertion of Control flag (Default) Note: CONTROL bitis not active for PMBusRegs1.
6	ALERT	R/W	1	Alert Detection Interrupt Mask 0 = Generates interrupt upon assertion of Alert flag 1 = Disables interrupt generation upon assertion of Alert flag (Default) Note: ALERT bit is not active for PMBusRegs1.
5	EOM	R/W	1	End of Message Interrupt Mask 0 = Generates interrupt upon assertion of End of Message flag 1 = Disables interrupt generation upon assertion of End of Message flag (Default)
4	SLAVE_ADDR_READY	R/W	1	Slave Address Ready Interrupt Mask 0 = Generates interrupt upon assertion of Slave Address Ready flag 1 = Disables interrupt generation upon assertion of Slave Address Ready flag (Default)
3	DATA_REQUEST	R/W	1	Data Request Interrupt Mask 0 = Generates interrupt upon assertion of Data Request flag 1 = Disables interrupt generation upon assertion of Data Request flag (Default)
2	DATA_READY	R/W	1	Data Ready Interrupt Mask 0 = Generates interrupt upon assertion of Data Ready flag 1 = Disables interrupt generation upon assertion of Data Ready flag (Default)
1	BUS_LOW_TIMEOUT	R/W	1	Clock Low Timeout Interrupt Mask 0 = Generates interrupt upon assertion of Clock Low Timeout flag 1 = Disables interrupt generation upon assertion of Clock Low Timeout flag (Default)
0	BUS_FREE	R/W	1	Bus Free Interrupt Mask 0 = Generates interrupt upon assertion of Bus Free flag 1 = Disables interrupt generation upon assertion of Bus Free flag (Default)

4.12.7 PMBus Control Register 2 (PMBCTRL2)

PMBusRegs - Address FFF7618

PMBusRegs1 - Address FFF7718

Figure 4-209. PMBus Control Register 2 (PMBCTRL2)

30	29	23
SLAVE_ADDR_2_EN*	SLAVE_ADDR_2*	
R/W-0	R/W-110 0000	

22	21	20	19	18	16
RX_BYTE_ACK_CNT		MAN_CMD	TX_PEC	TX_COUNT	
R/W-11		R/W-0	R/W-0	R/W-000	

15	14	8	7	6	0
PEC_ENA	SLAVE_MASK		MAN_SLAVE_ACK	SLAVE_ADDR	
R/W-0	R/W-111 1111		R/W-0	R/W-111 1100	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-210. PMBus Control Register 2 (PMBCTRL2) Register Field Descriptions

Bit	Field	Type	Reset	Description
30	SLAVE_ADDR_2_EN*	R/W	0	Enable auto detection of the 2nd slave address. 0 = 2nd slave address disabled (default) 1 = 2nd slave address enabled *Only available on UCD3138A64 and UCD3138128 A and non-A versions
29-23	SLAVE_ADDR_2*	R/W	110 0000	Configures the second device address of the slave. Used in automatic slave address acknowledge mode (default mode). *Only available on UCD3138A64 and UCD3138128 A and non-A versions)
22-21	RX_BYTE_ACK_CNT	R/W	11	Configures number of data bytes to automatically acknowledge when receiving data in slave mode. 00 = 1 byte received by slave. Firmware is required to manually acknowledge every received byte. 01 = 2 bytes received by slave. Hardware automatically acknowledges the first received byte. Firmware is required to manually acknowledge after the second received byte. 10 = 3 bytes received by slave. Hardware automatically acknowledges the first 2 received bytes. Firmware is required to manually acknowledge after the third received byte. 11 = 4 bytes received by slave. Hardware automatically acknowledges the first 3 received bytes. Firmware is required to manually acknowledge after the fourth received byte (Default)
20	MAN_CMD	R/W	0	Manual Command Acknowledgement Mode 0 = Slave automatically acknowledges received command code (Default) 1 = Data Request flag generated after receipt of command code, firmware required to issue ACK to continue message
19	TX_PEC	R/W	0	Asserted when the slave needs to send a PEC byte at end of message. PMBus Interface will transmit the calculated PEC byte after transmitting the number of data bytes indicated by TX Byte Cnt(Bits 19:17). 0 = No PEC byte transmitted (Default) 1 = PEC byte transmitted at end of current message
18-16	TX_COUNT	R/W	000	Number of valid bytes in Transmit Data Register 0 = No bytes valid (Default) 1 = One byte valid, Byte #0 (Bits 7:0 of Receive Data Register) 2 = Two bytes valid, Bytes #0 and #1 (Bits 15:0 of Receive Data Register) 3 = Three bytes valid, Bytes #0-2 (Bits 23:0 of Receive Data Register) 4 = Four bytes valid, Bytes #0-3 (Bits 31:0 of Receive Data Register)

Table 4-210. PMBus Control Register 2 (PMBCTRL2) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PEC_ENA	R/W	0	PEC Processing Enable 0 = PEC processing disabled (Default) 1 = PEC processing enabled
14-8	SLAVE_MASK	R/W	111 1111	Used in address detection, the slave mask enables acknowledgement of multiple device addresses by the slave. Writing a '0' to a bit within the slave mask enables the corresponding bit in the slave address to be either '1' or '0' and still allow for a match. Writing a '0' to all bits in the mask enables the PMBus Interface to acknowledge any device address. Upon power-up, the slave mask defaults to 7Fh, indicating the slave will only acknowledge the address programmed into the Slave Address (Bits 6-0).
7	MAN_SLAVE _ACK	R/W	0	Manual Slave Address Acknowledgement Mode 0 = Slave automatically acknowledges device address specified in SLAVE_ADDR, Also uses SLAVE_ADDR_2 if present and enabled. (Default) 1 = Enables the Manual Slave Address Acknowledgement Mode. Firmware is required to read received address and acknowledge on every message
6-0	SLAVE_ADDR	R/W	111 1100	Configures the current device address of the slave. Used in automatic slave address acknowledge mode (default mode). The PMBus Interface will compare the received device address with the value stored in the Slave Address bits and the mask configured in the Slave Mask bits. If matching, the slave will acknowledge the device address.

4.12.8 PMBus Hold Slave Address Register (PMBHSA)

PMBusRegs - Address FFF7F61C

PMBusRegs1 - Address FFF7F71C

Figure 4-210. PMBus Hold Slave Address Register (PMBHSA)

7	6	5	4	3	2	1	0
SLAVE_ADDR							SLAVE_RW
R-0							R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-211. PMBus Hold Slave Address Register (PMBHSA) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ADDR	R	0	Stored device address acknowledged by the slave
0	SLAVE_RW	R	0	Stored R/W bit from address acknowledged by the slave 0 = Write Access 1 = Read Access

4.12.9 PMBus Control Register 3 (PMBCTRL3)

PMbusRegs - Address FFF7F620

PMbusRegs1 - Address FFF7F720

Figure 4-211. PMBus Control Register 3 (PMBCTRL3)

24	23
I2C_MODE_EN*	CLK_HIS_DIS* or CLK_HI_EN*
R/W-0	R/W-1 or R/W-0

22	21	20	19	18	17	16
MASTER_EN	SLAVE_EN	CLK_LO_DIS	IBIAS_B_EN	IBIAS_A_EN	SCL_DIR	SCL_VALUE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8
SCL_MODE	SDA_DIR	SDA_VALUE	SDA_MODE	CNTL_DIR	CNTL_VALUE	CNTL_MODE	ALERT_DIR
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
ALERT_VALUE	ALERT_MODE	CNTL_INT_EDGE	FAST_MODE_PLUS	FAST_MODE	BUS_LO_INT_EDGE	ALERT_EN	RESET
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-212. PMBus Control Register 3 (PMBCTRL3) Register Field Descriptions

Bit	Field	Type	Reset	Description
24	I2C_MODE_EN*	R/W	0	I2C Mode Enable – Utilized for Master mode only 0 = I2C Mode Disabled (Default) 1 = I2C Mode Enabled The only effect of I2C_MODE_EN is to remove the automatic insertion of number of bytes in block writes in master mode. *Only available on UCD3138A64 and UCD3138128 A and non-A versions
23	CLK_HI_DIS*	R/W	1	Clock High Timeout Disable 0 = Clock High Timeout Enabled 1 = Clock High Timeout Disabled (Default) *Only available on UCD3138A64 and UCD3138128 A and non-A versions
23	CLK_HI_EN*	R/W	0	Clock High Timeout Enable 0 = Clock High Timeout Disabled (Default) 1 = Clock High Timeout Enabled *Only available on UCD3138A and UCD3138064A
22	MASTER_EN	R/W	0	PMBus Master Enable 0 = Disables PMBus Master capability (Default) 1 = Enables PMBus Master capability
21	SLAVE_EN	R/W	0	PMBus Slave Enable 0 = Disables PMBus Slave capability 1 = Enables PMBus Slave capability (Default)
20	CLK_LO_DIS	R/W	0	Clock Low Timeout Disable 0 = Clock Low Timeout Enabled (Default) 1 = Clock Low Timeout Disabled
19	IBIAS_B_EN	R/W	0	PMBus Current Source B Control 0 = Disables Current Source for PMBUS address detection thru ADC (Default) 1 = Enables Current Source for PMBUS address detection thru ADC
18	IBIAS_A_EN	R/W	0	PMBus Current Source A Control 0 = Disables Current Source for PMBUS address detection thru ADC (Default) 1 = Enables Current Source for PMBUS address detection thru ADC

Table 4-212. PMBus Control Register 3 (PMBCTRL3) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	SCL_DIR	R/W	0	Configures direction of PMBus clock pin in GPIO mode 0 = PMBus clock pin configured as output (Default) 1 = PMBus clock pin configured as input
16	SCL_VALUE	R/W	0	Configures output value of PMBus clock pin in GPIO Mode 0 = PMBus clock pin driven low in GPIO Mode (Default) 1 = PMBus clock pin driven high in GPIO Mode
15	SCL_MODE	R/W	0	Configures mode of PMBus Clock pin 0 = PMBus clock pin configured in functional mode (Default) 1 = PMBus clock pin configured as GPIO
14	SDA_DIR	R/W	0	Configures direction of PMBus data pin in GPIO mode 0 = PMBus data pin configured as output (Default) 1 = PMBus data pin configured as input
13	SDA_VALUE	R/W	0	Configures output value of PMBus data pin in GPIO Mode 0 = PMBus data pin driven low in GPIO Mode (Default) 1 = PMBus data pin driven high in GPIO Mode
12	SDA_MODE	R/W	0	Configures mode of PMBus Data pin 0 = PMBus data pin configured in functional mode (Default) 1 = PMBus data pin configured as GPIO
11	CNTL_DIR	R/W	0	Configures direction of Control pin in GPIO mode 0 = Control pin configured as output (Default) 1 = Control pin configured as input Note: CNTL_DIR bit is not active for PMBusRegs1.
10	CNTL_VALUE	R/W	0	Configures output value of Control pin in GPIO Mode 0 = Control pin driven low in GPIO Mode (Default) 1 = Control pin driven high in GPIO Mode Note: CNTL_VALUE bit is not active for PMBusRegs1.
9	CNTL_MODE	R/W	0	Configures mode of Control pin 0 = Control pin configured in functional mode (Default) 1 = Control pin configured as GPIO Note: CNTL_MODE bit is not active for PMBusRegs1.
8	ALERT_DIR	R/W	0	Configures direction of Alert pin in GPIO mode 0 = Control pin configured as output (Default) 1 = Control pin configured as input Note: ALERT_DIR bit is not active for PMBusRegs1.
7	ALERT_VALUE	R/W	0	Configures output value of Alert pin in GPIO Mode 0 = Alert pin driven low in GPIO Mode (Default) 1 = Alert pin driven high in GPIO Mode Note: ALERT_VALUE bit is not active for PMBusRegs1.
6	ALERT_MODE	R/W	0	Configures mode of Alert pin 0 = Alert pin configured in functional mode (Default) 1 = Aler3 pin configured as GPIO Note: ALERT_MODE bit is not active for PMBusRegs1.
5	CNTL_INT_EDGE	R/W	0	Control Interrupt Edge Select 0 = Interrupt generated on falling edge of Control (Default) 1 = Interrupt generated on rising edge of Control Note: CNTL_INT_EDGE bit is not active for PMBusRegs1.
4	FAST_MODE _PLUS	R/W	0	Fast Mode Plus Enable 0 = Standard 100 KHz mode enabled (Default) 1 = Fast Mode Plus enabled (1MHz operation on PMBus)

Table 4-212. PMBus Control Register 3 (PMBCTRL3) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	FAST_MODE	R/W	0	Fast Mode Enable 0 = Standard 100 KHz mode enabled (Default) 1 = Fast Mode enabled (400KHz operation on PMBus)
2	BUS_LO_INT _EDGE	R/W	0	Clock Low Timeout Interrupt Edge Select 0 = Interrupt generated on rising edge of clock low timeout (Default) 1 = Interrupt generated on falling edge of clock low timeout
1	ALERT_EN	R/W	0	Slave Alert Enable 0 = PMBus Alert is not driven by slave, pulled up high on PMBus (Default) 1 = PMBus Alert driven low by slave Note: ALERT_EN bit is not active for PMBusRegs1.
0	RESET	R/W	0	PMBus Interface Synchronous Reset 0 = No reset of internal state machines (Default) 1 = Control state machines are reset to initial states

4.13 4.13 GIO – General Purpose Input/Output Module

GIO Registers have the following attributes:

- Addresses placed on word boundaries
- Byte, Half-word and Word Writes are permitted
- All Registers can be read in any mode
- All Registers are writeable

4.13.1 Fault IO Direction Register (FAULTDIR)

Address FFF7FA00

Figure 4-212. Fault IO Direction Register (FAULTDIR)

3	2	1	0
FLT3_DIR	FLT2_DIR	FLT1_DIR	FLT0_DIR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-213. Fault IO Direction Register (FAULTDIR) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	FLT3_DIR	R/W	0	FAULT[3] Pin Configuration 0 = FAULT[3] pin configured as an input pin (Default) 1 = FAULT[3] pin configured as an output pin
2	FLT2_DIR	R/W	0	FAULT[2] Pin Configuration 0 = FAULT[2] pin configured as an input pin (Default) 1 = FAULT[2] pin configured as an output pin
1	FLT1_DIR	R/W	0	FAULT[1] Pin Configuration 0 = FAULT[1] pin configured as an input pin (Default) 1 = FAULT[1] pin configured as an output pin
0	FLT0_DIR	R/W	0	FAULT[0] Pin Configuration 0 = FAULT[0] pin configured as an input pin (Default) 1 = FAULT[0] pin configured as an output pin

4.13.2 Fault Input Register (FAULTIN)

Address FFF7FA04

Figure 4-213. Fault Input Register (FAULTIN)

3	2	1	0
FLT3_DIR	FLT2_DIR	FLT1_DIR	FLT0_DIR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-214. Fault Input Register (FAULTIN) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	FLT3_IN	R	0	Input Value of FAULT[3] Pin 0 = FAULT[3] pin driven low 1 = FAULT[3] pin driven high
2	FLT2_IN	R	0	Input Value of FAULT[2] Pin 0 = FAULT[2] pin driven low 1 = FAULT[2] pin driven high
1	FLT1_IN	R	0	Input Value of FAULT[1] Pin 0 = FAULT[1] pin driven low 1 = FAULT[1] pin driven high
0	FLT0_IN	R	0	Input Value of FAULT[0] Pin 0 = FAULT[0] pin driven low 1 = FAULT[0] pin driven high

4.13.3 Fault Output Register (FAULTOUT)

Address FFF7FA08

Figure 4-214. Fault Output Register (FAULTOUT)

3	2	1	0
FLT3_OUT	FLT2_OUT	FLT1_OUT	FLT0_OUT
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-215. Fault Output Register (FAULTOUT) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	FLT3_OUT	R/W	0	FAULT[3] Pin Output Value 0 = FAULT[3] pin driven low when configured as output (Default) 1 = FAULT[3] pin driven high when configured as output
2	FLT2_OUT	R/W	0	FAULT[2] Pin Output Value 0 = FAULT[2] pin driven low when configured as output (Default) 1 = FAULT[2] pin driven high when configured as output
1	FLT1_OUT	R/W	0	FAULT[1] Pin Output Value 0 = FAULT[1] pin driven low when configured as output (Default) 1 = FAULT[1] pin driven high when configured as output
0	FLT0_OUT	R/W	0	FAULT[0] Pin Output Value 0 = FAULT[0] pin driven low when configured as output (Default) 1 = FAULT[0] pin driven high when configured as output

4.13.4 Fault Interrupt Enable Register (FAULTINTENA)

Address FFF7FA14

Figure 4-215. Fault Interrupt Enable Register (FAULTINTENA)

7	6	5	4	3	2	1	0
GIO_D_INT_EN	GIO_C_INT_EN	DTC_B_INT_EN	DTC_A_INT_EN	FLT3_INT_EN	FLT2_INT_EN	FLT1_INT_EN	FLT0_INT_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-216. Fault Interrupt Enable Register (FAULTINTENA) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GIO_D_INT_EN	R/W	0	GPIOD Interrupt Enable 0 = Interrupt disabled for GPIOD pin (Default) 1 = Interrupt enabled for GPIOD pin in GPIO mode
6	GIO_C_INT_EN	R/W	0	GPIOC Interrupt Enable 0 = Interrupt disabled for GPIOC pin (Default) 1 = Interrupt enabled for GPIOC pin in GPIO mode
5	DTC_B_INT_EN	R/W	0	DTC_B Interrupt Enable 0 = Interrupt disabled for DTC_B pin (Default) 1 = Interrupt enabled for DTC_B pin in GPIO mode
4	DTC_A_INT_EN	R/W	0	DTC_A Interrupt Enable 0 = Interrupt disabled for DTC_A pin (Default) 1 = Interrupt enabled for DTC_A pin in GPIO mode
3	FLT3_INT_EN	R/W	0	FAULT[3] Interrupt Enable 0 = Interrupt disabled for FAULT[3] pin (Default) 1 = Interrupt enabled for FAULT[3] pin
2	FLT2_INT_EN	R/W	0	FAULT[2] Interrupt Enable 0 = Interrupt disabled for FAULT[2] pin (Default) 1 = Interrupt enabled for FAULT[2] pin
1	FLT1_INT_EN	R/W	0	FAULT[1] Interrupt Enable 0 = Interrupt disabled for FAULT[1] pin (Default) 1 = Interrupt enabled for FAULT[1] pin
0	FLT0_INT_EN	R/W	0	FAULT[0] Interrupt Enable 0 = Interrupt disabled for FAULT[0] pin (Default) 1 = Interrupt enabled for FAULT[0] pin

4.13.5 Fault Interrupt Polarity Register (FAULTINTPOL)

Address FFF7FA18

Figure 4-216. Fault Interrupt Polarity Register (FAULTINTPOL)

7	6	5	4	3	2	1	0
GIO_D_INT_POL	GIO_C_INT_POL	DTC_B_INT_POL	DTC_A_INT_POL	FLT3_INT_POL	FLT2_INT_POL	FLT1_INT_POL	FLT0_INT_POL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-217. Fault Interrupt Polarity Register (FAULTINTPOL) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GIO_D_INT_POL	R/W	0	GPIOD Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge
6	GIO_C_INT_POL	R/W	0	GPIOC Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge
5	DTC_B_INT_POL	R/W	0	DTC_B Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge
4	DTC_A_INT_POL	R/W	0	DTC_A Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge
3	FLT3_INT_POL	R/W	0	FLT3_INT_POL– FAULT[3] Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge
2	FLT2_INT_POL	R/W	0	FLT2_INT_POL– FAULT[2] Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge
1	FLT1_INT_POL	R/W	0	FLT1_INT_POL– FAULT[1] Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge
0	FLT0_INT_POL	R/W	0	FLT0_INT_POL– FAULT[0] Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge

4.13.6 Fault Interrupt Pending Register (FAULTINTPEND)

Address FFF7FA1C

Figure 4-217. Fault Interrupt Pending Register (FAULTINTPEND)

7	6	5	4	3	2	1	0
GPIO_INT_PEND_GPIOD	GPIO_INT_PEND_GPIOC	GPIO_INT_PEND_GPIOB	GPIO_INT_PEND_GPIOA	FLT3_INT_PEND	FLT2_INT_PEND	FLT1_INT_PEND	FLT0_INT_PEND
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-218. Fault Interrupt Pending Register (FAULTINTPEND) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_INT_PEND_GPIOD	R/W	0	GPIO_INT_PEND_GPIOD Interrupt Pending[(1)] 0 = No interrupt detected (Default) 1 = Interrupt pending
6	GPIO_INT_PEND_GPIOC	R/W	0	GPIO_INT_PEND_GPIOC Interrupt Pending[(1)] 0 = No interrupt detected (Default) 1 = Interrupt pending
5	GPIO_INT_PEND_GPIOB	R/W	0	GPIO_INT_PEND_GPIOB Interrupt Pending[(1)] 0 = No interrupt detected (Default) 1 = Interrupt pending
4	GPIO_INT_PEND_GPIOA	R/W	0	GPIO_INT_PEND_GPIOA Interrupt Pending[(1)] 0 = No interrupt detected (Default) 1 = Interrupt pending
3	FLT3_INT_PEND	R/W	0	FAULT[3] has caused an interrupt[(1)] 0 = No Interrupt detected (Default) 1 = Interrupt pending
2	FLT2_INT_PEND	R/W	0	FAULT[2] has caused an interrupt[(1)] 0 = No Interrupt detected (Default) 1 = Interrupt pending
1	FLT1_INT_PEND	R/W	0	FAULT[1] has caused an interrupt[(1)] 0 = No Interrupt detected (Default) 1 = Interrupt pending
0	FLT0_INT_PEND	R/W	0	FAULT[0] has caused an interrupt[(1)] 0 = No Interrupt detected (Default) 1 = Interrupt pending

(1) Writing a 1 to a bit will clear the interrupt flag

4.13.7 External Interrupt Direction Register (EXTINTDIR)

Address FFF7FA20

Figure 4-218. External Interrupt Direction Register (EXTINTDIR)

0
EXT_INT_DIR
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-219. External Interrupt Direction Register (EXTINTDIR) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EXT_INT_DIR	R/W	0	EXT-INT Pin Configuration 0 = EXT-INT pin configured as an input pin (Default) 1 = EXT-INT pin configured as an output pin

4.13.8 External Interrupt Input Register (EXTINTIN)

Address FFF7FA24

Figure 4-219. External Interrupt Input Register (EXTINTIN)

0
EXT_INT_EN
R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-220. External Interrupt Input Register (EXTINTIN) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EXT_INT_EN	R	0	Input Value of EXT-INT Pin 0 = EXT-INT pin driven low in GPIO mode 1 = EXT-INT pin driven high in GPIO mode

4.13.9 External Interrupt Output Register (EXTINTOUT)

Address FFF7FA28

Figure 4-220. External Interrupt Output Register (EXTINTOUT)

0
EXT_INT_OUT
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-221. External Interrupt Output Register (EXTINTOUT) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EXT_INT_OUT	R/W	0	EXT-INT Pin Output Value 0 = EXT-INT pin driven low (Default) 1 = EXT-INT pin driven high

4.13.10 External Interrupt Enable Register (EXTINTENA)

Address FFF7FA34

Figure 4-221. External Interrupt Enable Register (EXTINTENA)

0
EXT_INT_EN
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-222. External Interrupt Enable Register (EXTINTENA) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EXT_INT_EN	R/W	0	EXT-INT Interrupt Enable 0 = Interrupt disabled for EXT-INT pin (Default) 1 = Interrupt enabled for EXT-INT pin

4.13.11 External Interrupt Polarity Register (EXTTINTPOL)

Address FFF7FA38

Figure 4-222. External Interrupt Polarity Register (EXTTINTPOL)

0
EXT_INT_POL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-223. External Interrupt Polarity Register (EXTTINTPOL) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EXT_INT_POL	R/W	0	EXT-INT Interrupt Polarity Select 0 = Interrupt generated on falling edge (Default) 1 = Interrupt generated on rising edge

4.13.12 External Interrupt Pending Register (EXTINTPEND)

Address FFF7FA3C

Figure 4-223. External Interrupt Pending Register (EXTINTPEND)

0
EXT_INT_PEND
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-224. External Interrupt Pending Register (EXTINTPEND) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EXT_INT_PEND	R/W	0	EXT-INT has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag. 0 = No Interrupt detected (Default) 1 = Interrupt pending

4.14 Timer Module Register Reference

Timer Registers have the following attributes:

- 32-bit wide
- Addresses placed on word boundaries
- Byte, Half-Word and word writes permitted
- All Registers can be read in any mode
- All Registers, except for the Timer Powerdown Control Register, are writeable in any mode. The Timer Powerdown Control Register is writeable only in privilege mode

4.14.1 24-bit Counter Data Register (T24CNTDAT)

Address FFF7FD00

Figure 4-224. 24-bit Counter Data Register (T24CNTDAT)

23		0
CNT_DAT		
R-0		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-225. 24-bit Counter Data Register (T24CNTDAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CNT_DAT	R	0	Contains the 24-bit counter value

4.14.2 24-bit Counter Control Register (T24CNTCTRL)

Address FFF7FD04

Figure 4-225. 24-bit Counter Control Register (T24CNTCTRL)

15	8	7	3	2	1	0
PRESCALE		Reserved		EXT_CLK_SEL	OV_INT_ENA	OV_FLAG
R/W-0000 0000		R-00000		R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-226. 24-bit Counter Control Register (T24CNTCTRL) Register Field Descriptions

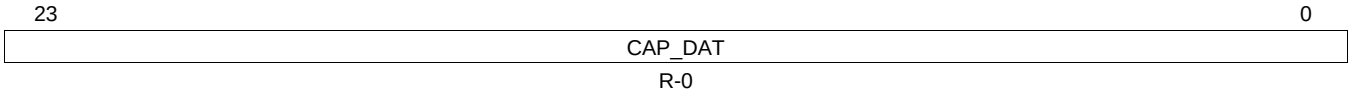
Bit	Field	Type	Reset	Description
15-8	PRESCALE	R/W	0000 0000	Defines the prescaler value used to select the 24-bit counter resolution. Counter Resolution = (Prescaler Value+1)*1/ICLK
7-3	Reserved	R/W	00000	
2	EXT_CLK_SEL	R/W	0	External Clock Select 0 = Selects ICLK as clock for 24-bit counter (Default) 1 = Selects External Clock on FAULT-0 as clock for 24-bit counter
1	OV_INT_ENA	R/W	0	Counter Overflow Interrupt Enable 0 = Disables 24-bit Counter Overflow Interrupt (Default) 1 = Enables 24-bit Counter Overflow Interrupt
0	OV_FLAG	R	0	Indicates a counter overflow. Overflow event is cleared by writing a '1' to this bit. If a clear and an overflow event occur at the same time, the flag will remain high (set has priority versus clear). 0 = No counter overflow since last clear 1 = Counter overflow since last clear

4.14.3 24-bit Capture Channel Data Register (T24CAPDAT) or (T24CAPDATx)

Address FFF7FD08 – 24-bit Capture Data Register 0

Address FFF7FD0C – 24-bit Capture Data Register 1

Figure 4-226. 24-bit Capture Channel Data Register (T24CAPDAT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-227. 24-bit Capture Channel Data Register (T24CAPDAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CAP_DAT	R	0	Contains the 24-bit input capture value

4.14.4 24-bit Capture Channel Control Register (T24CAPCTRLx or T24CAPCTRL)

Address FFF7FD14 – 24-bit Capture Channel Control Register 0

Address FFF7FD18 – 24-bit Capture Channel Control Register 1

Figure 4-227. 24-bit Capture Channel Control Register (T24CAPCTRL)

5	4	3	2	1	0
CAP_SEL		EDGE		CAP_INT_ENA	CAP_INT_FLAG
R/W-00		R/W-00		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-228. 24-bit Capture Channel Control Register (T24CAPCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
5-4	CAP_SEL	R/W	00	Capture Pin Select 00 = TCAP pin (Default) 01 = SCI_RX[0] pin 10 = SCI_RX[1] pin 11 = SYNC pin
3-2	EDGE	R/W	00	Input Capture Edge Select 00 = No Capture (Default) 01 = Rising Edge 10 = Falling Edge 11 = Both Edges
1	CAP_INT_ENA	R/W	0	Input Capture Interrupt Enable 0 = Disables 24-bit input capture interrupt (Default) 1 = Enables 24-bit input capture interrupt
0	CAP_INT_FLAG	R/W	0	Flag which indicates a valid input capture event. This bit is cleared by writing a ‘1’ to it or by reading the corresponding Capture Channel Data Register. If a clear and a valid capture event occur at the same time, the flag will remain high (set has priority versus clear). 0 = No valid capture event since last clear 1 = Valid capture event since last clear

4.14.5 24-bit Capture I/O Control and Data Register (T24CAPIO)

Address FFF7FD20

Figure 4-228. 24-bit Capture I/O Control and Data Register (T24CAPIO)

5	4	3	2	1	0
TCAP_1_IN*	TCAP_1_OUT*	TCAP_1_DIR*	TCAP_0_IN*	TCAP_0_OUT*	TCAP_0_DIR*
R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-229. 24-bit Capture I/O Control and Data Register (T24CAPIO) Register Field Descriptions

Bit	Field	Type	Reset	Description
5	TCAP_1_IN	R	0	Input data for pin TCAP_1/TDI/TDO pin, when connected to chip I/O 0 = Logic level low detected on TCAP pin 1 = Logic level high detected on TCAP pin
4	TCAP_OUT	R/W	0	Output data for pin TCAP_1 pin, when connected to chip I/O 0 = Logic level low driven on TCAP_1 pin in output mode (Default) 1 = Logic level high driven on TCAP_1 pin in output mode
3	TCAP_1_DIR	R/W	0	Controls data direction for pin TCAP, when connected to chip I/O 0 = TCAP_1 pin configured as input (Default) 1 = TCAP_1 pin configured as output
2	TCAP_IN or TCAP_0_IN	R	0	Input data for TCAP or TCAP0 pin, when connected to chip I/O 0 = Logic level low detected on TCAP pin 1 = Logic level high detected on TCAP pin
1	TCAP_OUT or TCAP_0_OUT	R/W	0	Output data for TCAP or TCAP0 pin, when connected to chip I/O 0 = Logic level low driven on TCAP pin in output mode (Default) 1 = Logic level high driven on TCAP pin in output mode
0	TCAP_DIR or TCAP_0_DIR*	R/W	0	Controls data direction for TCAP or TCAP0 pin, when connected to chip I/O 0 = TCAP pin configured as input (Default) 1 = TCAP pin configured as output

4.14.6 24-bit Output Compare Channel 0 Data Register (T24CMPDAT0)

Address FFF7FD24

Figure 4-229. 24-bit Output Compare Channel 0 Data Register (T24CMPDAT0)

23	0
CMP_DAT	
R/W-0000 0000 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-230. 24-bit Output Compare Channel 0 Data Register (T24CMPDAT0) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CMP_DAT	R/W	0000 0000 0000 0000 0000 0000	Contains the 24-bit output comparison value

4.14.7 24-bit Output Compare Channel 1 Data Register (T24CMPDAT1)

Address FFF7FD28

Figure 4-230. 24-bit Output Compare Channel 1 Data Register (T24CMPDAT1)

23		0
CMP_DAT		
R/W-0000 0000 0000 0000 0000 0000		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-231. 24-bit Output Compare Channel 1 Data Register (T24CMPDAT1) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-01	CMP_DAT	R/W	0000 0000 0000 0000 0000 0000	Contains the 24-bit output comparison value

4.14.8 24-bit Output Compare Channel 0 Control Register (T24CMPCTRL0)

Address FFF7FD2C

Figure 4-231. 24-bit Output Compare Channel 0 Control Register (T24CMPCTRL0)

1	0
CMP_INT_ENA	CMP_INT_FLAG
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-232. 24-bit Output Compare Channel 0 Control Register (T24CMPCTRL0) Register Field Descriptions

Bit	Field	Type	Reset	Description
1	CMP_INT_ENA	R/W	0	Output Compare Channel Interrupt 0 = Disables Output Compare Channel Interrupt (Default) 1 = Enables Output Compare Channel Interrupt
0	CMP_INT_FLAG	R/W	0	Indicates a valid output compare event. Bit can be cleared by writing a '1' to the bit or by rewriting the 24-bit Output Compare Channel Data Register. If a clear and compare event occur at the same time, the flag will remain high (set has priority versus clear). 0 = No compare event since last clear 1 = Compare event since last clear

4.14.9 24-bit Output Compare Channel 1 Control Register (T24CMPCTRL1)

Address FFF7FD30

Figure 4-232. 24-bit Output Compare Channel 1 Control Register (T24CMPCTRL1)

1	0
CMP_INT_ENA	CMP_INT_FLAG
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-233. 24-bit Output Compare Channel 1 Control Register (T24CMPCTRL1) Register Field Descriptions

Bit	Field	Type	Reset	Description
1	CMP_INT_ENA	R/W	0	Output Compare Channel Interrupt 0 = Disables Output Compare Channel Interrupt (Default) 1 = Enables Output Compare Channel Interrupt
0	CMP_INT_FLAG	R/W	0	Indicates a valid output compare event. Bit can be cleared by writing a '1' to the bit or by rewriting the 24-bit Output Compare Channel Data Register. If a clear and compare event occur at the same time, the flag will remain high (set has priority versus clear). 0 = No compare event since last clear 1 = Compare event since last clear

4.14.10 PWMx Counter Data Register (T16PWMxCNTDAT)

Address FFF7FD34 – 16-bit PWM0 Counter Data Register

Address FFF7FD58 – 16-bit PWM1 Counter Data Register

Address FFF7FD6C – 16-bit PWM2 Counter Data Register

Address FFF7FD80 – 16-bit PWM3 Counter Data Register

Figure 4-233. PWMx Counter Data Register (T16PWMxCNTDAT)

15		0
CNT_DAT		
R-0		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-234. PWMx Counter Data Register (T16PWMxCNTDAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CNT_DAT	R	0	Contains the 16-bit counter value. Read-only.

4.14.11 PWMx Counter Control Register (T16PWMxCNTCTRL)

Address FFF7FD38 – 16-bit PWM0 Counter Control Register

Address FFF7FD5C – 16-bit PWM1 Counter Control Register

Address FFF7FD70 – 16-bit PWM2 Counter Control Register

Address FFF7FD84 – 16-bit PWM3 Counter Control Register

Figure 4-234. PWMx Counter Control Register (T16PWMxCNTCTRL)

15							8
PRESCALE							
R/W-0000 0000							
7	6	5	4	3	2	1	0
Reserved	SYNC_SEL		SYNC_EN	SW_RESET	CMP_RESET_ENA	OV_INT_ENA	OV_INT_FLAG
R-0	R/W-00		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-235. PWMx Counter Control Register (T16PWMxCNTCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PRESCALE	R/W	0000 0000	Defines the prescaler value to select the PWM counter resolution. Counter Resolution = (Prescaler + 1) *1/ICLK
7	Reserved	R	0	
6-5	SYNC_SEL	R/W	00	Configures master PWM counter 0 = PWM0 Counter (Default) 1 = PWM1 Counter 2 = PWM2 Counter 3 = PWM3 Counter
4	SYNC_EN	R/W	0	PWM counter starts when master PWM counter is enabled 0 = PWM counter independent of other PWM counters (Default) 1 = PWM counter controlled by Master PWM counter
3	SW_RESET	R/W	0	PWM counter reset by software. This bit is cleared after reset and has to be set to run the PWM counter. 0 = PWM counter reset and counter stop (Default) 1 = PWM counter is running
2	CMP_RESET_ENA	R/W	0	Enables PWM counter reset by compare action of T16CMPxDR. 0 = Disable PWM counter reset by compare action (Default) 1 = Enable PWM counter reset by compare action
1	OV_INT_ENA	R/W	0	PWM Counter Overflow Interrupt Enable 0 = Disable PWM counter overflow interrupt (Default) 1 = Enable PWM counter overflow interrupt
0	OV_INT_FLAG	R/W	0	Flag which indicates a PWM counter overflow. This bit is cleared by writing ‘1’ to it. If a clear and an overflow event occur at the same time, the flag will remain high (set has priority versus clear). 0 = No PWM counter overflow since last clear 1 = PWM counter overflow since last clear

4.14.12 PWMx 16-bit Compare Channel 0-1 Data Register (T16PWMxCMPyDAT)

Address FFF7FD3C – 16-bit PWM0 Compare Channel 0 Data Register

Address FFF7FD40 – 16-bit PWM0 Compare Channel 1 Data Register

Address FFF7FD60 – 16-bit PWM1 Compare Channel 0 Data Register

Address FFF7FD64 – 16-bit PWM1 Compare Channel 1 Data Register

Address FFF7FD74 – 16-bit PWM2 Compare Channel 0 Data Register

Address FFF7FD78 – 16-bit PWM2 Compare Channel 1 Data Register

Address FFF7FD88 – 16-bit PWM3 Compare Channel 0 Data Register

Address FFF7FD8C – 16-bit PWM3 Compare Channel 1 Data Register

Figure 4-235. PWMx 16-bit Compare Channel 0-1 Data Register (T16PWMxCMPyDAT)

15	0
CMP_DAT	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-236. PWMx 16-bit Compare Channel 0-1 Data Register (T16PWMxCMPyDAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMP_DAT	R/W	0000 0000 0000 0000	Contains the 16-bit compare value. When in PWM mode, the value in the T16PWMxCMPyDAT is loaded after a match with the PWMx Counter Data Register. When in OC mode, it has to be written by the CPU. The mode is controlled by the bit SHADOW in the PWMx/Dual Compare Control Register. If both Registers T16PWMxCMP0DAT and T16PWMxCMP1DAT contain the same value, the interrupt and pin behavior is controlled by output compare channel 0 (T16PWMxCMP0DAT has priority over T16PWMxCMP1DAT).

4.14.13 PWMx Compare Control Register (T16PWMxCMPCTRL)

Address FFF7FD44 – 16-bit PWM0 Compare Control Register

Address FFF7FD68 – 16-bit PWM1 Compare Control Register

Address FFF7FD7C – 16-bit PWM2 Compare Control Register

Address FFF7FD90 – 16-bit PWM3 Compare Control Register

Figure 4-236. PWMx Compare Control Register (T16PWMxCMPCTRL)

12	11	10	9	8
SHADOW	PWM_IN	PWM_OUT	PWM_OUT_ENA	PWM_OUT_DRV
R/W-0	R-0	R/W-0	R/W-0	R/W-0

7 6	5 4	3	2	1	0
PWM_OUT_ACTION1	PWM_OUT_ACTION0	CMP1_INT_ENA	CMP1_INT_FLAG	CMP0_INT_ENA	CMP0_INT_FLAG
R/W-00	R/W-00	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-237. PWMx Compare Control Register (T16PWMxCMPCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
12	SHADOW	R/W	0	Controls the update of the 16-bit output compare Registers. 0 = PWM output compare Registers immediately written (Default) 1 = PWM output compare Registers updated through the buffers T16PWMxCMPyDAT after a match occurs in the corresponding Register T16PWMxCMPyDAT.
11	*PWM_IN	R	0	Input value of PWM pin when configured in PWM mode 0 = Logic level low detected on PWM pin 1 = Logic level high detected on PWM pin
10	*PWM_OUT	R/W	0	Data to be written into the output latch when PWM_OUT_DRV is high. 0 = Output latch is cleared when PWM_OUT_DRV=1 (Default) 1 = Output latch is set when PWM_OUT_DRV=1
9	*PWM_OUT_ENA	R/W	0	FAN-PWM pin configuration 0 = FAN-PWM configured as an input pin (Default) 1 = FAN-PWM configured as an output pin
8	*PWM_OUT_DRV	R/W	0	Causes the value of the bit PWM_OUT to be written into the output latch. So it is possible to preload the output latch or to use the pin as GPIO. The compare action has priority before the preload function. This bit is always read as '0'. 0 = Output latch not affected by the value of PWM_OUT (Default) 1 = Value of OUT written into the output latch
7-6	PWM_OUT_ACTION1	R/W	00	These 2 bits select the output action when a compare equal is detected on T16CMP1DAT 00 = No action (Default) 01 = Set pin 10 = Clear pin 11 = Toggle pin
5-4	PWM_OUT_ACTION0	R/W	00	Selects the output action when a compare equal is detected on T16CMP0DAT. 00 = No action (Default) 01 = Set pin 10 = Clear pin 11 = Toggle pin
3	CMP1_INT_ENA	R/W	0	Compare 1 Interrupt Enable 0 = Disables Compare 1 Interrupt (Default) 1 = Enables Compare 1 Interrupt

Table 4-237. PWMx Compare Control Register (T16PWMxCMPCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CMP1_INT_FLAG	R/W	0	Flag which indicates a valid output compare 1 event. This bit is cleared by writing '1' to this bit or by rewriting T16PWMxCMP1DAT. If a clear and a compare event occurs at the same time, the flag will remain high (set has priority versus write clear). 0 = No compare event since last clear 1 = Compare event since last clear
1	CMP0_INT_ENA	R/W	0	Compare 0 Interrupt Enable 0 = Disables Compare 0 Interrupt (Default) 1 = Enables Compare 0 Interrupt
0	CMP0_INT_FLAG	R/W	0	Flag which indicates a valid output compare 1 event. This bit is cleared by writing '1' to this bit or by rewriting T16PWMxCMP0DAT. If a clear and a compare event occurs at the same time, the flag will remain high (set has priority versus write clear). 0 = No compare event since last clear 1 = Compare event since last clear

4.14.14 Watchdog Status (WDST)

Address FFF7FD94

Figure 4-237. Watchdog Status (WDST)

3	2	1	0
WAKE_EV_RAW	WD_EV_RAW	WAKE_EV_INT	WD_EV_INT
R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-238. Watchdog Status (WDST) Register Field Descriptions

Bit	Field	Type	Reset	Description
3	WAKE_EV_RAW	R	0	Watchdog Wake Event Raw Status 0 = Watchdog Timer has not reached ½ of terminal count 1 = Watchdog Timer has reached ½ of terminal count
2	WD_EV_RAW	R	0	Watchdog Event Raw Status 0 = Watchdog Timer has not reached terminal count 1 = Watchdog Timer has reached terminal count
1	WAKE_EV_INT	R	0	Watchdog Wake Event Interrupt Status, cleared on read of Watchdog Status Register 0 = Watchdog Timer has not reached ½ of terminal count 1 = Watchdog Timer has reached ½ of terminal count
0	WD_EV_INT	R	0	Watchdog Event Interrupt Status, cleared on read of Watchdog Status Register 0 = Watchdog Timer has not reached terminal count 1 = Watchdog Timer has reached terminal count

4.14.15 Watchdog Control (WDCTRL)

Address FFF7FD98

Figure 4-238. Watchdog Control (WDCTRL)

14 8	7	6	5	4	3	2	1	0
WD_PERIOD	Reserved	PROTECT	CPU_RESET_EN	WDRST_INT_EN	WKEV_INT_EN	WKEV_EN	WDRST_EN	CNT_RESET
R/W-1111 1111	R-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-239. Watchdog Control (WDCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
14-8	WD_PERIOD	R/W	1111 1111	Configures the time for the watchdog reset. H'7F ~ 2.2s typical (1.85 min to 2.6 max seconds)(Default) H'00 ~ 17mstypical (14.5 min to 20.1 max milliseconds)
7	Reserved	R	0	
6	PROTECT	R/W	1	Watchdog Protect Bit, Active Low 0 = Watchdog enable bits are protected, only can be cleared by POR. CPU_RESET_ENA (Bit 5), WDRST_ENA (Bit 2) and WKEV_ENA (Bit 1) are automatically set high when PROTECT is written low. 1 = Watchdog enable bits can be set by processor (Default)
5	CPU_RESET_EN	R/W	0	Enables Watchdog Reset Event to reset the CPU 0 = Watchdog Reset does not reset CPU (Default) 1 = Watchdog Reset resets CPU and peripherals
4	WDRST_INT_EN	R/W	0	Watchdog Reset Event Interrupt Enable 0 = Disables generation of Watchdog Reset Interrupt (Default) 1 = Enables generation of Watchdog Reset Interrupt
3	WKEV_INT_EN	R/W	0	Watchdog Wake Event Interrupt Enable 0 = Disables generation of Watchdog Wake Event Interrupt (Default) 1 = Enables generation of Watchdog Wake Event Interrupt
2	WKEV_EN	R/W	0	Watchdog Wake Event Comparator Enable 0 = Disables Watchdog Wake Event Comparator (Default) 1 = Enables Watchdog Wake Event Comparator
1	WDRST_EN	R/W	0	Watchdog Reset Event Comparator Enable 0 = Disables Watchdog Reset Event Comparator (Default) 1 = Enables Watchdog Reset Event Comparator
0	CNT_RESET	R/W	1	This bit resets the watchdog counters. This bit self clears and if the enables are set, the counters restart counting. 0 = Watchdog counters enabled (Default) 1 = Watchdog counters reset

4.15 Memory Controller – MMC Registers Reference

All MMC control registers have the following attributes:

- 16-bit width
- Addresses placed on word boundaries
- 16-bit data is placed on the least significant data bus D[15:0]
- Only half-word writes are permitted
- Registers are readable in any mode, but writeable only in privilege mode

4.15.1 Static Memory Control Register (SMCTRL)

Address FFFFFD00

Figure 4-239. Static Memory Control Register (SMCTRL)

13 12	11 9	8	7 4	3	2	1 0
LEAD	TRAIL	Rsvd	ACTIVE	ENDIAN	Rsvd	WIDTH
R/W-00	R/W-000	R-0	R/W-0000	R-0	R-0	R/W-00

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-240. Static Memory Control Register (SMCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
13-12	LEAD	R/W	00	Address setup time cycles (write operations) 00 = No setup time required (Default) 01 = Write strobe is delayed one cycle 10 = Write strobe is delayed two cycles 11 = Write strobe is delayed three cycles
11-9	TRAIL	R/W	000	Number of Trailing wait states. Determine the trailing wait states after read and write operations to the memory associated with the chip select corresponding to the wait states.
8	Reserved	R	0	
7-4	ACTIVE	R/W	0000	Active Wait states (both read/write operations) 0000 = 0 Wait states (Default) 0001 = 1 Wait states 0010 = 2 Wait states 0011 = 3 Wait states 0100 = 4 Wait states 0101 = 5 Wait states 0110 = 6 Wait states 0111 = 7 Wait states 1000 = 8 Wait states 1001 = 9 Wait states 1010 = 10 Wait states 1011 = 11 Wait states 1100 = 12 Wait states 1101 = 13 Wait states 1110 = 14 Wait states 1111 = 15 Wait states
3	ENDIAN	R	0	Endian Mode Identification 0 = CPU configured in big endian mode 1 = CPU configured in little endian mode
2	Reserved	R	0	

Table 4-240. Static Memory Control Register (SMCTRL) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	WIDTH	R/W	00	Data Width for Memories 00 = 8 bits (Default) 01 = 16 bits 10 = 32 bits 11 = Reserved

4.15.2 Write Control Register (WCTRL)

Address FFFFFD2C

Figure 4-240. Write Control Register (WCTRL)

1	0
TRAIL_OVR	WBUF_ENA
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-241. Write Control Register (WCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
1	TRAIL_OVR	R/W	0	Write trailing wait state override. 0 = At least one trailing wait state (Default) 1 = TRAIL sets trailing wait states
0	WBUF_ENA	R/W	0	Write buffer enable. When this bit is 1, the memory controller latches the data and control signals in the first cycle for write operations to the memories and peripherals on the expansion bus and lets the CPU perform other operations. However, the CPU starts a wait state if there is another request before the memory controller finishes. 0 = Write buffer disabled (Disabled) 1 = Write buffer enabled

4.15.3 Peripheral Control Register (PCTRL)

Address FFFFFD30

Figure 4-241. Peripheral Control Register (PCTRL)

0
PBUF_ENA
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-242. Peripheral Control Register (PCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PUBF_ENA	R/W	0	Write buffer enable. When this bit is set to 1, the memory controller latches the data and control signals in the first cycle for write operations to the memories and peripherals on the expansion bus and lets the CPU perform other operations. However, the CPU starts a wait state if there is another request before the memory controller finishes. 0 = Write buffer disabled (Default) 1 = Write buffer enabled

4.15.4 Peripheral Location Register (PLOC)

Address FFFFFD34

Figure 4-242. Peripheral Location Register (PLOC)

15	0
LOC	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-243. Peripheral Location Register (PLOC) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	LOC	R/W	0000 0000 0000 0000	These 16 bits represent the peripheral location bits, which correspond to each of the 16 peripheral selects. 0 = Peripheral is internal (Default) 1 = Peripheral is external

4.15.5 Peripheral Protection Register (PPROT)

Address FFFFFD38

Figure 4-243. Peripheral Protection Register (PPROT)

15	0
PROT	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-244. Peripheral Protection Register (PPROT) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PROT	R/W	0000 0000 0000 0000	These 16 bits represent the peripheral protection bits, which correspond to each of the 16 peripheral selects. 0 = Peripheral is accessible in all modes (Default) 1 = Peripheral is accessible in privilege mode only

4.16 DEC – Address Manager Registers Reference

The DEC generates the memory selects and SAR peripheral select signals by decoding the address and control signals from the ARM processor. In addition, the DEC provides the control signals for the Program and Data Flash.

The assigned memory selects for UCD3138 are as follows:

Memory Select 0 => Boot ROM (1Kx32)

Memory Select 1 => Program Flash (8Kx32)

Memory Select 2 => Data Flash (512x32)

Memory Select 3 => Data RAM (1Kx32)

Memory Select 4 => Loop Mux (1Kx32)

Memory Select 5 => Fault Mux (1Kx32)

Memory Select 6 => ADC12 Control (1Kx32)

Memory Select 7 => DPWM3 (1Kx32)

Memory Select 8 => Filter 2 (1Kx32)

Memory Select 9 => DPWM 2 (1Kx32)

Memory Select 10 => Front End Control 2 (1Kx32)

Memory Select 11 => Filter 1 (1Kx32)

Memory Select 12 => DPWM 1 (1Kx32)

Memory Select 13 => Front End Control 1 (1Kx32)

Memory Select 14 => Filter 0 (1Kx32)

Memory Select 15 => DPWM 0 (1Kx32)

Memory Select 16 => Front End Control 0 (1Kx32)

Memory Select 17 => Program Flash 1(8Kx32) – Not in UCD3138, in all other devices

Memory Select 18 => Program Flash 2(8Kx32) - Only in 3138128

Memory Select 19 => Program Flash 3(8Kx32) - Only in 3138128

Some of the bit descriptions below show up to 4 values for bit states. This is because the memory maps change when the UCD goes from power up to ROM mode and to the 2 Flash modes. For an overview of this process, see the memory map section of the UCD3138128/064 Programmer's Manual.

The modes are:

1. Power up – after reset, before ROM starts running
2. ROM Mode
3. Flash 0 – This is if blocks 0 and 1 are mapped to start at location 0
4. Flash 2 – This is if blocks 2 and 3 are mapped to start at location 0

4.16.1 Memory Fine Base Address High Register 0 (MFBAHR0)

Address FFFFFE00

Figure 4-244. Memory Fine Base Address High Register 0 (MFBAHR0)

15	0
ADDRESS[31:16]	
R/W	
Power Up-0000 0000 0000 0000 ROM Mode-0000 0000 0000 0000 Flash Modes-0000 0000 0000 0002	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-245. Memory Fine Base Address High Register 0 (MFBAHR0) Register Field Descriptions

Bit	Field	Type	Reset			Description
			Power Up	ROM Mode	Flash Modes	
15-0	ADDRESS[31:16]	R/W	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0002	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.2 Memory Fine Base Address Low Register 0 (MFBALR0)

Address FFFFFE04

Figure 4-245. Memory Fine Base Address Low Register 0 (MFBALR0)

15	10	8	7	4	1	0
ADDRESS[15:10]		MS	BLOCK_SIZE		RONLY	PRIV
R/W Power-Up-00 0000 ROM Mode-00 0000 Flash Modes-00 0000		R/W Power-Up-0 ROM Mode-1 Flash Modes-1	R/W Power-Up-0000 ROM Mode-1001 Flash Modes-0100		R/W Power-Up-0 ROM Mode-1 Flash Modes-1	R/W Power-Up-0 ROM Mode-0 Flash Modes-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-246. Memory Fine Base Address Low Register 0 (MFBALR0) Register Field Descriptions

Bit	Field	Type	Reset			Description
			Power Up	ROM Mode	Flash Modes	
15-10	ADDRESS[15:10]	R/W	00 0000	00 0000	00 0000	6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.
8	MS	R/W	0	1	1	Memory Map Select 0 = Memory Map configuration not updated (Default) 1 = Enables the fine and coarse memory selects and activates the memory map
7-4	BLOCK_SIZE	R/W	0000	1001	0100	Configures the size of the memory 0000 = Memory select is disabled (Default) 0001 = 1KB 0010 = 2KB 0011 = 4KB 0100 = 8KB 0101 = 16KB 0110 = 32KB 0111 = 64KB 1000 = 128KB 1001 = 256KB 1010 = 512KB 1011 = 1MB 1100 = 2MB 1101 = 4MB 1110 = 8MB 1111 = 16MB
1	RONLY	R/W	0	1	0	Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory. 0 = Read/write access to memory (Default) 1 = Read accesses to memory only
0	PRIV	R/W	0	0	0	Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode. 0 = User/privilege mode accesses to memory (Default) 1 = Privilege mode accesses to memory only

4.16.3 1.1.1 Memory Fine Base Address High Register 1-3,17-19 (MFBAHRx)

Address FFFFFE08 – Memory Fine Base Address High Register 1

Address FFFFFE10 – Memory Fine Base Address High Register 2

Address FFFFFE18 – Memory Fine Base Address High Register 3

Address FFFFFE88 – Memory Fine Base Address High Register 17

Address FFFFFEA8 – Memory Fine Base Address High Register 18

Address FFFFFEB0 – Memory Fine Base Address High Register 19

Figure 4-246. Memory Fine Base Address High Register 1 and 17 (MFBAHRx)

15	0
ADDRESS[31:16]	

R/W
Power Up-0000 0000 0000 0000
ROM Mode-0000 0000 0000 0100
Flash 0-0000 0000 0000 0000
Flash 1-0000 0000 0000 0001

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 4-247. Memory Fine Base Address High Register 2 and 3 (MFBAHRx)

15	0
ADDRESS[31:16]	

R/W
Power Up-0000 0000 0000 0000
ROM and Flash Modes-0000 0000 0000 0110

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 4-248. Memory Fine Base Address High Register 18 and 19 (MFBAHRx)

15	0
ADDRESS[31:16]	

R/W
Power Up-0000 0000 0000 0000
ROM Mode-0000 0000 0000 0101
Flash 0-0000 0000 0000 0001
Flash 1-0000 0000 0000 0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-247. Memory Fine Base Address High Register 1 and 17 (MFBAHRx) Register Field Descriptions

Bit	Field	Type	Reset				Description
			Power Up	ROM Mode	Flash 0	Flash 2	
15-0	ADDRESS[31:16]	R/W	0000 0000 0000 0000	0000 0000 0000 0100	0000 0000 0000 0000	0000 0000 0000 0001	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

Table 4-248. Memory Fine Base Address High Register 2 and 3 (MFBAHRx) Register Field Descriptions

Bit	Field	Type	Reset		Description
			Power Up	ROM and Flash Modes	
15-0	ADDRESS[31:16]	R/W	0000 0000 0000 0000	0000 0000 0000 0110	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

Table 4-249. Memory Fine Base Address High Register 18 and 19 (MFBAHRx) Register Field Descriptions

Bit	Field	Type	Reset				Description
			Power Up	ROM Mode	Flash 0	Flash 2	
15-0	ADDRESS[31:16]	R/W	0000 0000 0000 0000	0000 0000 0000 0101	0000 0000 0000 0001	0000 0000 0000 0000	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.4 Memory Fine Base Address Low Register 1-3, 17-19 (MFBALRx)

Address FFFFFE0C – Memory Fine Base Address Low Register 1

Address FFFFFE14 – Memory Fine Base Address Low Register 2

Address FFFFFE1C – Memory Fine Base Address Low Register 3

Address FFFFFE8C – Memory Fine Base Address Low Register 17

Address FFFFFEAC – Memory Fine Base Address Low Register 18

Address FFFFFEB4 – Memory Fine Base Address Low Register 19

Figure 4-249. Memory Fine Base Address Low Register 1 and 18 (MFBALRx)

15	10	9	7	4	1	0
ADDRESS[15:10]		AW	BLOCK_SIZE		RONLY	PRIV
R/W-00 0000		R/W-0	R/W Power Up-0000 ROM and Flash Modes-0110		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 4-250. Memory Fine Base Address Low Register 2 (MFBALRx)

15	10	9	7	4	1	0
ADDRESS[15:10]		AW	BLOCK_SIZE		RONLY	PRIV
R/W- Power Up-00 0000 ROM and Flash Modes-10 0110		R/W-0	R/W Power Up-0000 ROM and Flash Modes-0100		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 4-251. Memory Fine Base Address Low Register 3 (MFBALRx)

15	10	9	7	4	1	0
ADDRESS[15:10]		AW	BLOCK_SIZE		RONLY	PRIV
R/W- Power Up-00 0000 ROM and Flash Modes-10 1000		R/W-0	R/W Power Up-0000 ROM and Flash Modes-0100		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 4-252. Memory Fine Base Address Low Register 2 (MFBALRx)

15	10	9	7	4	1	0
ADDRESS[15:10]		AW	BLOCK_SIZE		RONLY	PRIV
R/W- Power Up-00 0000 ROM and Flash Modes-10 0110		R/W-0	R/W Power Up-0000 ROM and Flash Modes-0100		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 4-253. Memory Fine Base Address Low Register 17 and 19 (MFBALRx)

15	10	9	7	4	1	0
ADDRESS[15:10]		AW	BLOCK_SIZE		RONLY	PRIV
R/W- Power Up-00 0000 ROM and Flash Modes-10 0000		R/W-0	R/W Power Up-0000 ROM and Flash Modes-0110		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-250. Memory Fine Base Address Low Register 1 and 18 (MFBALRx) Register Field Descriptions

Bit	Field	Type	Reset		Description
			Power Up	ROM and Flash Modes	
15-10	ADDRESS[15:10]	R/W	00 0000	00 0000	6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.
9	AW	R/W	0	0	Auto-wait-on-write. When this bit is set, any write operation on this memory select takes two system cycles. 0 = Write operation is not supplemented with an additional cycle (Default) 1 = Write operation takes an additional cycle
7-4	BLOCK_SIZE	R/W	0000	0110	Configures the size of the memory 0000 = Memory select is disabled (Default) 0001 = 1KB 0010 = 2KB 0011 = 4KB 0100 = 8KB 0101 = 16KB 0110 = 32KB 0111 = 64KB 1000 = 128KB 1001 = 256KB 1010 = 512KB 1011 = 1MB 1100 = 2MB 1101 = 4MB 1110 = 8MB 1111 = 16MB
1	RONLY	R/W	0	0	Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory. 0 = Read/write access to memory (Default) 1 = Read accesses to memory only
0	PRIV	R/W	0	0	Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode. 0 = User/privilege mode accesses to memory (Default) 1 = Privilege mode accesses to memory only

Table 4-251. Memory Fine Base Address Low Register 2 (MFBALRx) Register Field Descriptions

Bit	Field	Type	Reset		Description
			Power Up	ROM and Flash Modes	
15-10	ADDRESS[15:10]	R/W	00 0000	10 0110	6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.
9	AW	R/W	0	0	Auto-wait-on-write. When this bit is set, any write operation on this memory select takes two system cycles. 0 = Write operation is not supplemented with an additional cycle (Default) 1 = Write operation takes an additional cycle
7-4	BLOCK_SIZE	R/W	0000	0010	Configures the size of the memory 0000 = Memory select is disabled (Default) 0001 = 1KB 0010 = 2KB 0011 = 4KB 0100 = 8KB 0101 = 16KB 0110 = 32KB 0111 = 64KB 1000 = 128KB 1001 = 256KB 1010 = 512KB 1011 = 1MB 1100 = 2MB 1101 = 4MB 1110 = 8MB 1111 = 16MB
1	RONLY	R/W	0	0	Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory. 0 = Read/write access to memory (Default) 1 = Read accesses to memory only
0	PRIV	R/W	0	0	Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode. 0 = User/privilege mode accesses to memory (Default) 1 = Privilege mode accesses to memory only

Table 4-252. Memory Fine Base Address Low Register 3 (MFBALRx) Register Field Descriptions

Bit	Field	Type	Reset		Description
			Power Up	ROM and Flash Modes	
15-10	ADDRESS[15:10]	R/W	00 0000	10 1000	6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.
9	AW	R/W	0	0	Auto-wait-on-write. When this bit is set, any write operation on this memory select takes two system cycles. 0 = Write operation is not supplemented with an additional cycle (Default) 1 = Write operation takes an additional cycle
7-4	BLOCK_SIZE	R/W	0000	0100	Configures the size of the memory 0000 = Memory select is disabled (Default) 0001 = 1KB 0010 = 2KB 0011 = 4KB 0100 = 8KB 0101 = 16KB 0110 = 32KB 0111 = 64KB 1000 = 128KB 1001 = 256KB 1010 = 512KB 1011 = 1MB 1100 = 2MB 1101 = 4MB 1110 = 8MB 1111 = 16MB
1	RONLY	R/W	0	0	Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory. 0 = Read/write access to memory (Default) 1 = Read accesses to memory only
0	PRIV	R/W	0	0	Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode. 0 = User/privilege mode accesses to memory (Default) 1 = Privilege mode accesses to memory only

Table 4-253. Memory Fine Base Address Low Register 17 and 19 (MFBALRx) Register Field Descriptions

Bit	Field	Type	Reset		Description
			Power Up	ROM and Flash Modes	
15-10	ADDRESS[15:10]	R/W	00 0000	10 0000	6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.
9	AW	R/W	0	0	Auto-wait-on-write. When this bit is set, any write operation on this memory select takes two system cycles. 0 = Write operation is not supplemented with an additional cycle (Default) 1 = Write operation takes an additional cycle
7-4	BLOCK_SIZE	R/W	0000	0110	Configures the size of the memory 0000 = Memory select is disabled (Default) 0001 = 1KB 0010 = 2KB 0011 = 4KB 0100 = 8KB 0101 = 16KB 0110 = 32KB 0111 = 64KB 1000 = 128KB 1001 = 256KB 1010 = 512KB 1011 = 1MB 1100 = 2MB 1101 = 4MB 1110 = 8MB 1111 = 16MB
1	RONLY	R/W	0	0	Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory. 0 = Read/write access to memory (Default) 1 = Read accesses to memory only
0	PRIV	R/W	0	0	Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode. 0 = User/privilege mode accesses to memory (Default) 1 = Privilege mode accesses to memory only

4.16.5 Memory Fine Base Address High Register 4 (MFBAHR4)

Address FFFFFE20 – Memory Fine Base Address High Register 4

Figure 4-254. Memory Fine Base Address High Register 4 (MFBAHR4)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 0010	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-254. Memory Fine Base Address High Register 4 (MFBAHR4) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 0010	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.6 Memory Fine Base Address Low Register 4-16 (MFBALRx)

Address FFFFFE24 – Memory Fine Base Address Low Register 4

Address FFFFFE2C – Memory Fine Base Address Low Register 5

Address FFFFFE34 – Memory Fine Base Address Low Register 6

Address FFFFFE3C – Memory Fine Base Address Low Register 7

Address FFFFFE44 – Memory Fine Base Address Low Register 8

Address FFFFFE4C – Memory Fine Base Address Low Register 9

Address FFFFFE54 – Memory Fine Base Address Low Register 10

Address FFFFFE5C – Memory Fine Base Address Low Register 11

Address FFFFFE64 – Memory Fine Base Address Low Register 12

Address FFFFFE6C – Memory Fine Base Address Low Register 13

Address FFFFFE74 – Memory Fine Base Address Low Register 14

Address FFFFFE7C – Memory Fine Base Address Low Register 15

Address FFFFFE84 – Memory Fine Base Address Low Register 16

Figure 4-255. Memory Fine Base Address Low Register 4-16 (MFBALRx)

15	10	9	8	2	1	0
ADDRESS[15:10]		AW	Reserved		RONLY	PRIV
R/W-00 0000		R/W-0	R/W-000 0000		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-255. Memory Fine Base Address Low Register 4-17 (MFBALRx) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	ADDRESS[15:10]	R/W	00 0000	6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.
9	AW	R/W	0	Auto-wait-on-write. When this bit is set, any write operation on this memory select takes two system cycles. 0 = Write operation is not supplemented with an additional cycle (Default) 1 = Write operation takes an additional cycle
8-2	Reserved	R/W	000 0000	
1	RONLY	R/W	0	Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory. 0 = Read/write access to memory (Default) 1 = Read accesses to memory only
0	PRIV	R/W	0	Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode. 0 = User/privilege mode accesses to memory (Default) 1 = Privilege mode accesses to memory only

4.16.7 Memory Fine Base Address High Register 5 (MFBAHR5)

Address FFFFFE28 – Memory Fine Base Address High Register 5

Figure 4-256. Memory Fine Base Address High Register 5 (MFBAHR5)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 0011	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-256. Memory Fine Base Address High Register 5 (MFBAHR5) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 0011	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.8 Memory Fine Base Address High Register 6 (MFBAHR6)

Address FFFFFE30 – Memory Fine Base Address High Register 6

Figure 4-257. Memory Fine Base Address High Register 6 (MFBAHR6)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 0100	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-257. Memory Fine Base Address High Register 6 (MFBAHR6) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 0100	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.9 Memory Fine Base Address High Register 7 (MFBAHR7)

Address FFFFFE38 – Memory Fine Base Address High Register 7

Figure 4-258. Memory Fine Base Address High Register 7 (MFBAHR7)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 0101	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-258. Memory Fine Base Address High Register 7 (MFBAHR7) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 0101	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.10 Memory Fine Base Address High Register 8 (MFBAHR8)

Address FFFFFE40 – Memory Fine Base Address High Register 8

Figure 4-259. Memory Fine Base Address High Register 8 (MFBAHR8)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 0110	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-259. Memory Fine Base Address High Register 8 (MFBAHR8) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 0110	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.11 Memory Fine Base Address High Register 9 (MFBAHR9)

Address FFFFFE48 – Memory Fine Base Address High Register 9

Figure 4-260. Memory Fine Base Address High Register 9 (MFBAHR9)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 0111	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-260. Memory Fine Base Address High Register 9 (MFBAHR9) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 0111	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.12 Memory Fine Base Address High Register 10 (MFBAHR10)

Address FFFFFE50 – Memory Fine Base Address High Register 10

Figure 4-261. Memory Fine Base Address High Register 10 (MFBAHR10)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 1000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-261. Memory Fine Base Address High Register 10 (MFBAHR10) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 1000	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.13 Memory Fine Base Address High Register 11 (MFBAHR11)

Address FFFFFE58 – Memory Fine Base Address High Register 11

Figure 4-262. Memory Fine Base Address High Register 11 (MFBAHR11)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 1001	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-262. Memory Fine Base Address High Register 11 (MFBAHR11) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 1001	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.14 Memory Fine Base Address High Register 12 (MFBAHR12)

Address FFFFFE60 – Memory Fine Base Address High Register 12

Figure 4-263. Memory Fine Base Address High Register 12 (MFBAHR12)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 1010	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-263. Memory Fine Base Address High Register 12 (MFBAHR12) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 1010	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.15 Memory Fine Base Address High Register 13 (MFBAHR13)

Address FFFFFE68 – Memory Fine Base Address High Register 13

Figure 4-264. Memory Fine Base Address High Register 13 (MFBAHR13)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 1011	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-264. Memory Fine Base Address High Register 13 (MFBAHR13) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 1011	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.16 Memory Fine Base Address High Register 14 (MFBAHR14)

Address FFFFFE70 – Memory Fine Base Address High Register 14

Figure 4-265. Memory Fine Base Address High Register 14 (MFBAHR14)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 1100	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-265. Memory Fine Base Address High Register 14 (MFBAHR14) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0000 1100	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.17 Memory Fine Base Address High Register 15 (MFBAHR15)

Address FFFFFE78 – Memory Fine Base Address High Register 15

Figure 4-266. Memory Fine Base Address High Register 15 (MFBAHR15)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 1101	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-266. Memory Fine Base Address High Register 15 (MFBAHR15) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 1101	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.18 Memory Fine Base Address High Register 16 (MFBAHR16)

Address FFFFFE80 – Memory Fine Base Address High Register 16

Figure 4-267. Memory Fine Base Address High Register 16 (MFBAHR16)

15	0
ADDRESS[31:16]	
R/W-0000 0000 0001 1110	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-267. Memory Fine Base Address High Register 16 (MFBAHR16) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDRESS[31:16]	R/W	0000 0000 0001 1110	16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

4.16.19 Program Flash Control Register (PFLASHCTRL)

Address FFFFFE90 - PFLASHCTRL_0

Address FFFFFE9C - PFLASHCTRL_1

Address FFFFFEA0 - PFLASHCTRL_2

Address FFFFFEA4 - PFLASHCTRL_3

Figure 4-268. Program Flash Control Register (PFLASHCTRL)

11	10	9	8	7 5	4 0
BUSY	Reserved	PAGE_ ERASE	MASS_ ERASE	Reserved	PAGE_SEL
R-0	R-0	R/W-0	R/W-0	R-000	R-00000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-268. Program Flash Control Register (PFLASHCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
11	BUSY	R	0	Program Flash Busy Indicator 0 = Program Flash available for read/write/erase access 1 = Program Flash unavailable for read/write/erase access
10	Reserved	R	0	
9	PAGE_ERASE	R/W	0	Program Flash Page Erase Enable 0 = No Page Erase initiated on Program Flash (Default) 1 = Page Erase on Program Flash enabled. Page erased is based on PAGE_SEL (Bits 4-0). Interlock Key must be set in Program Flash Interlock Register () to initiate Page Erase cycle. This bit is cleared upon completion of Page Erase cycle.
8	MASS_ERASE	R/W	0	Program Flash Mass Erase Enable 0 = No Mass Erase initiated on Program Flash (Default) 1 = Mass Erase of Program Flash enabled. Interlock Key must be set in Program Flash Interlock Register () to initiate Mass Erase cycle. This bit is cleared upon completion of Mass Erase cycle.
7-5	Reserved	R	000	
4-0	PAGE_SEL	R	00000	Selects page to be erased during Page Erase Cycle

4.16.20 Data Flash Control Register (DFLASHCTRL)

Address FFFFFE94

Figure 4-269. Data Flash Control Register (DFLASHCTRL)

11	10	9	8	7	6	5	0
BUSY	Reserved	PAGE_ ERASE	MASS_ ERASE	Reserved		PAGE_SEL	
R-0	R-0	R/W-0	R/W-0	R-0		R/W-000000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-269. Data Flash Control Register (DFLASHCTRL) Register Field Descriptions

Bit	Field	Type	Reset	Description
11	BUSY	R	0	Data Flash Busy Indicator 0 = Data Flash available for read/write/erase access 1 = Data Flash unavailable for read/write/erase access
10	Reserved	R	0	
9	PAGE_ERASE	R/W	0	Data Flash Page Erase Enable 0 = No Page Erase initiated on Data Flash (Default) 1 = Page Erase Cycle on Data Flash enabled. Page erased is based on PAGE_SEL (Bits 4-0). This bit is cleared upon completion of Page Erase cycle.
8	MASS_ERASE	R/W	0	Data Flash Mass Erase Enable 0 = No Mass Erase initiated on Data Flash (Default) 1 = Mass Erase of Data Flash enabled. Bit is cleared upon completion of mass erase.
7-6	Reserved	R	0	
5-0	PAGE_SEL	R/W	000000	Selects page to be erased during Page Erase Cycle

4.16.21 Flash Interlock Register (FLASHILOCK)

Address FFFFFE98

Figure 4-270. Flash Interlock Register (FLASHILOCK)

31	0
INTERLOCK_KEY	
R/W-0000 0000 0000 0000 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-270. Flash Interlock Register (FLASHILOCK) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INTERLOCK_KEY	R/W	0000 0000 0000 0000 0000 0000 0000 0000	Flash Interlock Key. Register must be set to: 0x42DC157E prior to every Data Flash write/mass erase/page erase or 0x42DC157E prior to every Program Flash#0 write/mass erase/page erase or 0x6C97D0C5 prior to every Program Flash#1 write/mass erase/page erase or 0x184219B3 prior to every Program Flash#2 write/mass erase/page erase or 0x5973EF21 prior to every Program Flash#3 write/mass erase/page erase. If the Interlock Key is not set, the write/erase cycle to the Flash will not initiate. This register will clear upon the completion of a write/erase cycle to the Flash modules.

4.17 CIM – Central Interrupt Module

CIM Registers have the following attributes:

- 32-bit width
- Addresses placed on word boundaries
- Byte, half-word and word writes permitted
- All Registers have read/write access in any mode
- Interrupt Mask and FIQ/IRQ Program Control Registers are writeable in privilege mode only. A write in user mode to these Registers causes a peripheral illegal access exception.

4.17.1 IRQ Index Offset Vector Register (IRQIVEC)

Address FFFFFF20

Figure 4-271. IRQ Index Offset Vector Register (IRQIVEC)

7							0
IRQIVEC							
R-0							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-271. IRQ Index Offset Vector Register (IRQIVEC) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IRQIVEC	R	0	Index of the highest priority IRQ interrupt pending. (Higher interrupt numbers have higher priority) 0 = No interrupt pending 1 = Pending interrupt on Channel 0 2 = Pending interrupt on Channel 1 N = Pending interrupt on Channel N-1, where N <= 31

4.17.2 FIQ Index Offset Vector Register (FIQIVEC)

Address FFFFFF24

Figure 4-272. FIQ Index Offset Vector Register (FIQIVEC)

7							0
FIQIVEC							
R-0							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-272. FIQ Index Offset Vector Register (FIQIVEC) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIQIVEC	R	0	Index of the highest priority FIQ interrupt pending. (Higher interrupt numbers have higher priority) 0 = No interrupt pending 1 = Pending interrupt on Channel 0 2 = Pending interrupt on Channel 1 N = Pending interrupt on Channel N-1, where N <= 31

4.17.3 FIQ/IRQ Program Control Register (FIRQPR)

Address FFFFFF2C

A 32-bit FIQ/IRQ program control Register (FIRQPR) determines whether a given interrupt request will be FIQ or IRQ type.

Figure 4-273. FIQ/IRQ Program Control Register (FIRQPR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXT_FAULT_INT	SYS_SSI_INT	DPWM0_INT	DPWM1_INT	DPWM2_INT	DPWM3_INT	FAULT_MUX_INT	ADC_INT	CPCC_RTC_INT	T24_OC0_INT	T24_CAP0_INT	T24_OC1_INT	T24_CAP1_DTC_INT	T24_OVF	T16_PWM0_INT	T16_PWM1_INT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T16_PWM2_INT	T16_PWM3_INT	FE2_INT	FE1_INT	FE0_INT	DCOMP_I2C_SPI_INT	PMBUS_INT	UART1_TX_INT	UART1_RX_INT	UART0_TX_INT	UART0_RX_INT	UART_0_1_ERR_INT	WD_WAKE_INT	WD_FULL_INT	EXT_INT	BROWNOUT_INT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-273. FIQ/IRQ Program Control Register (FIRQPR) Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EXT_FAULT_INT	R/W	0	External Fault Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
30	SYS_SSI_INT	R/W	0	SYS SSI Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
29	DPWM0_INT	R/W	0	DPWM0 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
28	DPWM1_INT	R/W	0	DPWM1 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
27	DPWM2_INT	R/W	0	DPWM2 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
26	DPWM3_INT	R/W	0	DPWM3 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
25	FAULT_MUX_INT	R/W	0	Fault Mux Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
24	ADC_INT	R/W	0	ADC12 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
23	CPCC_RTC_INT	R/W	0	CPCC/RTC Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
22	T24_OC0_INT	R/W	0	24-bit Output Compare 0 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type

Table 4-273. FIQ/IRQ Program Control Register (FIRQPR) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	T24_CAP0_INT	R/W	0	24-bit Timer Capture Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
20	T24_OC1_INT	R/W	0	24-bit Output Compare 1 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
19	T24_CAP1_DTC_INT	R/W	0	24-bit Timer CAP1/DTC Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
18	T24_OVF	R/W	0	24-bit Timer Overflow Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
17	T16_PWM0_INT	R/W	0	16-bit Timer 0 PWM Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
16	T16_PWM1_INT	R/W	0	16-bit Timer 1 PWM Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
15	T16_PWM2_INT	R/W	0	16-bit Timer 2 PWM Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
14	T16_PWM3_INT	R/W	0	16-bit Timer 3 PWM Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
13	FE2_INT	R/W	0	Front End 2 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
12	FE1_INT	R/W	0	Front End 1 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
11	FE0_INT	R/W	0	Front End 0 Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
10	DCOMP_I2C_SPI_INT	R/W	0	Digital Comparator/I2C/SPI Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
9	PMBUS_INT	R/W	0	PMBus Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
8	UART1_TX_INT	R/W	0	UART1TX Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
7	UART1_RX_INT	R/W	0	UART1RX Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
6	UART0_TX_INT	R/W	0	UART0 TX Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type

Table 4-273. FIQ/IRQ Program Control Register (FIRQPR) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	UART0_RX_INT	R/W	0	UART0 RX Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
4	UART_0_1_ERR_INT	R/W	0	UART0/1 ERR Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
3	WD_WAKE_INT	R/W	0	Watchdog Half Count Reached Interrupt Request 0 = Interrupt request is of IRQ type (Default)
2	WD_FULL_INT	R/W	0	Watchdog Max Count Reached Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
1	EXT_INT	R/W	0	External Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type
0	BROWNOUT_INT	R/W	0	Brownout Interrupt Request 0 = Interrupt request is of IRQ type (Default) 1 = Interrupt request is of FIQ type

4.17.4 Pending Interrupt Read Location Register (INTREQ)

Address FFFFFF30

Figure 4-274. Pending Interrupt Read Location Register (INTREQ)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXT_FAULT_INT	SYS_SSI_INT	DPWM0_INT	DPWM1_INT	DPWM2_INT	DPWM3_INT	FAULT_MUX_INT	ADC_INT	CPCC_RTC_INT	T24_OC0_INT	T24_CAP_INT	T24_OC1_INT	T24_CAP1_DTC_INT	T24_OVF	T16_PWM0_INT	T16_PWM1_INT
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T16_PWM2_INT	T16_PWM3_INT	FE2_INT	FE1_INT	FE0_INT	DCOMP_I2C_SPI_INT	PMBUS_INT	UART1_TX_INT	UART1_RX_INT	UART0_TX_INT	UART0_RX_INT	UART_0_1_ERR_INT	WD_WAKE_INT	WD_FULL_INT	BROWNOUT_INT	BROWNOUT_INT
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-274. Pending Interrupt Read Location Register (INTREQ) Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EXT_FAULT_INT	R	X	External Fault Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
30	SYS_SSI_INT	R	X	SYS SSI Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
29	DPWM0_INT	R	X	DPWM0 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
28	DPWM1_INT	R	X	DPWM1 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
27	DPWM2_INT	R	X	DPWM2 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
26	DPWM3_INT	R	X	DPWM3 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
25	FAULT_MUX_INT	R	X	Fault Mux Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
24	ADC_INT	R	X	ADC12 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
23	CPCC_RTC_INT	R	X	CPCC/RTC Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
22	T24_OC0_INT	R	X	24-bit Output Compare 0 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
21	T24_CAP_INT	R	X	24-bit Timer Capture Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending

Table 4-274. Pending Interrupt Read Location Register (INTREQ) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	T24_OC1_INT	R	X	24-bit Output Compare 1 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
19	T24_CAP1_DTC_INT	R	X	24-bit Timer CAP1/DTC Interrupt 0 = No interrupt has occurred 1 = Interrupt is pending
18	T24_OVF	R	X	24-bit Timer Overflow Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
17	T16_PWM0_INT	R	X	16-bit Timer 0 PWM Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
16	T16_PWM1_INT	R	X	16-bit Timer 1 PWM Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
15	T16_PWM2_INT	R	X	16-bit Timer 2 PWM Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
14	T16_PWM3_INT	R	X	16-bit Timer 3 PWM Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
13	FE2_INT	R	X	Front End 2 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
12	FE1_INT	R	X	Front End 1 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
11	FE0_INT	R	X	Front End 0 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
10	DCOMP_I2C_SPI_INT	R	X	Digital Comparator/I2C/SPI Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
9	PMBUS_INT	R	X	PMBus Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
8	UART1_TX_INT	R	X	UART1RX Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
7	UART1_RX_INT	R	X	UART1RX Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
6	UART0_TX_INT	R	X	UART0 TX Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
5	UART0_RX_INT	R	X	UART0 RX Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending

Table 4-274. Pending Interrupt Read Location Register (INTREQ) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	UART_0_1_ERR_INT	R	X	UART0/1 ERR Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
3	WD_WAKE_INT	R	X	Watchdog Half Count Reached Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
2	WD_FULL_INT	R	X	Watchdog Max Count Reached Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
1	EXT_INT	R	X	External Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
0	BROWNOUT_INT	R	X	Brownout Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending

4.17.5 Interrupt Mask Register (REQMASK)

Address FFFFFF34

Figure 4-275. Interrupt Mask Register (REQMASK)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXT_FAULT_INT	SYS_SSI_INT	DPWM0_INT	DPWM1_INT	DPWM2_INT	DPWM3_INT	FAULT_MUX_INT	ADC_INT	CPCC_RTC_INT	T24_OC0_INT	T24_CAP_INT	T24_OC1_INT	T24_CAP1_DTC_INT	T24_OVF	T16_PWM0_INT	T16_PWM1_INT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T16_PWM2_INT	T16_PWM3_INT	FE2_INT	FE1_INT	FE0_INT	DCOMP_I2C_SPI_INT	PMBUS_INT	UART1_TX_INT	UART1_RX_INT	UART0_TX_INT	UART0_RX_INT	UART_0_1_ERR_INT	WD_WAKE_INT	WD_FULL_INT	BROWNOUT_INT	BROWNOUT_INT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-275. Interrupt Mask Register (REQMASK) Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EXT_FAULT_INT	R/W	0	External Fault Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
30	SYS_SSI_INT	R/W	0	SYS SSI Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
29	DPWM0_INT	R/W	0	DPWM0 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
28	DPWM1_INT	R/W	0	DPWM1 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
27	DPWM2_INT	R/W	0	DPWM2 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
26	DPWM3_INT	R/W	0	DPWM3 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
25	FAULT_MUX_INT	R/W	0	Fault Mux Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
24	ADC_INT	R/W	0	ADC12 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
23	CPCC_RTC_INT	R/W	0	CPCC/RTC Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
22	T24_OC0_INT	R/W	0	24-bit Output Compare 0 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
21	T24_CAP_INT	R/W	0	24-bit Timer Capture Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending

Table 4-275. Interrupt Mask Register (REQMASK) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	T24_OC1_INT	R/W	0	24-bit Output Compare 1 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
19	T24_CAP1_DTC_INT	R/W	0	24-bit Timer CAP1/DTC Interrupt 0 = No interrupt has occurred 1 = Interrupt is pending
18	T24_OVF	R/W	0	24-bit Timer Overflow Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
17	T16_PWM0_INT	R/W	0	16-bit Timer 0 PWM Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
16	T16_PWM1_INT	R/W	0	16-bit Timer 1 PWM Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
15	T16_PWM2_INT	R/W	0	16-bit Timer 2 PWM Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
14	T16_PWM3_INT	R/W	0	16-bit Timer 3 PWM Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
13	FE2_INT	R/W	0	Front End 2 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
12	FE1_INT	R/W	0	Front End 1 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
11	FE0_INT	R/W	0	Front End 0 Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
10	DCOMP_I2C_SPI_INT	R/W	0	Digital Comparator/I2C/SPI Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
9	PMBUS_INT	R/W	0	PMBus Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
8	UART1_TX_INT	R/W	0	UART1RX Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
7	UART1_RX_INT	R/W	0	UART1RX Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
6	UART0_TX_INT	R/W	0	UART0 TX Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
5	UART0_RX_INT	R/W	0	UART0 RX Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending

Table 4-275. Interrupt Mask Register (REQMASK) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	UART_0_1_ERR_INT	R/W	0	UART0/1 ERR Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
3	WD_WAKE_INT	R/W	0	Watchdog Half Count Reached Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
2	WD_FULL_INT	R/W	0	Watchdog Max Count Reached Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
1	EXT_INT	R/W	0	External Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending
0	BROWNOUT_INT	R/W	0	Brownout Interrupt Request 0 = No interrupt has occurred 1 = Interrupt is pending

4.18 SYS – System Module

SYS Registers have the following attributes:

- 16-bit wide
- Addresses placed on word boundaries
- Byte, half-word and word writes permitted
- All Registers can be read in any mode of operation.
- Global Control Register is writeable in privilege mode only. All other Registers are writeable in any mode.

4.18.1 Clock Control Register (CLKCNTL)

Address FFFFFFD0

The clock control Register configures the MCLK divider for low power modes and the clock multiplexer which drives the Sync pin when configured to output the CLKOUT signal. CLKCNTRL is accessible in user and privilege mode and supports byte, half-word and word accesses. Any access to this Register takes two SYSCLK cycles. Note that the performance of peripherals is not guaranteed at M_DIV_RATIO settings other than the default.

Figure 4-276. Clock Control Register (CLKCNTL)

9 8	7	6 5	4	3	2 0
M_DIV_RATIO	Reserved	CLKSR	Reserved	CLKDOUT	Reserved
R-00	R-0	R/W-00	R-0	R/W-0	R-000

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 4-276. Clock Control Register (CLKCNTL) Register Field Descriptions

Bit	Field	Type	Reset	Description
9-8	M_DIV_RATIO	R	00	MCLK (Processor Clock) Divide Ratio 00 = MCLK frequency equals High Frequency Oscillator divided by 8 (Default) 01 = MCLK frequency equals High Frequency Oscillator divided by 16 10 = MCLK frequency equals High Frequency Oscillator divided by 32 11 = MCLK frequency equals High Frequency Oscillator divided by 64
7	Reserved	R	0	
6-5	CLKSR	R/W	00	These bits control the source/function of CLKOUT 00 = Driven by value in CLKDOUT (Bit 3) (Default) 01 = Driven by the interface clock (ICLK) 10 = Driven by the CPU clock (MCLK) 11 = Driven by the system clock (SYSCLK)
4	Reserved	R	0	
3	CLKDOUT	R/W	0	This pin represents the output value of CLKOUT 0 = CLKOUT driven to logic low in output mode (Default) 1 = CLKOUT driven to logic high in output mode
2-0	Reserved	R	000	

4.18.2 System Exception Control Register (SYSECR)

Address FFFFFFE0

The system exception control Register contains bits that allow the user to generate a software reset. The OVR bits disable some reset/abort conditions when TRST is high.

Figure 4-277. System Exception Control Register (SYSECR)

15	14	13	8
RESET		Reserved	
R/W-01		R-0	

7	3	2	1	0
Reserved		PACCOVR	ACCOVR	ILLOVR
R-0		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-277. System Exception Control Register (SYSECR) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESET	R/W	01	Software Reset Enable. These bits always read as 01 01 = No reset 1X = Global system reset (X = don't care) X0 = Global system reset (X = don't care)
13-3	Reserved	R	0	
2	PACCOVR	R/W	0	Peripheral Access Violation Override 0 = Peripheral access violation error causes a reset or abort (Default) 1 = No action taken on a peripheral access violation
1	ACCOVR	R/W	0	Memory Access Reset Override 0 = Memory access violation error causes a reset or abort (Default) 1 = No action taken on an illegal address
0	ILLOVR	R/W	0	Illegal Address Reset Override 0 = Illegal address causes a reset or abort (Default) 1 = No action taken on an illegal address

4.18.3 System Exception Status Register (SYSESR)

Address FFFFFFE4

The System Exception Status Register contains flags for different reset/abort sources. On power-up, all bits are cleared to 0. When a reset condition is recognized, the appropriate bit in the Register is set and the value of the bit is maintained through the reset. When a new reset condition occurs, the current contents of this Register are not cleared. The contents of this Register are cleared on a power-on reset or by software.

Figure 4-278. System Exception Status Register (SYSESR)

15	14	13	12	11	10	9	8
PORRST	CLKRST	WDRST	ILLMODE	ILLADR	ILLACC	PILLACC	ILLMAP
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6						0
SWRST	Reserved						
R/W-0	R-000 0000						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-278. System Exception Status Register (SYSESR) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PORRST	R/W	0	Power-On reset flag. Set when power-on reset is asserted. Reset is asserted as long as power-on-reset is active. Whenever a device is powered, this bit is set. User and privilege modes (read 0 = Power-up reset has not occurred since the last clear 1 = Power-up reset has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect
14	CLKRST	R/W	0	This bit represents the clock fail flag. This bit indicates a clock fault condition has occurred. After power-on-reset, the CLKRST is reset to 0. Value remains unchanged during other resets. User and privilege modes (read) 0 = Clock failure has not occurred since the last clear 1 = Clock failure has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect
13	WDRST	R/W	0	This bit represents the watchdog reset flag. This bit indicates that the last reset was caused by the watchdog. User and privilege modes (read 0 = Watchdog reset has not occurred since the last clear 1 = Watchdog reset has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect
12	ILLMODE	R/W	0	This bit represents the illegal mode flag. This bit is set when the mode bits in the program status Register are set to an illegal value. User and privilege modes (read) 0 = Illegal mode has not occurred since the last clear 1 = Illegal mode has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect

Table 4-278. System Exception Status Register (SYSESR) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ILLADR	R/W	0	This bit represents the illegal address access flag. This bit is set when an access to an unimplemented location in the memory map is detected in non-user mode. User and privilege modes (read) 0 = Illegal address has not occurred since the last clear 1 = Illegal address has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect
10	ILLACC	R/W	0	This bit represents the illegal memory access flag. This bit is set when an access to a protected location without permission rights is detected in non-user mode. User and privilege modes (read) 0 = Illegal memory access has not occurred since the last clear 1 = Illegal memory access has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect
9	PILLACC	R/W	0	This bit represents the peripheral illegal access flag. This bit is set when a peripheral access violation is detected in user mode. User and privilege modes (read) 0 = Illegal peripheral access has not occurred since the last clear 1 = Illegal peripheral access has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect
8	ILLMAP	R/W	0	This bit represents the illegal address map flag. This bit is set when the base addresses of one or more memories overlap. Reset occurs when the overlapped registration is accessed. User and privilege modes (read) 0 = Illegal address mapping has not occurred since the last clear 1 = Illegal address mapping has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect
7	SWRST	R/W	0	This bit represents the software reset flag. This bit is set when the last reset is caused by software writing the RESET bits. User and privilege modes (read) 0 = Software reset has not occurred since the last clear 1 = Software reset has occurred since the last clear User and privilege modes (write) 0 = Clears the corresponding bit to 0 1 = No effect
6-0	Reserved	R	000 0000	

4.18.4 Abort Exception Status Register (ABRTESR)

Address FFFFFFE8

The Abort Exception Status Register shows the abort cause.

Figure 4-279. Abort Exception Status Register (ABRTESR)

15	14	13	12	8
ADRABT	MEMABT	PACCVIO	Reserved	
R/W-0	R/W-0	R/W-0	R-0 0000 0000 0000	
7				0
Reserved				
R-0 0000 0000 0000				

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-279. Abort Exception Status Register (ABRTESR) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ADRABT	R/W	0	is bit represents the illegal address abort. An illegal address access was detected in user mode. An abort was generated due to an illegal address access from either the MPU or system User and privilege modes (read) 0 = No illegal address 1 = Abort caused by an illegal address User and privilege modes (write) 0 = Clears bit to 0 1 = No effect
14	MEMABT	R/W	0	This bit represents the memory access abort. This bit indicates an illegal memory access was detected in user mode. An abort was generated due to the illegal memory access from either the MPU or system. User and privilege modes (read) 0 = No illegal memory access 1 = Abort caused by an illegal memory access User and privilege modes (write) 0 = Clears bit to 0 1 = No effect
13	PACCVIO	R/W	0	This bit represents the peripheral access violation error. This bit indicates a peripheral access violation error was detected during a peripheral Register access in user mode. An abort was generated due to a peripheral access violation. User and privilege modes (read) 0 = No peripheral access violation 1 = Abort caused by a peripheral access violation User and privilege modes (write) 0 = Clears bit to 0 1 = No effect
12-0	Reserved	R	0 0000 0000 0000	

4.18.5 Global Status Register (GLBSTAT)

Address FFFFFFEC

The Global Status Register specifies the module that triggered the illegal address, illegal access, abort or reset. When a new reset condition reset occurs, the current contents of this Register are not cleared. The contents of this Register are cleared on a power-on reset or by software.

Figure 4-280. Global Status Register (GLBSTAT)

7	6	5	4	3 – 0
SYSADDR	SYSACC	MPUADDR	MPUACC	Reserved
R/W-0	R/W-0	R/W-0	R/W-0	R-0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-280. Global Status Register (GLBSTAT) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SYSADDR	R/W	0	This bit represents the system illegal address flag. This bit is set when the system detects an illegal address. User and privilege modes (read) 0 = No system illegal address 1 = Abort or reset caused by a system illegal address User and privilege modes (write) 0 = Clears bit to 0 1 = No effect
6	SYSACC	R/W	0	This bit represents the system illegal access flag. This bit is set when the system detects an illegal access. User and privilege modes (read) 0 = No system illegal access 1 = Abort or reset caused by a system illegal access User and privilege modes (write) 0 = Clears bit to 0 1 = No effect
5	MPUADDR	R/W	0	This bit represents the MPU illegal address flag. This bit is set when the memory protection unit detects an illegal address. User and privilege modes (read) 0 = No MPU illegal address 1 = Abort or reset caused by a MPU illegal address User and privilege modes (write) 0 = Clears bit to 0 1 = No effect
4	MPUACC	R/W	0	This bit represents the MPU illegal access flag. This bit is set when the MPU detects an illegal access. User and privilege modes (read) 0 = No MPU illegal access 1 = Abort or reset caused by a MPU illegal access User and privilege modes (write) 0 = Clears bit to 0 1 = No effect
3-0	Reserved	R	0000	

4.18.6 Device Identification Register (DEV)

Address FFFFFFF0

The Device Identification Register contains device specification information that is hard coded during device manufacturing. This register is read-only.

Figure 4-281. Device Identification Register (DEV)

15	0
DEV	
R-0010 0100 0100 0111	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-281. Device Identification Register (DEV) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEV	R	0010 0100 0100 0111	These bits represent the device identification code.

4.18.7 System Software Interrupt Flag Register (SSIF)

Address FFFFFFF8

The System Software Interrupt Flag Register is set when a software interrupt is triggered. The flag allows the user to poll for a software interrupt.

Figure 4-282. System Software Interrupt Flag Register (SSIF)

0
SSIFLAG
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-282. System Software Interrupt Flag Register (SSIF) Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SSIFLAG	R/W	0	This bit represents the system software interrupt flag. This bit is set when a correct SSKEY is written to the System Software Interrupt Flag Register. This bit is cleared only by software.

4.18.8 System Software Interrupt Request Register (SSIR)

Address FFFFFFFC

The System Software Interrupt Request Register contains a key sequence that triggers a software interrupt request to the CIM. Also, the Register contains an 8-bit data field.

Figure 4-283. System Software Interrupt Request Register (SSIR)

15	8	7	0
SSKEY		SSDATA	
R/W-0000 0000		R/W-0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-283. System Software Interrupt Request Register (SSIR) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	SSKEY	R/W	0000 0000	These bits represent the system software interrupt request key. These write-only bits are executable in both user and privilege modes. A 0x75 written to these bits initiates IRQ/FIQ interrupts. Data in this field is always read as zero.
7-0	SSDATA	R/W	0000 0000	These bits represent the system software interrupt data. The SSDATA bits provide an 8-bit field that can be used for passing messages into the system software interrupt.

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