Functional Safety Information

TMP390-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TMP390-Q1 (SOT-563 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

TMP390-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the SOT-563 package of the TMP390-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor Control from table 11
- Power dissipation: 1.0mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog and Mixed =< 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TMP390-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTA false trip, fails to trip	20
OUTB false trip, fails to trip	20
OUTA functional trips at incorrect temperature	30
OUTB functional trips at incorrect temperature	30

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMP390-Q1 (SOT-563 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TMP390-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMP390-Q1 data sheet.

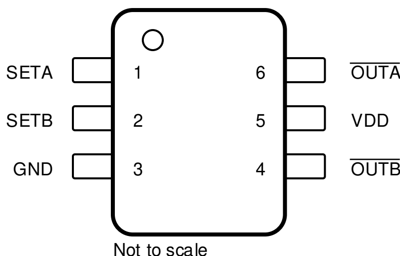

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is the only target on the I^{2}C bus
- External pull-up resistor on SCL and SDA pins

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SETA	1	SETA stuck low. Non-functional. False thermal limit triggers.	B
SETB	2	SETB stuck low. Non-functional. False thermal limit triggers.	B
GND	3	No effect. Normal operation.	D
OUTB	4	OUTB stuck low. Non-functional. False thermal limit triggers.	B
VDD	5	Device not powered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
OUTA	6	OUTA stuck low. Non-functional. False thermal limit triggers.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect	Failure Effect Class
SETA	1	SETA stuck open. OUTA trip point is undetermined. False thermal limit can trigger.	B
SETB	2	SETB stuck open. OUTB trip point is undetermined. False thermal limit can trigger.	B
GND	3	Device functionality undetermined. Device not powered or connect to ground internally through alternate pin ESD diode and power up.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect	Failure Effect Class
OUTB	4	OUTB stuck open. Non-functional. No thermal limit triggers.	B
VDD	5	Device functionality is undetermined. Device is not powered if all external analog and digital pins are held low. Device can power up through internal ESD diodes to V+ if voltages above the power-on reset threshold of the device are present on any of the analog or digital pins.	B
OUTA	6	OUTA stuck open. Non-functional. No thermal limit triggers.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect	Failure Effect Class
SETA	1	SETB	OUTA and OUTB trip point is undetermined. False thermal limit can trigger.	B
SETB	2	GND	SETB stuck low. Non-functional. False thermal limit triggers.	B
OUTB	3	VDD	OUTB stuck high. Non-functional. No thermal limit triggers.	B
VDD	4	OUTA	OUTA stuck high. Non-functional. No thermal limit triggers.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect	Failure Effect Class
SETA	1	SETA stuck high. OUTA trip point is undetermined. False thermal limit can trigger.	B
SETB	2	SETB stuck high. OUTB trip point is undetermined. False thermal limit can trigger.	B
GND	3	Device functionality undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
OUTB	4	OUTB stuck high. Non-functional. No thermal limit triggers.	B
VDD	5	No effect. Normal operation.	D
OUTA	6	OUTA stuck high. Non-functional. No thermal limit triggers.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (September 2024) **Page**

- Added the *Pin Failure Mode Analysis* section.. 5

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