
ADC0XD1520RB

Reference Board Users' Guide

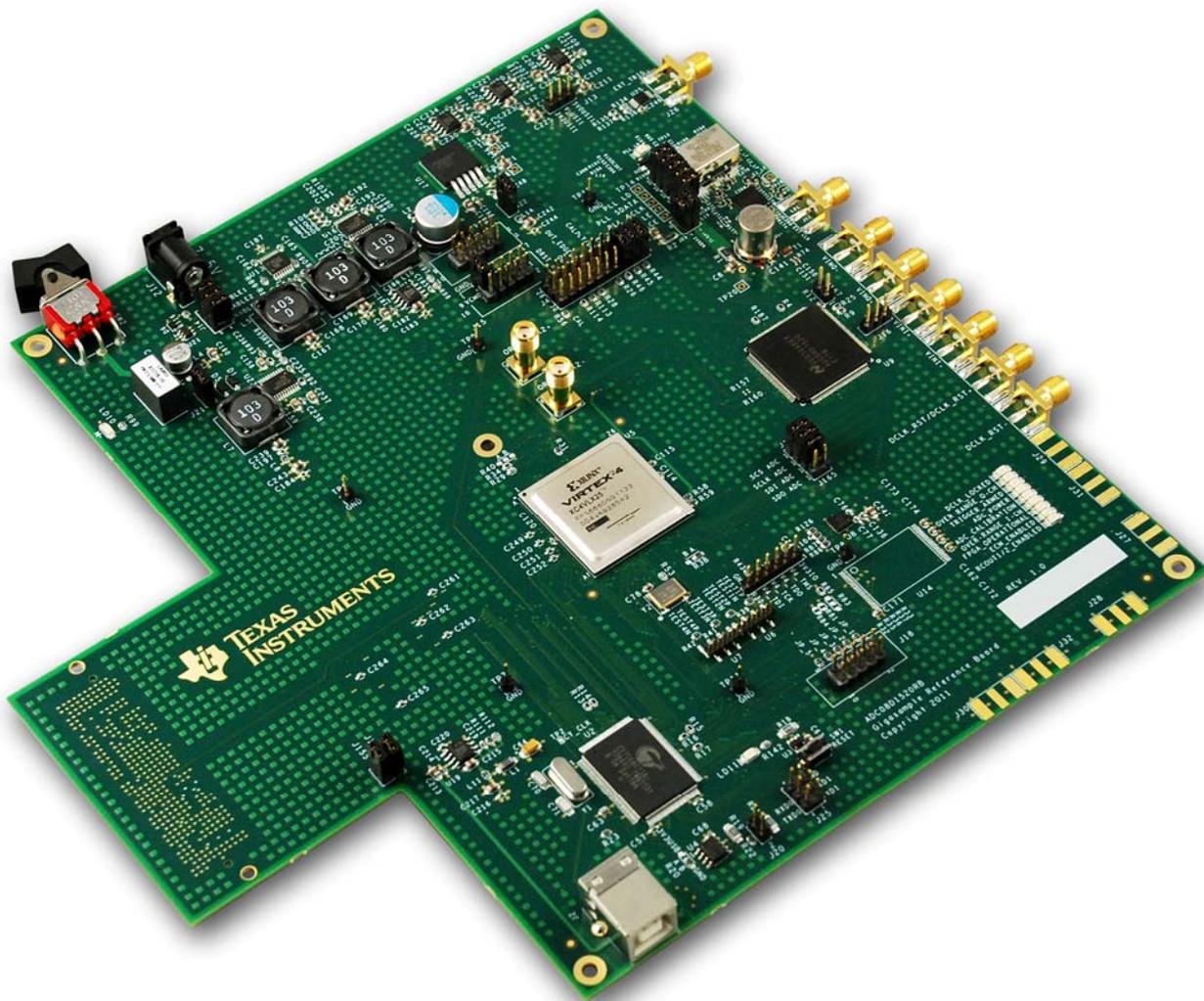


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1.0 Overview

The ADC0XD1520RB demonstrates a high-performance signal acquisition sub-system that achieves 7/8-bit resolution and corresponding SNR and dynamic range on two channels with sampling rates of at least 1.5 GS/s or one channel at a sampling rate of 3.0 GHz. The board showcases the following Texas Instruments devices:

- **ADC0XD1520** analog-to-digital converter
- **LMX2541** clock synthesizer
- **LP3878** and **LP38513-ADJ** linear LDO regulators
- **LM20242**, **LM25576** and **LM26400** switching regulators
- **LM3880** power sequencing controller
- **LM95233** temperature sensor

In addition, the board also employs the **Xilinx XC4VLX25-11FFG668 Virtex-4** FPGA for the critical function of capturing the high-speed digital data sourced by the ADC.

1.1 Features

- ❑ Demonstrates the ADC0XD1520's typical dynamic performance – see the datasheet for full details.
- ❑ Dual channel sample rates of up to 1.5 GS/s (limited by the ADC specifications and the FPGA capture limitations)
- ❑ Single channel (Interleaved) sample rates of up to 3.0 GS/s (limited by the ADC specifications and the FPGA capture limitations)
- ❑ FMC Expansion Header for streaming data capture
- ❑ External Hardware Trigger
- ❑ Updated Status LEDs
- ❑ On-board LMX2541 based clock circuit with a connector for a selectable external clock
- ❑ A complete high-performance low-noise power management section for the ADC, clock circuit, FPGA and USB controller
- ❑ Single +12V power adapter input
- ❑ Simplicity and performance of USB 2.0 connection to the PC
- ❑ Functions with TI's latest WaveVision 5 signal-path control and analysis software

1.2 Packing List

The ADC0XD1520RB kit consists of the following components:

- ADC0XD1520RB Reference Board
- Documentation on CD Including
 - ADC0XD1520RB Users Guide (this document)
 - Wavevision 5 Software
 - ADC0XD1520RB schematic & layout
 - ADC0XD1520RB bill of materials
 - ADC0XD1520RB performance plots
 - FPGA source code
 - Balun datasheets
- Hardware Kit Including
 - 110V-240V AC to +12V DC Power Adapter
 - USB cable
 - 4 – DC blocks
 - 2 – 50Ω terminators
 - 1 – ADC-Low Distortion-Balun Board (useful bandwidth of 400 MHz to 3 GHz)
 - 1 – ADC-Wide Band-Balun Board (useful bandwidth of 4.5 MHz to 3 GHz)
 - 4 – 6” SMA cables

1.3 References

- *ADC0XD1520 datasheet
- *LMX2541 datasheet

*Note: Please refer to www.ti.com for the latest edition of all datasheets / application notes.

1.4 Board Orientation

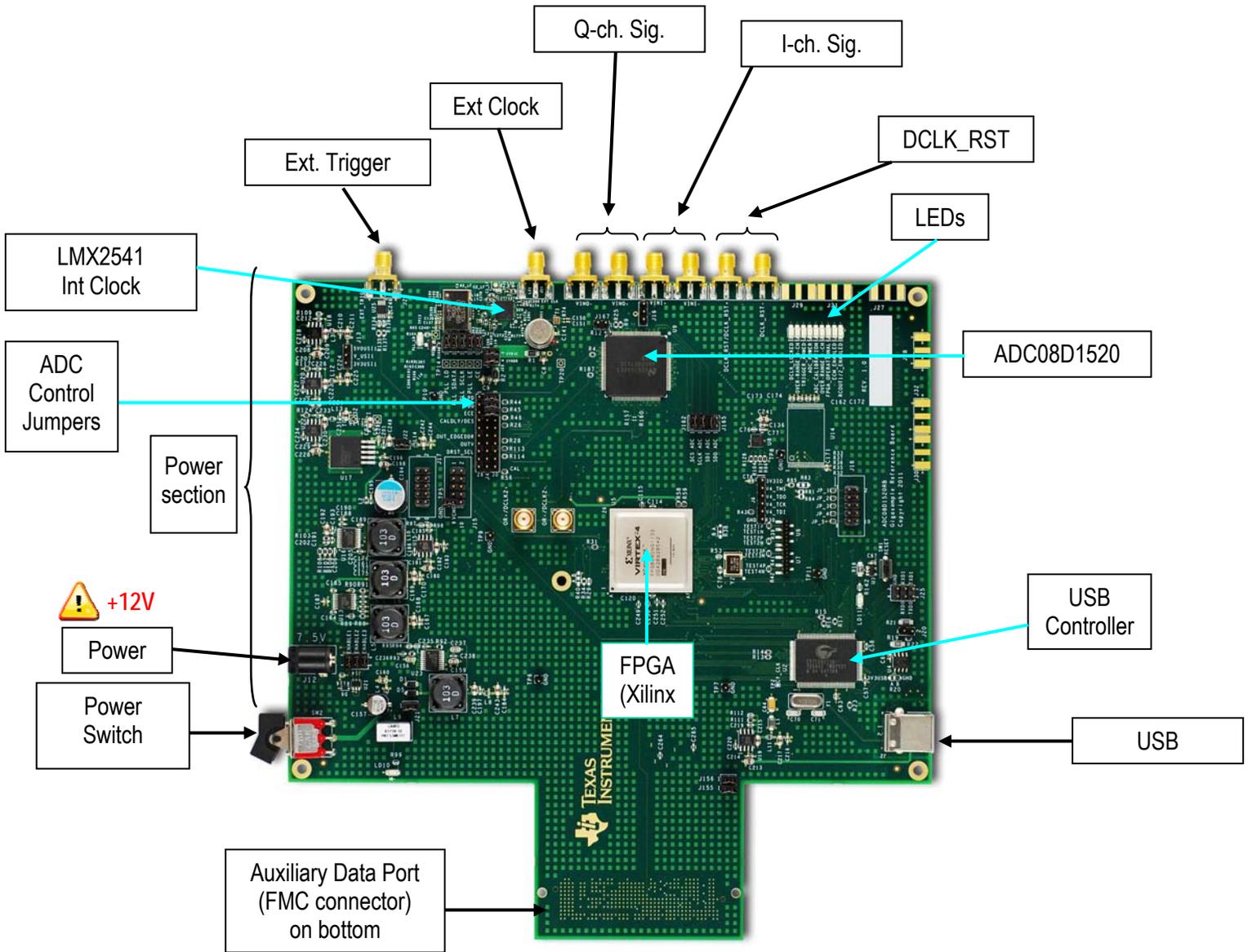


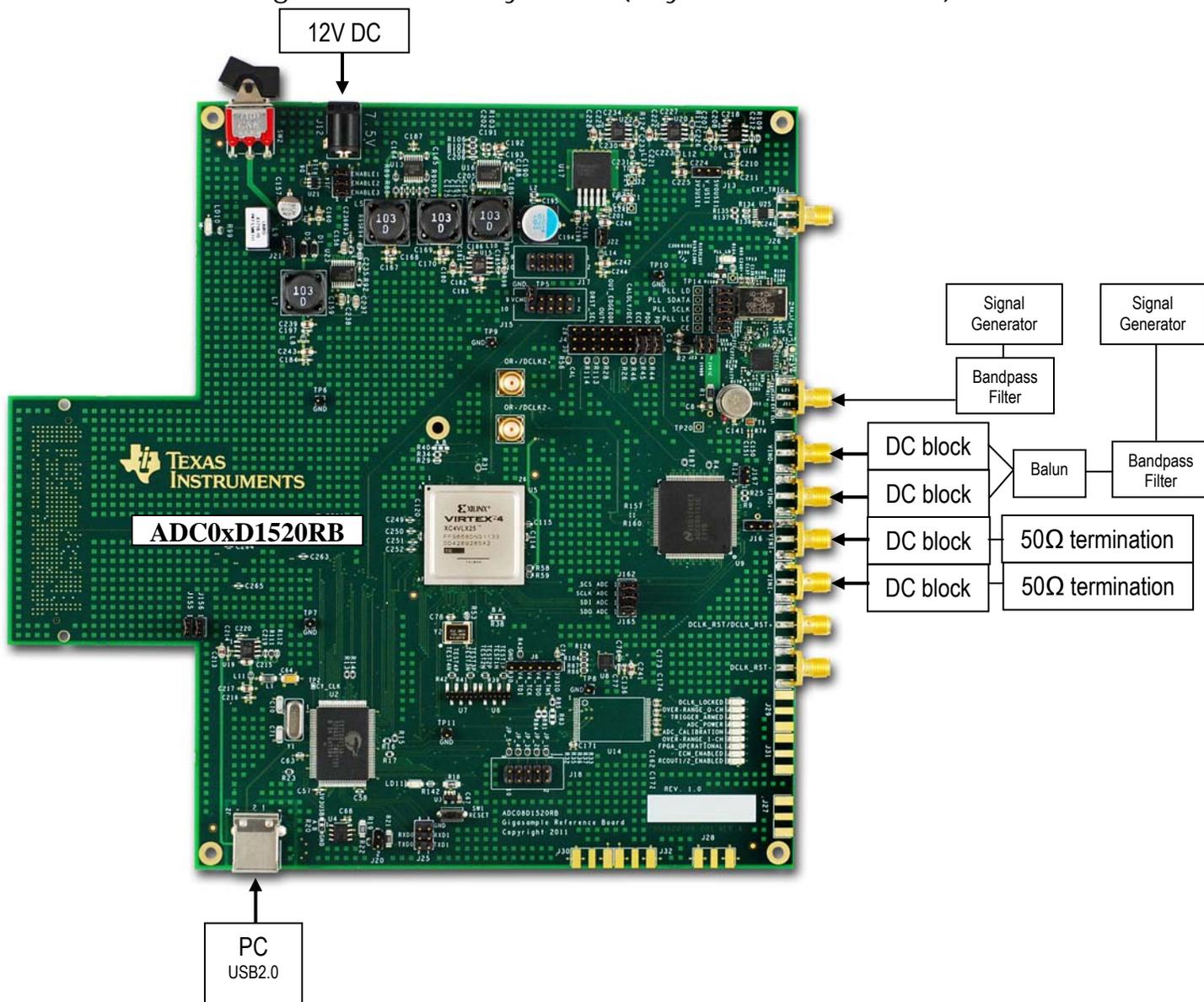
Figure 1: ADC0XD1520RB Board Layout

2.0 Quick Start

This section will aid in bringing up the board for the first time as well as a brief tutorial on the WaveVision 5 (WV5) software. Further description of the Reference Board is in subsequent sections of this document. The software is further described in the WaveVision 5 Users' Guide or the HELP function within the software. The ADC0XD1520 and LMX2541 datasheets should be consulted for detailed understanding of device functionality.

The user is advised to construct a lab setup as close to the one shown in Figure 2 as possible. This setup, along with the board and software configuration described below, is what was used to test the reference board at TI's lab. This set of conditions produces the stated reference performance - which is normally included with each board shipped to customers. The objective is to assure that the user can achieve the same performance as that recorded at TI's lab prior to board shipment.

Figure 2: Recommended lab setup. A filter may not be necessary on the clock if the generator is very clean (beyond -80dBm SFDR).



2.1 Installing the WaveVision 5 Software

1. Insert the included WaveVision 5 CD-ROM into the computer CD drive.
2. Locate, unzip and run the install.bat program on the CD-ROM.
3. Follow the on-screen instructions to complete the installation.
4. Follow the WaveVision 5 Software Driver Installation Guide from www.ti.com/tool/wavevision5 to install the required drivers for the ADC board. This typically involves manually installing them from the “driver” folder in the WaveVision 5 directory.

2.2 Installing the ADC0XD1520RB Hardware

1. Place the ADC0XD1520RB Reference Board on a clean, static-free surface.
2. For the ADC, the "ECE (Extended Control Enable, active low)" jumper should be installed in the LOW position. This enables SPI control of the ADC.
3. Pin 9 on J15 must be connected to Ground for ac-coupled operation. The board ships with this jumper in place as it is configured for ac-coupled operation only. (The jumper is removed for dc-coupled operation. In that case the applied signal must be dc-coupled, and have the common mode DC voltage set to the required ADC0XD1520 V_{CM} voltage.)
4. Connect the enclosed +12V DC power adapter to the power jack. Connect the other side of the power supply to an AC outlet (100-240 VAC, 50-60 Hz). Note that some earlier versions of the ADC08D1520RB may use a 7.5VDC source; the silk screen by the power connector is labeled.
5. Connect the input signal generator, the band-pass filter, the balun and the DC blocks to the ADC0XD1520RB Reference Board's I-channel input connectors. Set the signal generator at one of the frequencies and signal levels stated in the reference performance report. Always use high-quality RF SMA cables for optimum performance.



Do not overdrive the signal and clock inputs as the ADC may be damaged. Refer to the Electrical Specification section of the datasheet for the voltage tolerance of these inputs. Including insertion loss from filters, baluns, cables, DC blocks, etc. input power should not exceed operating limits as found in the datasheet.

6. In the TI lab, the following (or equivalent performance) equipment are used to test the board. It is essential that the customer use signal generators, filters, DC blocks and a balun of equivalent or better performance.
 - Rohde & Schwarz SME-03 or SMA-100 signal generator
 - Filters - Trilithic 5VF 5% tunable bandpass filter or other fixed frequency bandpass filter of equivalent performance
 - Balun – ADC-LD-BB
 - DC blocks – Mini Circuits BLK-89 S+
 - 50 Ω terminators – Mini Circuits ANNE 50+

Note: The board comes equipped with DC-blocks applied to the I-channel signal input connectors and DC blocks and terminators applied to the unused Q-channel input connectors. These must be used at all times - that is, the channel being used must be connected through dc-blocks if the ADC is configured for ac-coupled operation (as shipped). The unused channel must also be DC blocked then terminated to ac ground. This is graphically illustrated in Figure 2.
7. Turn on the SW2 rocker power switch. Verify that the green LED (labeled LD10, near the J12 power jack) is lit.
8. Connect the supplied USB 2.0 cable from the PC USB port to the ADC0XD1520RB USB jack.

2.3 Launch the WaveVision 5 Software.

Start the WaveVision 5 software on your computer by selecting the desktop icon “WaveVision 5” or by clicking on the Start button, and selecting

Start -> Programs -> WaveVision 5 -> WaveVision 5

The software will automatically detect the board and load the appropriate software profile and will proceed to download the controller firmware and FPGA code onto the reference board. As an alternative, the icon on the desktop can be used to launch WaveVision 5. The WaveVision 5 user interface will appear on the computer screen.

The status LED’s should take on the following states when the system is initially powered up, Wavevision 5 has loaded the FPGA image and the system is ready for an acquisition:

(Where green is *on*, black is *off*)

DCLK_LOCKED 
 OVER-RANGE_Q-CH 
 TRIGGER_ARMED 
 ADC_POWER 
 ADC_CALIBRATION 
 OVER-RANGE_I-CH 
 FPGA_OPERATIONAL 
 ECM_ENABLED 
 RCOUT1/2_ENABLED 

NOTE: The status LEDs are valid, only if the **FPGA_OPERATIONAL** LED is lit.

Meaning of the status LED’s:

- **DCLK_LOCKED**: If FPGA detects DCLKI and DCLKQ toggling, this LED lights.
- **TRIGGER_ARMED**: Lights when “H/W Trigger” is checked inside the Wavevision 5 GUI. Does not clear upon data capture.
- **ADC_POWER**: Lights when ADC supply voltage of 1.9V is detected.
- **ADC_CALIBRATION**: Will light temporarily when calibration is run. ADC’s CalRun pin is pulse stretched to about a half second.
- **OVER-RANGE**: ADC’s overrange I- or Q-ch pin pulse stretched to around a half second when overranged.
- **FPGA_OPERATIONAL**: Lights when FPGA’s 100MHz reference is locked and FPGA is out of reset.
- **ECM_ENABLED**: Lights when ADC is in Extended Control Mode.

2.4 WaveVision 5 - User Interface Overview

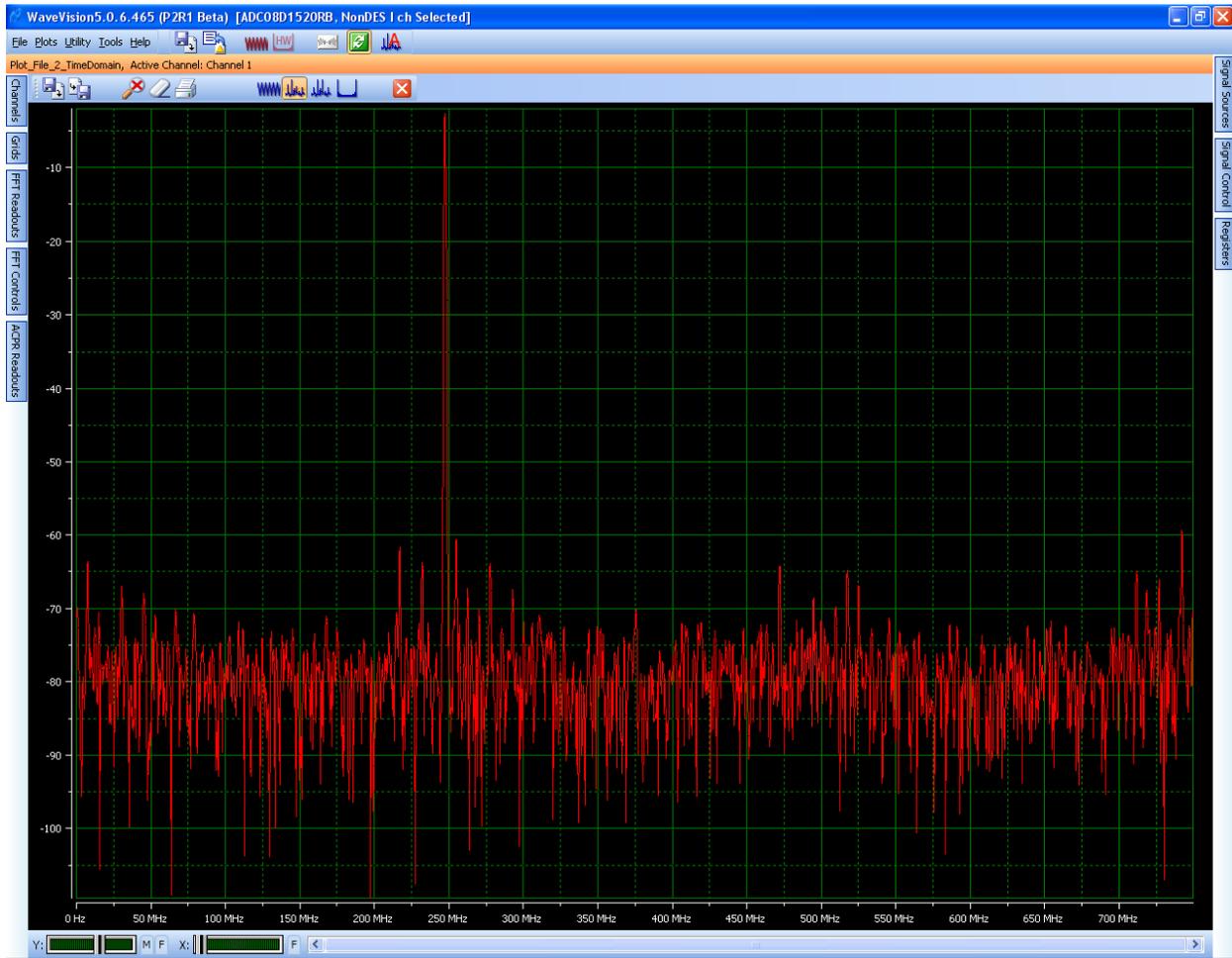


Figure 3: WaveVision 5 Example Window

Figure 3 above shows the WV5 user interface panel (GUI). This is the top level interface panel. It is arranged in such a way that the plot is always in the middle. There are tabs arranged on each side of the window to give the user additional information or control of features.

The tabs available on the **left side** access panels that are pertinent to the current plot window - such as *channel selection*, *grid selection*, *FFT Readouts*, and *FFT controls*.

The **right side** panels allow the user to take control of the hardware. These include the *Signal Source*, *Signal Control* and *Registers* panels (the most relevant for this board).

In addition, a small FFT parameter summary box can be displayed by pressing CTL-R.

For more details on the general operation and use of WaveVision 5, please refer to the **WaveVision 5 Users Guide**.

2.5 System / Device Configuration

Prior to capturing data, confirm that the board is in the "ECE (Extended Control Enable)" mode. The ECE jumper is located in the ADC pin control jumper area. The board should be sent with this jumper in place. This means that the ADC will be controlled through the SPI interface and not with jumpers driving the control pins. This allows the user to control the ADC's behavior through the WaveVision 5 Registers panel.



Figure 4: WaveVision 5 overview of control buttons

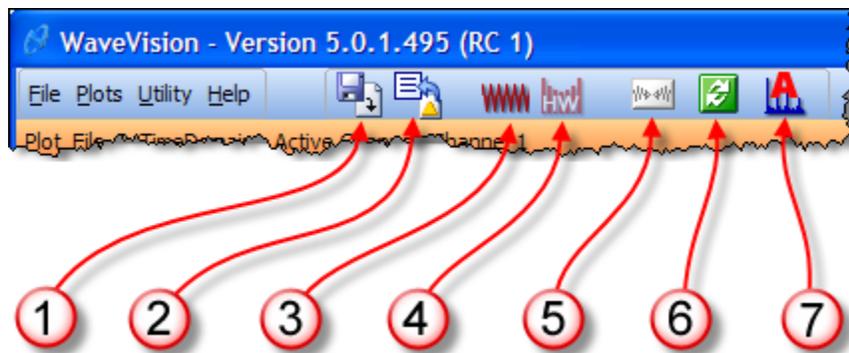


Figure 5: WaveVision 5 main window command buttons

2.5.1 Main Panel

The main menu bar of the WaveVision 5 software has several control buttons as shown in Figures 4 and 5, which may be used to perform most tasks with a button click.

1 - Load Plot

A new plot window is created and the Plot Load dialog is displayed. The selected plot file is loaded into the new window.

2 - Import Data

Clicking this button creates a new time-domain plot and opens the Import Data dialog. Data may be imported from WaveVision 4 data files as well as from ASCII data files created by other programs.

3 - Create a New Time Domain Plot

Clicking this button creates a new time-domain plot. The plot will contain no data, but is available as a data destination.

4 - Create a New Hardware Histogram Plot

Clicking this button creates a new hardware histogram plot. Hardware histograms are available only in conjunction with evaluation boards which can gather histogram data internally. This button is enabled only when an evaluation board which supports hardware histograms is attached.

5 - Acquire Data

Click this button to acquire data to the active plot. If you have created more than one plot, the Active plot has a highlighted title bar.

6 - Continuous Acquisition

This button is a toggle - when it is pressed, data is acquired continuously, one buffer after another as fast as the hardware can go; when pressed again data acquisition stops. When in continuous acquisition mode, acquisition may be started and stopped using the Acquire button without leaving the continuous acquisition mode.

7 - FFT Averaging

This button is also a toggle - when it is pressed, FFT's are averaged. The number of buffers to be averaged is specified in the hardware section of the Signal Sources tab.

Please refer to the **WaveVision 5 Users Guide** for more information.

2.5.2 Plot Window Controls

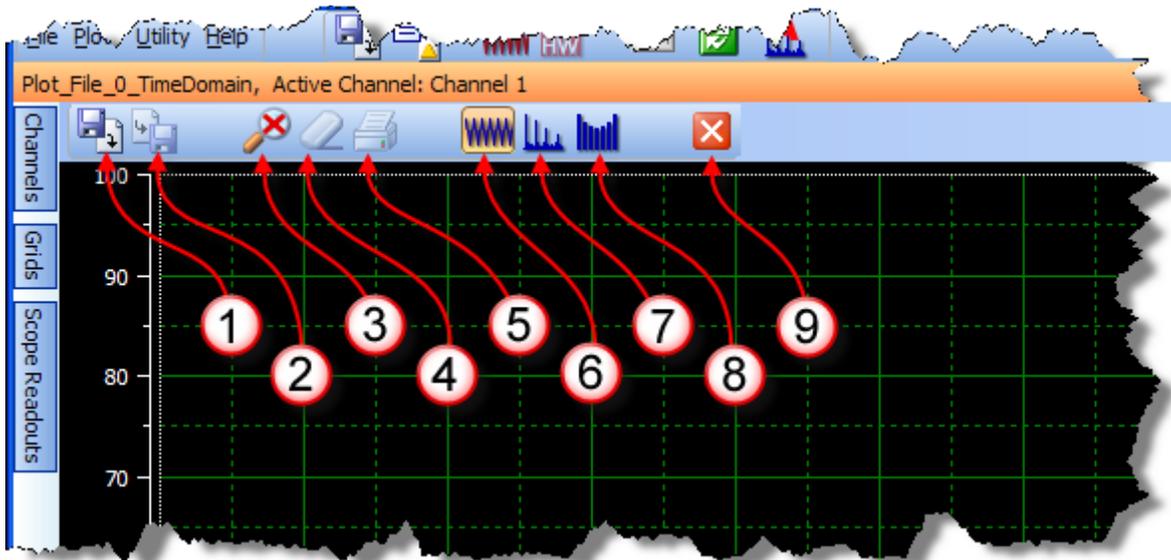


Figure 6: WaveVision 5 plot window controls

1 - Load Plot

The Plot Load dialog is displayed, and the selected plot file is loaded into the new window.

2 - Save Plot

Displays the Plot Save dialog (this button is only active when the plot contains one or more channels with data).

3 - Reset Zoom

Reset X and Y axis zoom to 100%.

4 - Clear

Clear data from all channels.

5 - Print

Print the plot.

6 - Time Domain

Display the plot as time domain data.

7 - FFT

Display the plot as an FFT

8 - Histogram

Display a histogram of the data.

9 - Close

Close this plot.

2.5.3 Right Panels – Signal Source

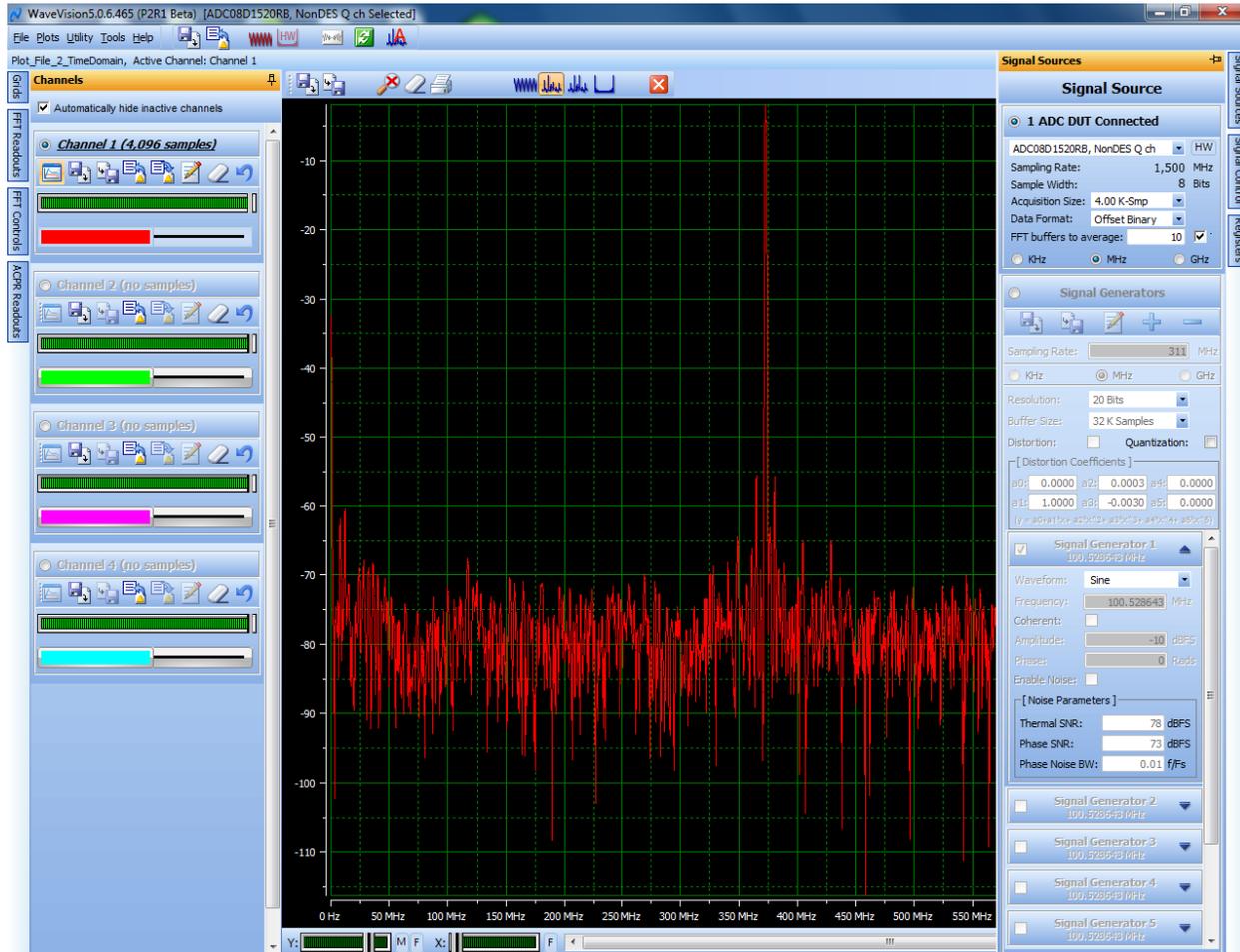


Figure 7a: WaveVision 5 main window command buttons

Open the *Signal Source* panel on the right side of the window and confirm that the ADC0XD1520RB is available and confirm that it is selected. There are five possible modes of operation selectable here:

- NonDES I ch – Dual channel mode capturing and viewing the I-channel data
- NonDES Q ch – Dual channel mode capturing and viewing the Q-channel data
- NonDES I and Q – Dual channel mode capturing and viewing both the I- and Q-channel data
- DESI Mode – Double Edge Sample (interleaved) mode with I input
- DESQ Mode – Double Edge Sample (interleaved) mode with Q input

Double Edge Sampling (DES) – Double edge sampling works much in the same way as single edge sampling except that the signals is sampled both on the rising and falling edge of the sample clock. This effectively doubles the sample rate. In this mode, both converters inside the ADC0XD1520 work on a common input signal. The various DES modes are selected from the *Signal Source* tab on the right side and have requirements for how the inputs must be driven. See the datasheet for more details.

Note – When using “I and Q” mode, it is also necessary to select the *Channels* tab and deselect the “Automatically hide inactive channels” option box in order to allow both channels to appear on the plot. Alternatively, one channel may be displayed per plot:

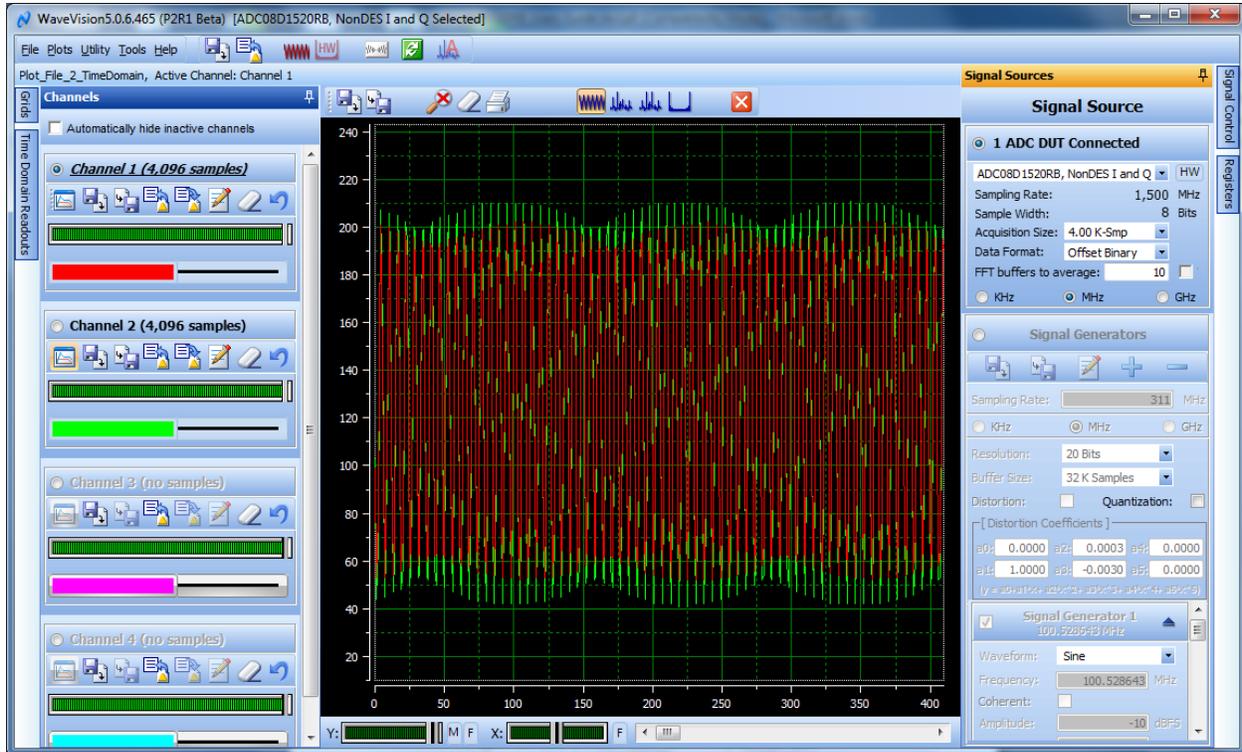


Figure 7b: I and Q mode – both channels displayed on one plot

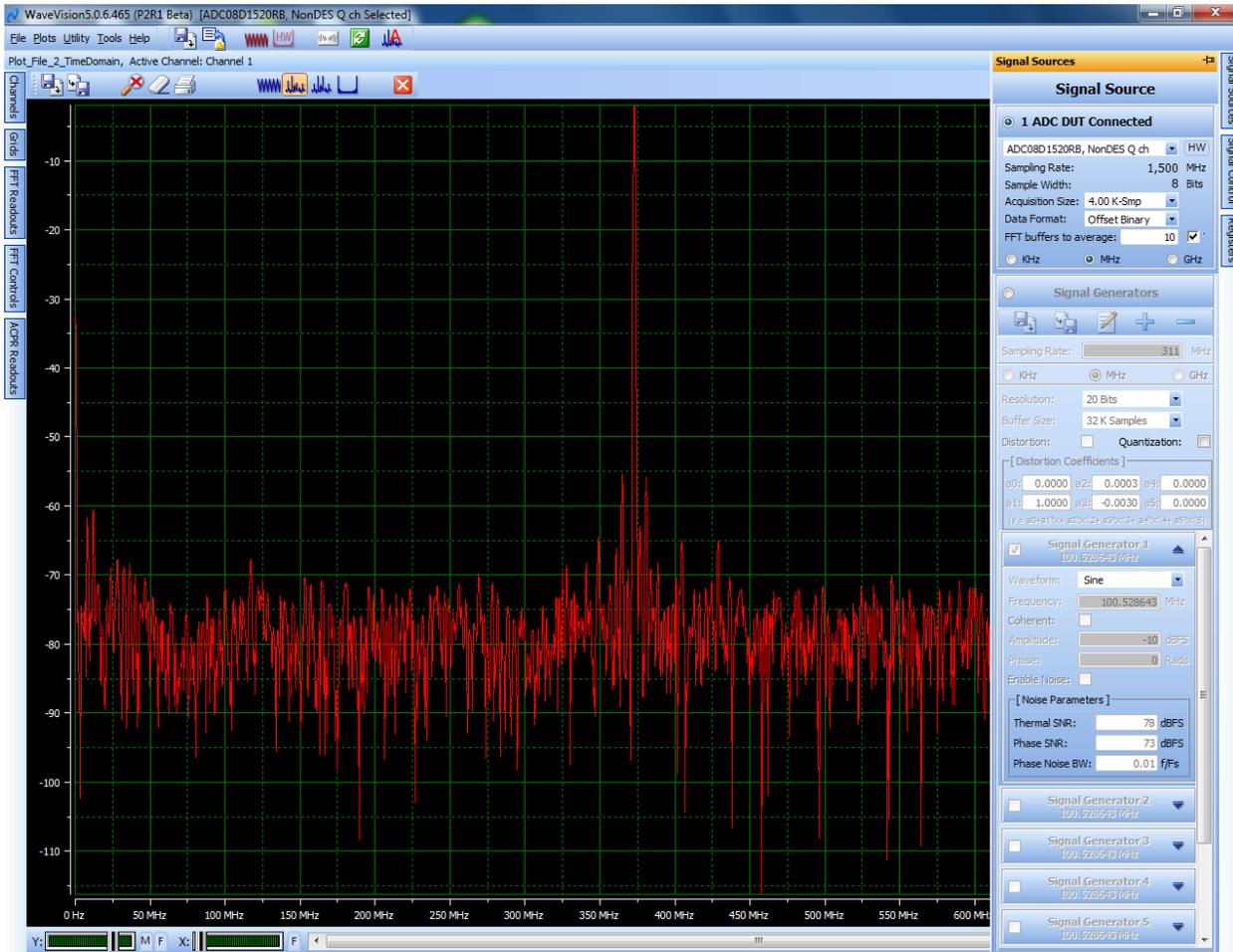


Figure 8: WaveVision 5 main window command buttons

- **Sampling Rate** - When the signal source panel is selected, the clock frequency is displayed. This is initially the internal clock. In this example, 1500 MHz is generated by the LMX2541 on the reference board. The sampling rate is determined by the FPGA when the board is powered up. The calculation is accurate to better than 1%. If an external source is in use, confirm that this number corresponds to the clock reference that is applied. If it is not correct, subsequent data captures and display will not be correct.
- **Resolution** – This will always be set to the ADC0XD1520 resolution which is 8 bits.
- **Acquisition Size** - This setting displays and selects the number of samples captured in each acquisition. 4K samples is the default, with settings up to 32K samples. A larger sample size increases the equivalent FFT bandwidth resolution, but at the expense of more memory and slower acquisition time.
- **Data Format** - The default data format is *offset binary* for the ADC0XD1520.
- **FFT buffers to average** - The last option is the FFT averaging function. Using this feature, subsequent samples can be averaged to obtain improved signal to noise. However, this is at the expense of time.

2.5.4 Right Panels - Registers

Next, configure the hardware (including the ADC) using the Registers control panel on the right side. This is the most important of all the panels for controlling the ADC0XD1520RB.

This panel has seven sub-tabs that control the settings of the board and registers inside the ADC0XD1520. The seven sub-tabs are shown below and include; *Settings*, *Config*, *Extended Config*, *I-channel*, *Q-channel*, *t_{AD} Adjust*, and *Temperature*.

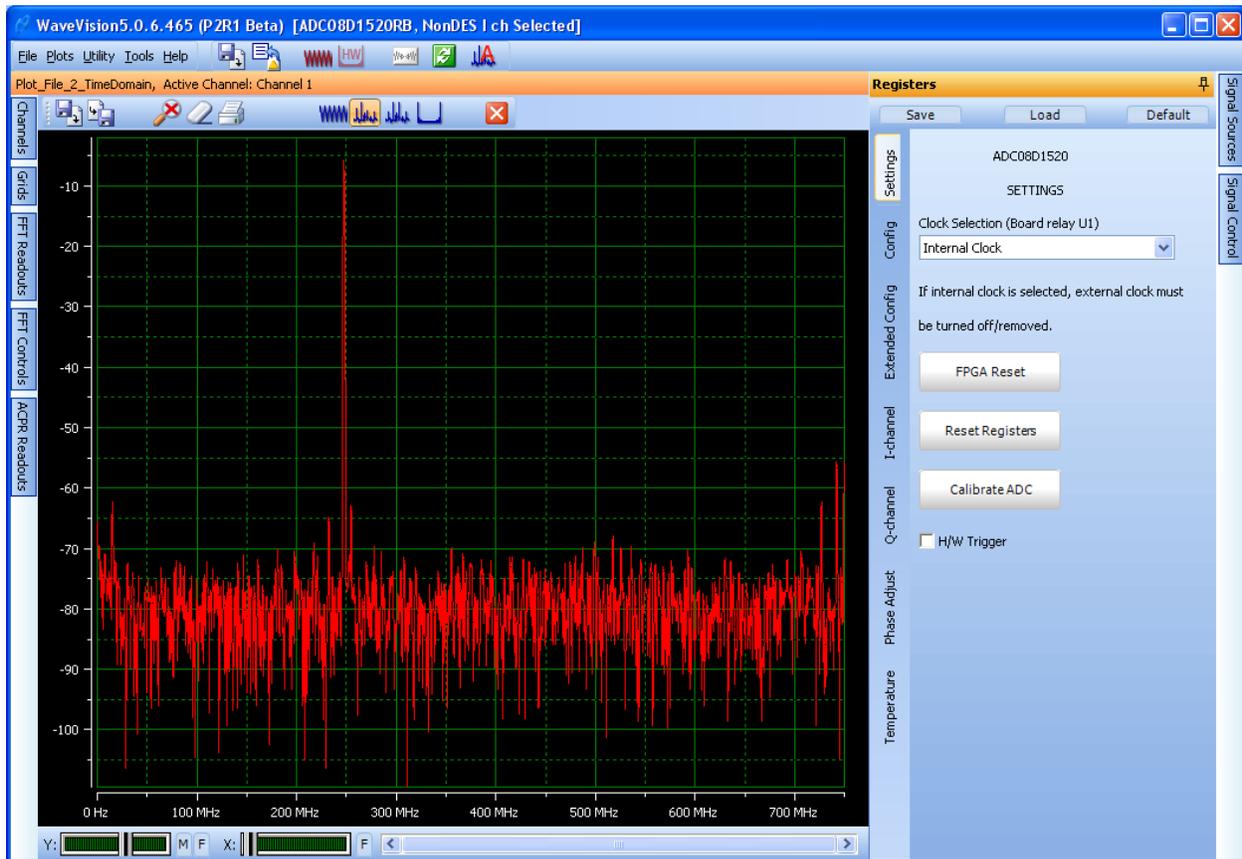


Figure 9: The top level of the Register panel showing the available tabs

The following is a short description of each tab under the *Register* panel.

Settings: This tab gives choice of either External Clock or Internal Clock, and buttons to initiate FPGA Reset, Reset Registers and Calibrate ADC. Calibration of the ADC should be performed if changes occur such as device temperature, mode changes (single channel to dual channel, single edge sampling (Non-DES) to double edge sampling (DES)). For more information, refer to the Calibration section of the ADC0XD1520 datasheet. The H/W Trigger function is also enabled using the check box on this tab.

Note: If the Internal Clock is selected, then the External Clock signal generator should be disconnected or switched off to prevent performance degradation.

Config: This tab configures various features and modes of the ADC0XD1520 and is shown below. It accesses or changes the following functions, all of which are controlled through Configuration Register 1.

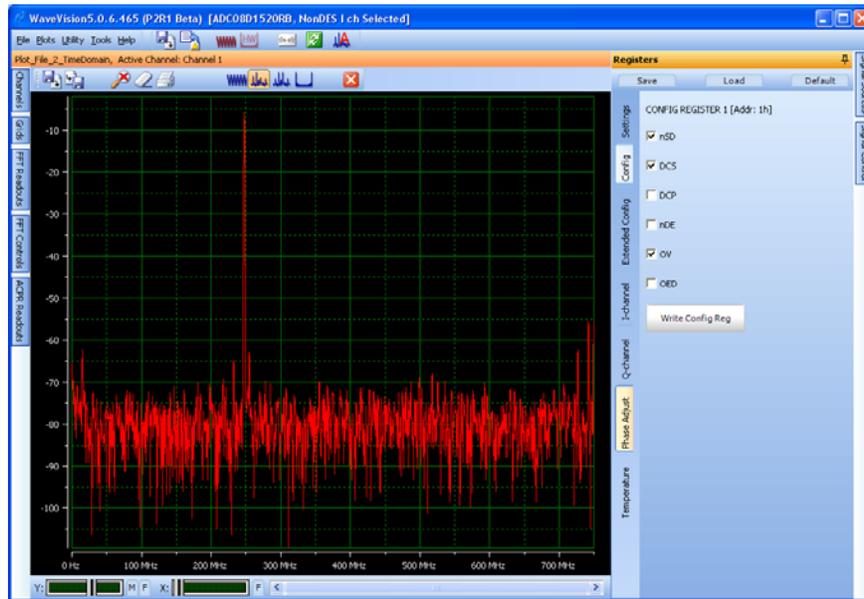


Figure 10: Config Panel

- **nSD** – Second DCLK output – When this bit is 1b, the device only has one DCLK output and one OR output. When this output is 0b, the device has two identical DCLK outputs and no OR output.
- **DCS** – Duty Cycle Stabilizer – When this bit is set to 1b, a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disabled.
- **DCP** – DDR Clock Phase – This bit only has an effect in the DDR mode. When this bit is set to 0b, the DCLK edges are time-aligned with the data bus edges (“0 degree phase”). When this bit is set to 1b, the DCLK edges are placed in the middle of the data bit-cells (“90 degree phase”).
- **nDE** – DDR Enable – When this bit is set to 0b, data bus clocking follows the DDR mode whereby a data word is output with each rising and falling edge of DCLK. When this bit is set to a 1b, data bus clocking follows the SDR mode whereby each data word is output with either the rising or falling edge of DCLK, as determined by the OutEdge bit.
- **OV** – Output Voltage – This bit determines the LVDS outputs’ voltage amplitude and has the same function as the OutV pin that is used in the Non-extended Control Mode. When this bit is set to 1b, the normal output amplitude is used. When this bit is set to 0b, the reduced output amplitude is used.
- **OED** – Output edge and demux control – This bit has two functions. When the device is in SDR mode, this bit selects the DCLK edge with which the data words transition and has the same effect as the OutEdge pin in the Non-Extended Control Mode. When this bit is set to 1b, the data outputs change with the rising edge of DCLK+. When this bit is set to 0b, the data output changes with the falling edge of DCLK+. When the device is in DDR mode, this bit selects the Non-demultiplexed Mode when set to 1b. When the bit set to 0b, the device is programmed into the Demultiplexed Mode. If the device is in DDR and Non-Demultiplexed Mode, then the DCLK has a 0 degree phase relationship with the data; it is not possible to select the 90 degree phase relationship.

Note: No changes will take effect until the **Write Config Reg** button is clicked.

Extended Config: This tab controls the extended configuration register.

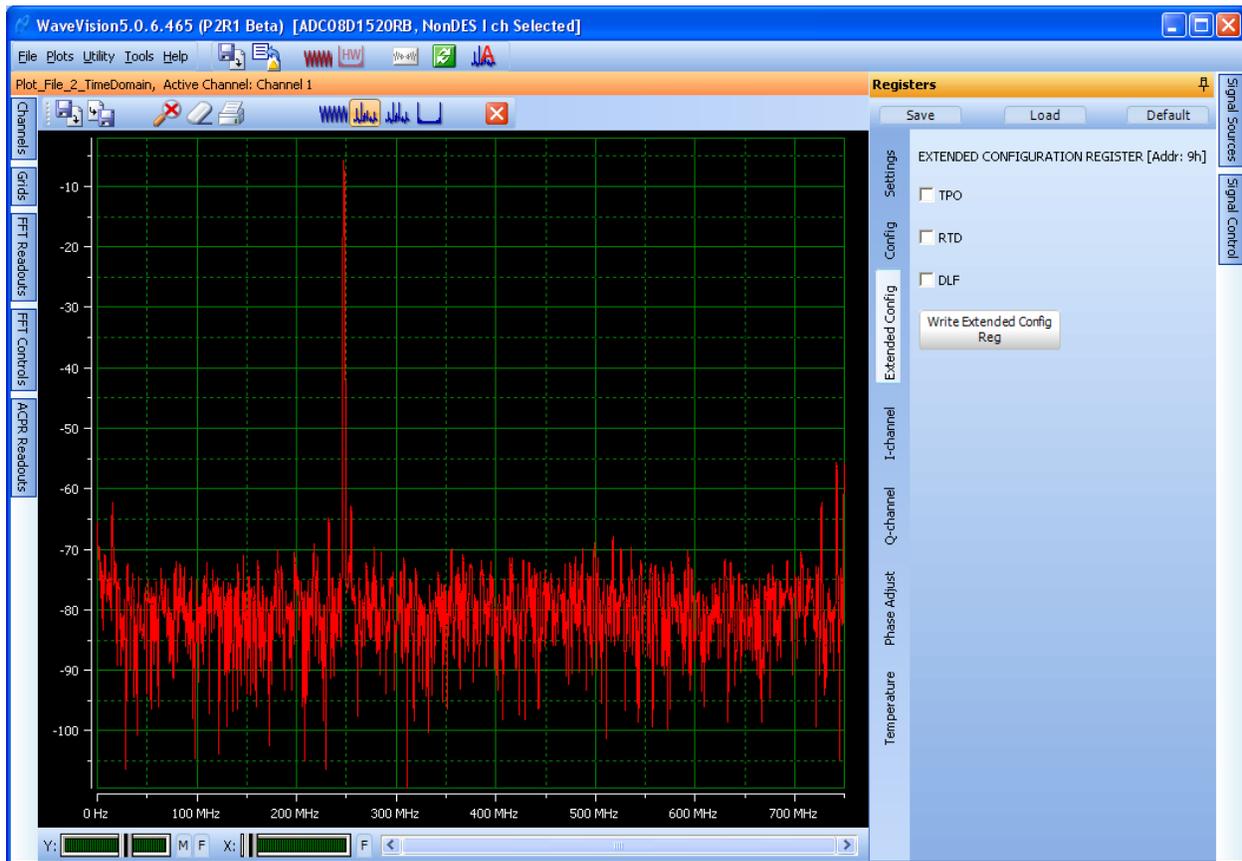


Figure 11: Extended Config Panel

- **TPO** – Test Pattern Output – When this bit is set to 1b, the ADC is disengaged and a test pattern generator is connected to the outputs including OR. This test pattern will work with the device in the SDR, DDR, and the Non-demux Modes (DES and Non-DES).
- **RTD** – Resistor Trim Disable – When this bit is set to 1b, the input termination resistor is not trimmed during the calibration cycle and the DCLK output remains enabled. Note that the ADC is calibrated regardless of this setting.
- **DLF** – DES Low Frequency – When this bit is set to 1b, the dynamic performance of the device is improved when the input clock is less than 900 MHz.

Note: No changes will take effect until the **Write Extended Config Reg** button is clicked.

I-channel: This tab changes the sign and the magnitude of the offset and the full scale range settings.

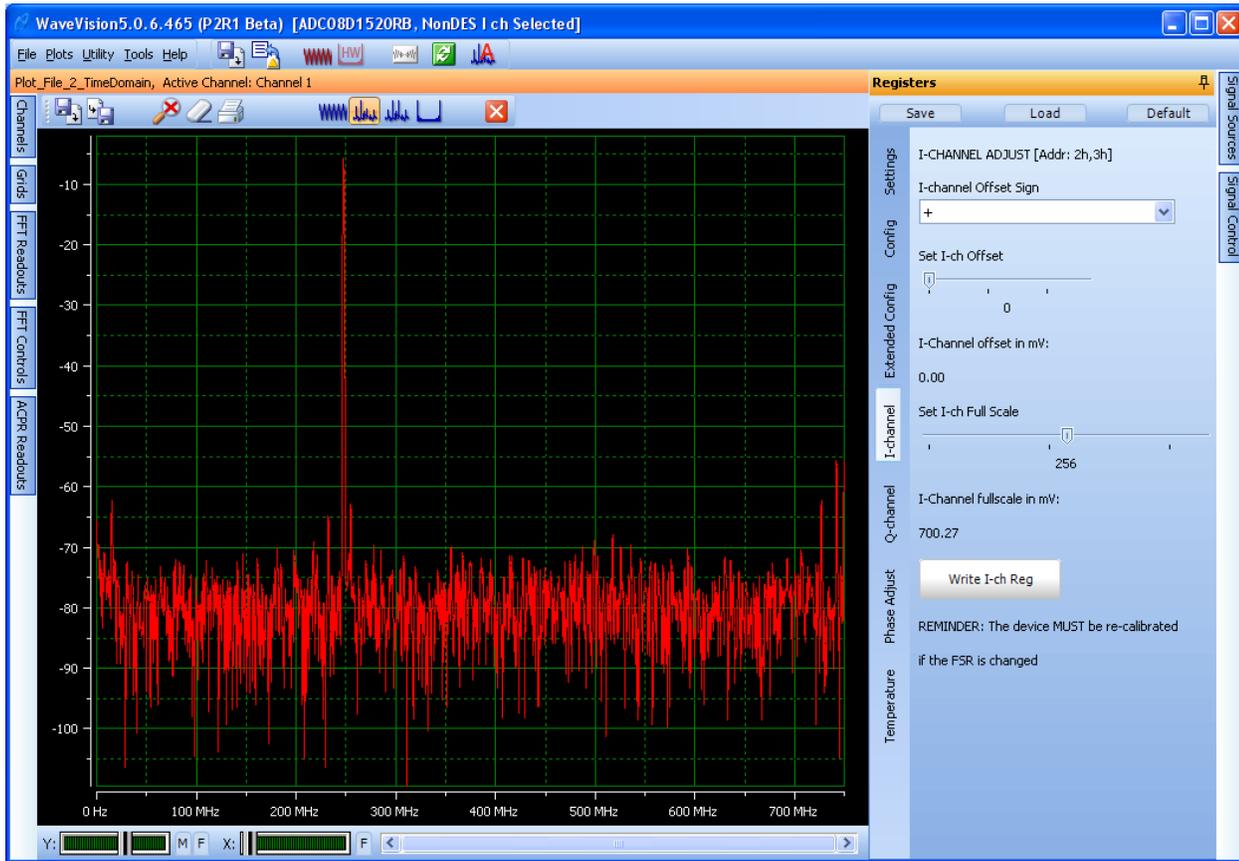


Figure 12: I-Channel Panel

- **I-channel Offset Sign** – This pull-down selects a positive or negative offset.
- **I-ch Offset** – This slider selects the magnitude of I-ch Offset applied. Adjustment can be done using the computer mouse/pointer, or using left/right arrow keys once the slider has been selected. Although the offset is entered in an 8 bit (0 to 255) relative form, it is also displayed in approximate mV.
- **I-Channel Full Scale** - The approximate I-Channel input full scale range (mV peak-to-peak) is selected, ranging from a minimum of 560mV to a maximum of 840mV. The default setting is 700mV.

Note: No changes will take effect until the **Write I-ch Reg** button is clicked. Also, the ADC must be re-calibrated if the full-scale is changed.

Q-channel: Similar to I-channel

Phase Adjust: This tab controls the Aperture Delay function.

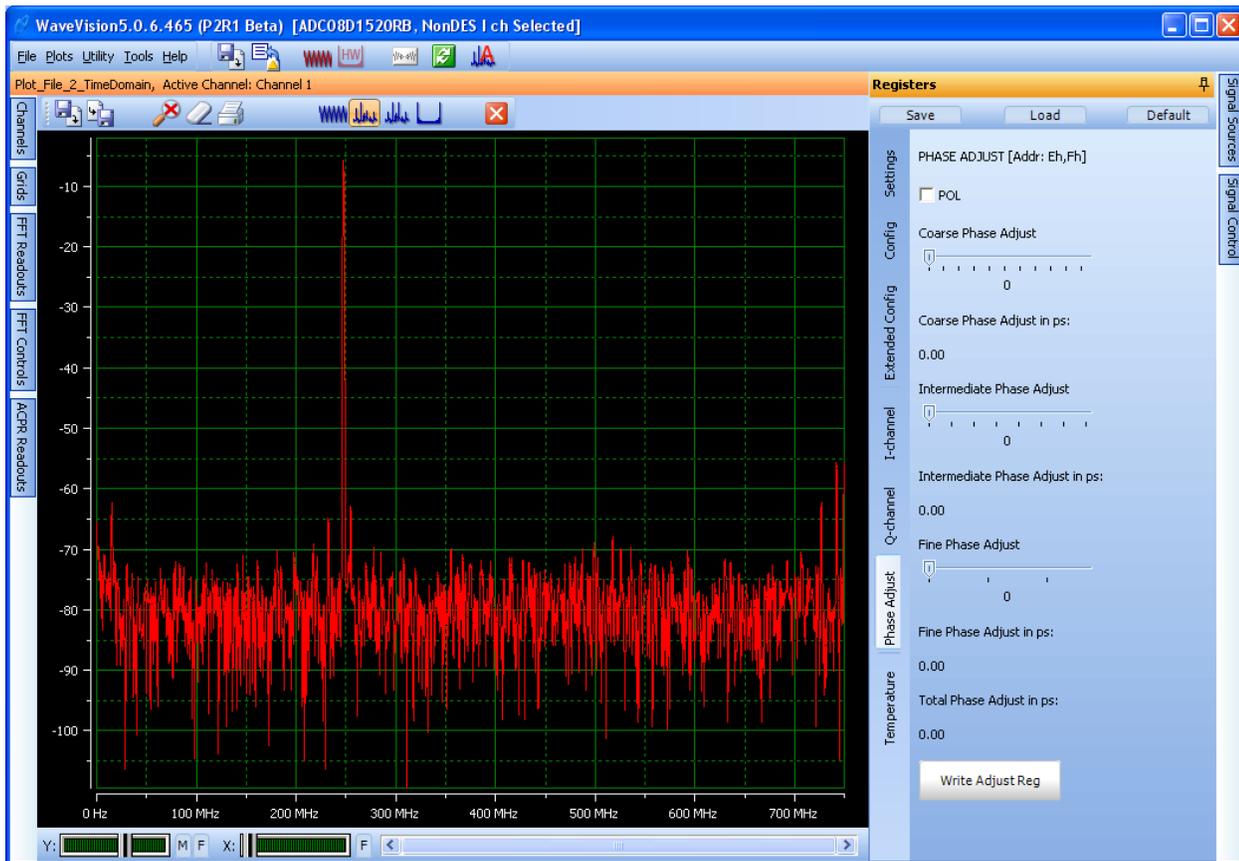


Figure 13: t_{AD} Adjust Panel

- **POL** – Polarity Select – When this bit is selected, the polarity of the ADC sampling clock is inverted
- **Coarse Phase Adjust** – Sets the approximate amount of coarse Aperture Delay applied.
- **IPA** – Intermediate Phase Adjust – Each code value in this field delays the sample clock by approximately 11 ps. A value of 000b in this field causes zero adjustment. Maximum combined adjustment using Coarse Phase Adjust and Intermediate Phase adjust is approximately 2.1 ns.
- **Fine Phase Adjust** – Sets the approximate amount of fine Aperture Delay applied.

Note: No changes will appear until the **Write Adjust Reg** button is clicked.

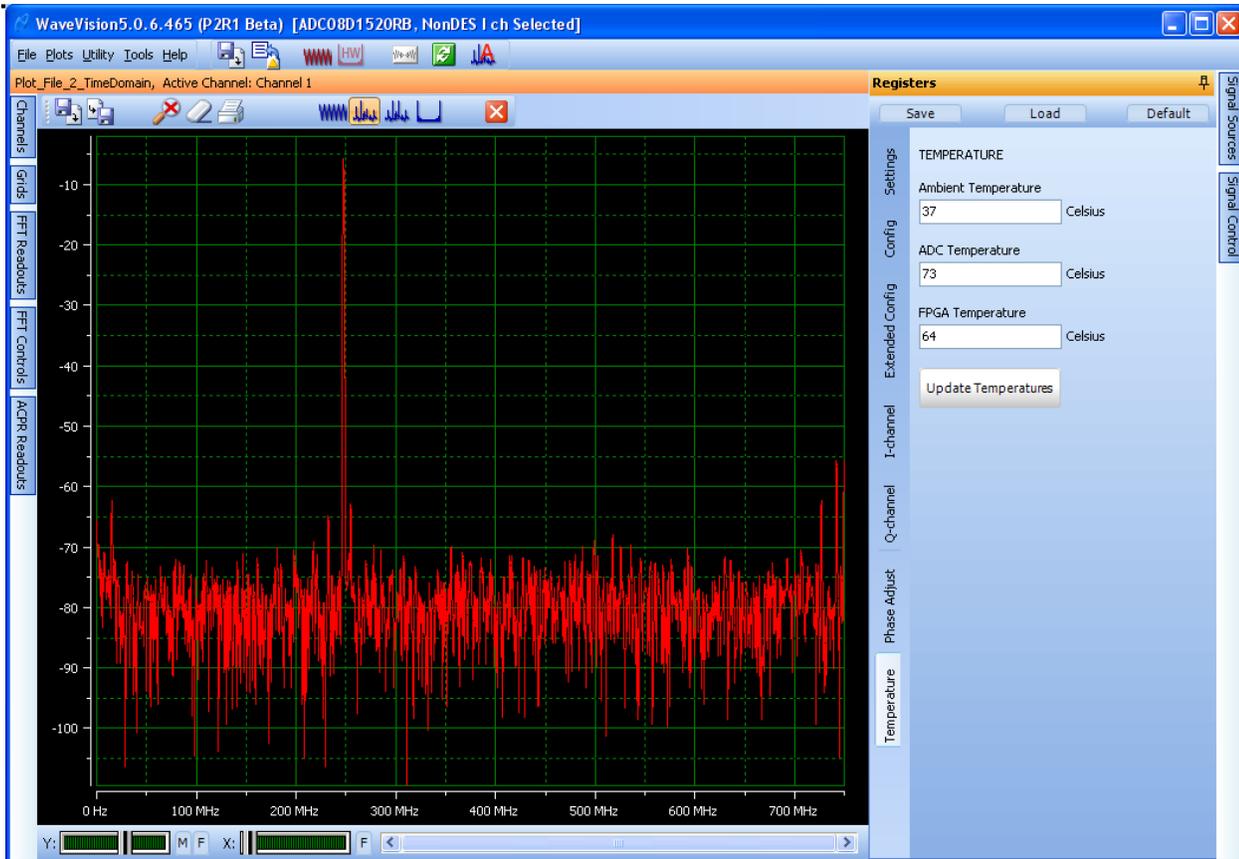


Figure 14: Temperature Panel

- **Ambient Temperature** – Provides the local/board temperature of the LM95233 IC.
- **ADC Temperature** – Provides the approximate die temperature of the ADC0XD1520.
- **FPGA Temperature** – Provides the approximate die temperature of the Xilinx Virtex-4 FPGA.

Note: No changes will appear until the **Update Temperatures** button is clicked.

2.6 Data Capturing

The board is now ready for a data capture. Before proceeding, perform a manual calibration of the ADC. Even though the ADC performs a self-calibration at the time of power-up, it is recommended that the user perform another calibration after sufficient time has passed for the system (primarily temperature) to stabilize. Manual calibration is performed by clicking the *Calibrate ADC* feature in the *Register* control panel, *Settings* sub-tab.

2.6.1 Configure Display Settings

Open the FFT Control left panel. Confirm that the *dBFS* unit is selected. Also confirm that the correct clock frequency is being measured by the software by checking in the *Signal Source* right panel. The default frequency of the on-board clock source is shown in the board performance data shipped with your board.

2.6.2 Check Input Amplitude

*The ADC's inputs can be damaged if the Operating Maximums are exceeded (see **Operating Ratings** section in the datasheet).*

IMPORTANT: Since the ADC signal and clock inputs are not provided with additional protection circuitry on this board, the burden is on the user to not overdrive the inputs to the extent of damaging them. An "Over-range" LED is provided for each channel to indicate that the signal amplitude is beyond the ADC full-scale range, i.e. 0dBFS. Keep the signal amplitude within the operating ratings as specified in the datasheet.

2.6.3 Acquire and Display Data

Perform a data acquisition by clicking the Acquire Data button (Item #5 in Figure 6).

The acquired data will now appear in the (default) time domain plot window. Switch to the frequency-domain window (FFT) using the WaveVision 5 controls. Type Ctrl-r to obtain the summary of the acquisition. Place the software in continuous mode (Item #6 of Figure 6) and then acquire again.

At this point, dynamic performance metrics similar to those shown on the reference data shipped with the board may be obtained. One of the basic variables that you may experiment with at this point is to change the input signal magnitude and frequency. Please note that to achieve the reference performance, band-pass filters similar to the items referenced in Section 2.2 should be used. The absence of these filters on the input signal or external clock will result in sub-standard performance. This is because most signal generators also generate harmonics which, if not filtered out, will reduce the system performance.

The displayed units can be in dBc or dBFS.

2.6.4 External Clock Source

It is also possible to apply a high-quality external signal source to the clock input rather than using the on-board LMX2541 clock synthesizer. This will help quantify the LMX2541's performance in an ultra-high-speed signal-path such as this one. Also, it enables the user to sample at a frequency other than that which the LMX2541 is programmed to.

If it is attempted to make a data capture while the External Clock source is selected, but the external source signal generator is not turned on, then the software will hang until a clock source is provided.

The external clock source should be disconnected or turned off when the on-board clock source is selected. Failure to do so will result in poor performance due to the mixing of the on-board clock and the small amount of external clock signal leaking through the internal/external clock relay. When the external clock source is selected, the on-board LMX2541 is turned off, so that it does not interfere with the external clock source.

If the internal/external clock selection is changed, then the ADC should be re-calibrated.

The required clock amplitude to the ADC may be found in the datasheet as V_{IN_CLK} . For the ADC0XD1520, this range is {0.4Vpp, 2.0Vpp}. However, there is a significant insertion for the Teledyne relay, RF303, and other components on the ADC0XD1520RB, as shown in Figure 15. To compensate for this insertion loss, use the recommended values in Table 1. The magnitude shown is for the signal at J11, the External Clock Input SMA, in order to maintain the proper level at the ADC's CLK+/- inputs. For example, measure and adjust the amplitude of the external signal generator + filter on a power meter or spectrum analyzer before connecting to the External Clock Input.

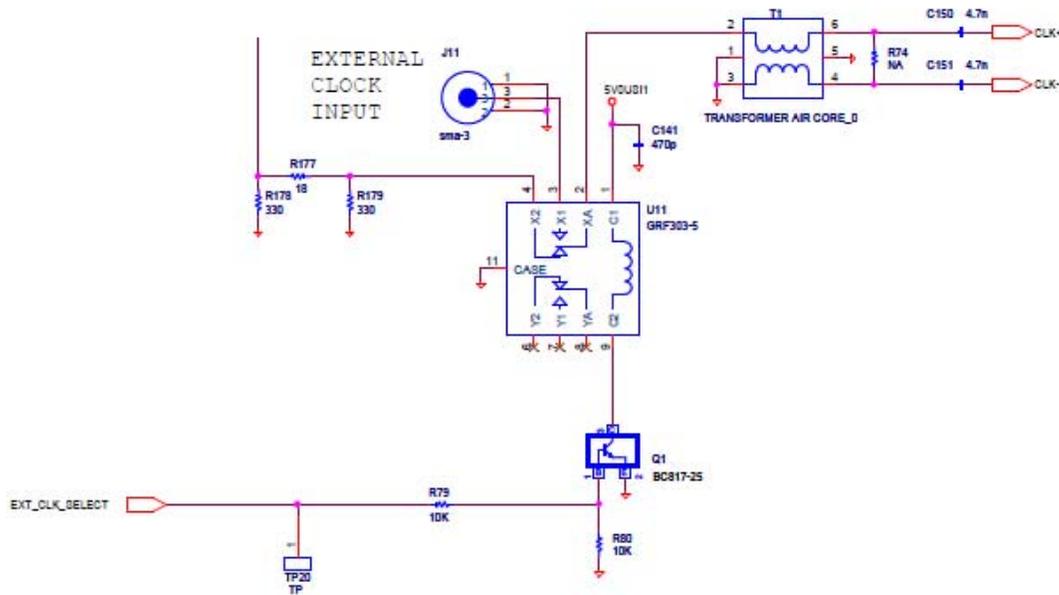


Figure 15. External / internal clock selection circuit on ADC0XD1520RB

Ext Clk Freq	To maintain 0.4Vpp	To maintain 2.0Vpp
1.0 GHz	-2 dBm	+9 dBm
1.2 GHz	+1 dBm	+11 dBm
1.4 GHz	+1 dBm	+12 dBm
1.6 GHz	+3 dBm	+16 dBm
1.8 GHz	+2 dBm	+14.5 dBm
2.0 GHz	+3 dBm	+16 dBm (hit max gen @ 1.8V)

Table 1. External clock frequency relay insertion loss compensation

Reference Board Functional Description

2.7 System Block Diagram

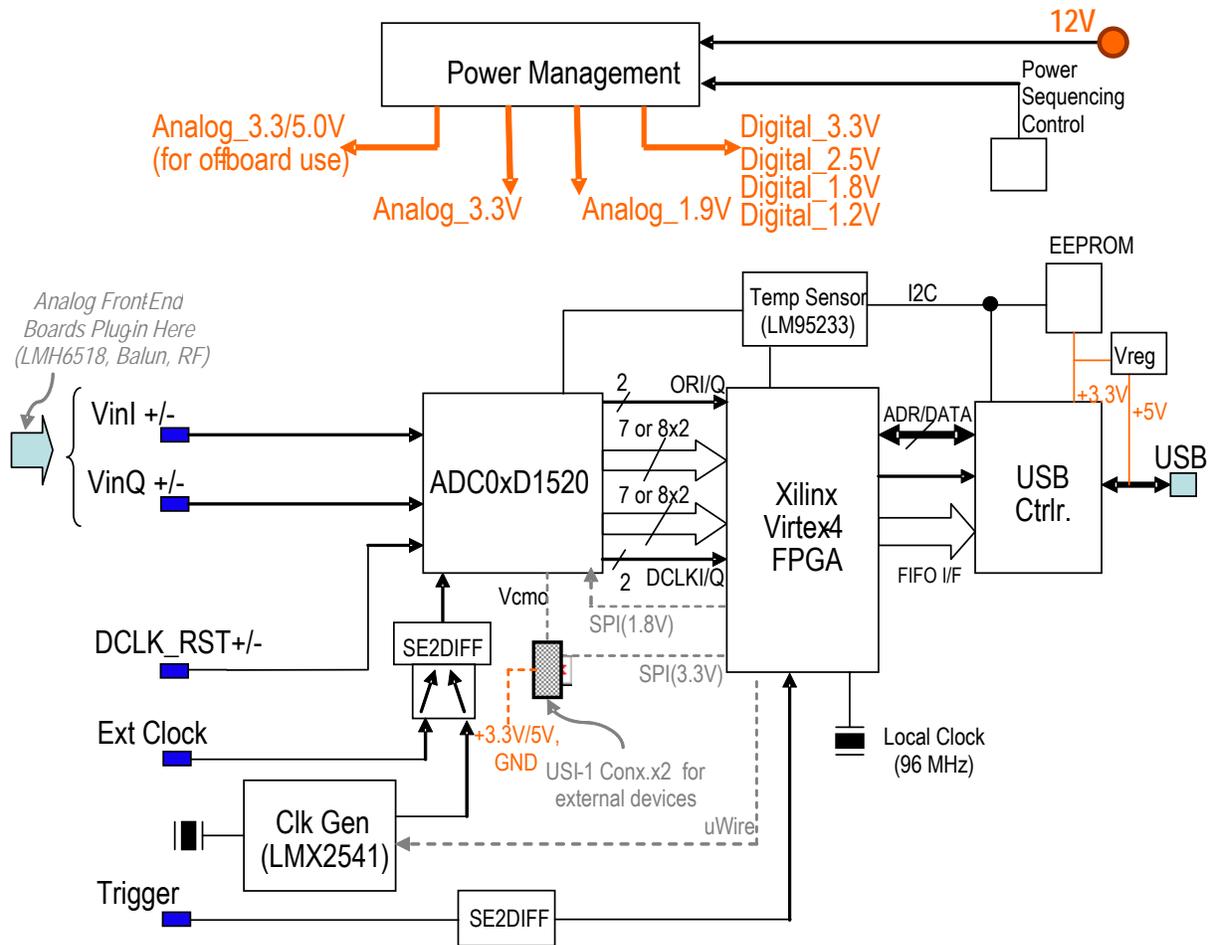


Figure 16: ADC0XD1520RB System Block Diagram

2.8 System Description

2.8.1 The ADC0XD1520

The ADC0XD1520 forms the heart of this reference board. This low-power, high-performance CMOS analog-to-digital converter digitizes signals at 7/8-bit resolution at guaranteed minimum sampling rates of 1.5 Gs/s in dual channel configuration and 3.0 Gs/s in single channel configuration. The ADC0XD1520 is targeted at achieving very good accuracy and dynamic performance while consuming the lowest power available in the industry when both channels are powered-up. Refer to the latest version of the ADC0XD1520 datasheet for more detailed information.

This reference board gives complete control over the ADC0XD1520 and gives the user direct performance results of the chip without the need for an elaborate setup. Each of the device's control pins may be set high or low. Control is provided in two different manners - direct pin control with jumpers or through the serial interface (the device's extended control mode) using the WV 5 register control panel. *In order to use the extended control mode the ECE jumper must be set to LOW.* This is the recommended method and gives the user the most flexibility and ease of use.

Analog Front-End: The analog signal connection to the ADC is kept simple on this board in order to achieve the highest possible bandwidth. The board is designed to be coupled to front-end circuitry in a DC or AC coupled manner. AC-coupling requires the use of dc-blocks on the SMA connectors. By default, the board is shipped by TI with dc-blocks. In addition, the board is also jumper-configured for DC-coupled operation (pin 9 on J15 is removed for DC operation).

2.8.2 LMX2541 Clock Synthesis chip

The LMX2541xxxx family provides a single-chip, very low-jitter clock solution at frequencies up to 4.0 GHz. In this application, the LMX2541SQ3030E is used - which can be programmed to operate over a range of 2810-3230MHz. This output frequency from the VCO is divided to achieve the desired clocking frequency of the ADC. On the ADC0XD1520RB board, the device is configured for a 1.5 GHz output through the serial interface. The initial command sequence that automatically configures the LMX2541 is pre-programmed into the FPGA's firmware.

The clock source for the ADC can be selected between the on-board LMX2541 or an external clock source connected through the J11 SMA connector. The selection is performed through the WV 5 register panel. It is recommended that the external clock source should be connected and enabled before it is selected. ***For optimum performance, the external clock signal generator and the LMX2541 should not be enabled at the same time.*** This is because the RF relay used to select between them does not provide adequate isolation to keep one from affecting the other. Having both clocks on simultaneously will result in excessive spurious signals. The default setting for this board is the on-board LMX2541 clock source.

2.8.3 FPGA

The design employs a Xilinx Virtex-4 FPGA for capturing the digital data. While the board is powered up and configured, the FPGA is continually receiving data from the ADC. In response to a user command through the WV-5 software, the ADC captures the desired amount of data in its on-chip buffer (up to a maximum of 32K samples per-channel). The user can then command the FPGA to upload the captured data to the PC through the USB interface for further processing.

This board can support the ability to program the FPGA for specific requirements. A standard JTAG connector is provided for downloading FPGA object code from the Xilinx development environment.

Please note that Texas Instruments does not provide support for any user-designed FPGA functionality beyond the standard functionality that is shipped with the board.

Hardware Trigger: The external trigger feature of the Reference Board is designed to enable applications which trigger a data capture. When the hardware trigger is enabled, an acquisition can be selected from the software, but the actual beginning of data capture will be postponed until the external trigger pulse is applied to the J26, the EXT_TRIG SMA.

Note: This only applies to the data which is captured and displayed in the WaveVision GUI; the streaming data to the FMC connector still runs continuously.

Apply the trigger signal at J26, the EXT_TRIG SMA. If the voltage applied, $V_{trigger}$ is less than the threshold, V_{th} , of the MC100EP16, then the system will not capture. If $V_{trigger}$ is greater than V_{th} , then a data capture will occur. V_{th} is approximately 2.1V, so it is recommended that high trigger voltage is in the range of {2.5V, 3.3V}. The low trigger voltage should be 0V. Note that this may be a single shot data capture or a continuous trigger. If the trigger is armed, but $V_{trigger}$ is not greater than V_{th} within approximately 3 minutes, then the software will time out and show the error message: “Board failed to collect samples.”

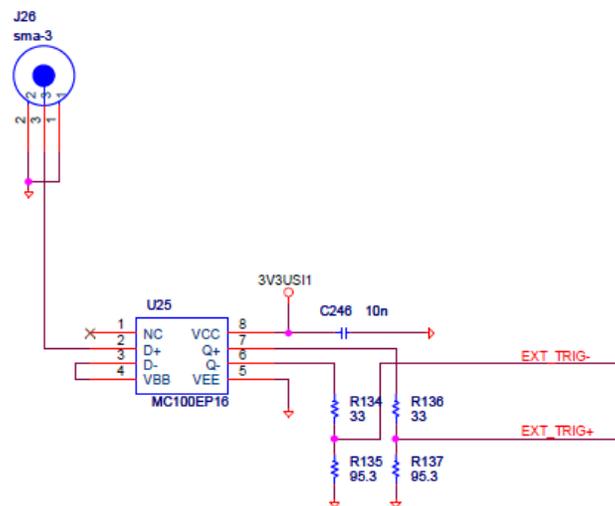


Figure 17: Trigger circuit on reference board

1. Connect a signal source to the EXT_TRIG SMA (J26).
2. In the WaveVision5 GUI, select Registers – Settings – check the H/W Trigger box.
3. Select single or continuous capture.
4. Apply $V_{trigger}$ above the threshold, V_{th} , when ready to capture.

Auxiliary Port: FMC connector forms an auxiliary data port. With it, the FPGA captures the ADC’s high-speed continuous streaming data and retransmits the data out of the FMC port. See photo below of the FMC port on the bottom of the board.

- Install J155 to force FPGA to output data on FMC port (without a power good signal from Carrier to Mezzanine). This is useful when a non FMC compliant board is connected to Mezzanine (ADC0XD1520RB)
- Install J156 to force a power good signal from Mezzanine (ADC0XD1520RB) to Carrier. This is used to override for initial FPGA debug.

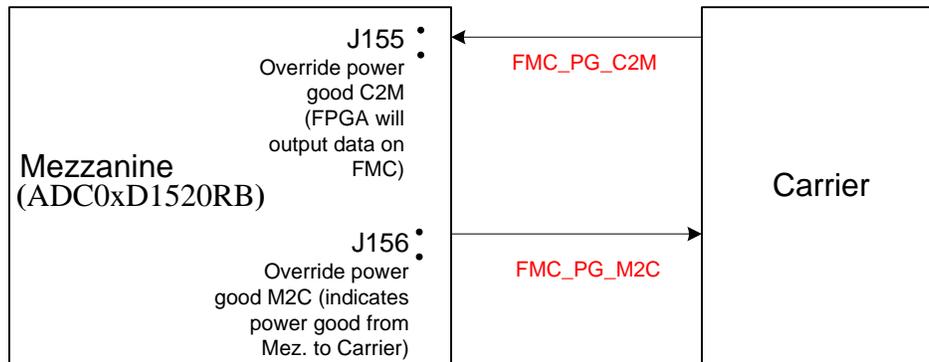


Figure 18: Explanation of Power Good override jumpers for FMC port

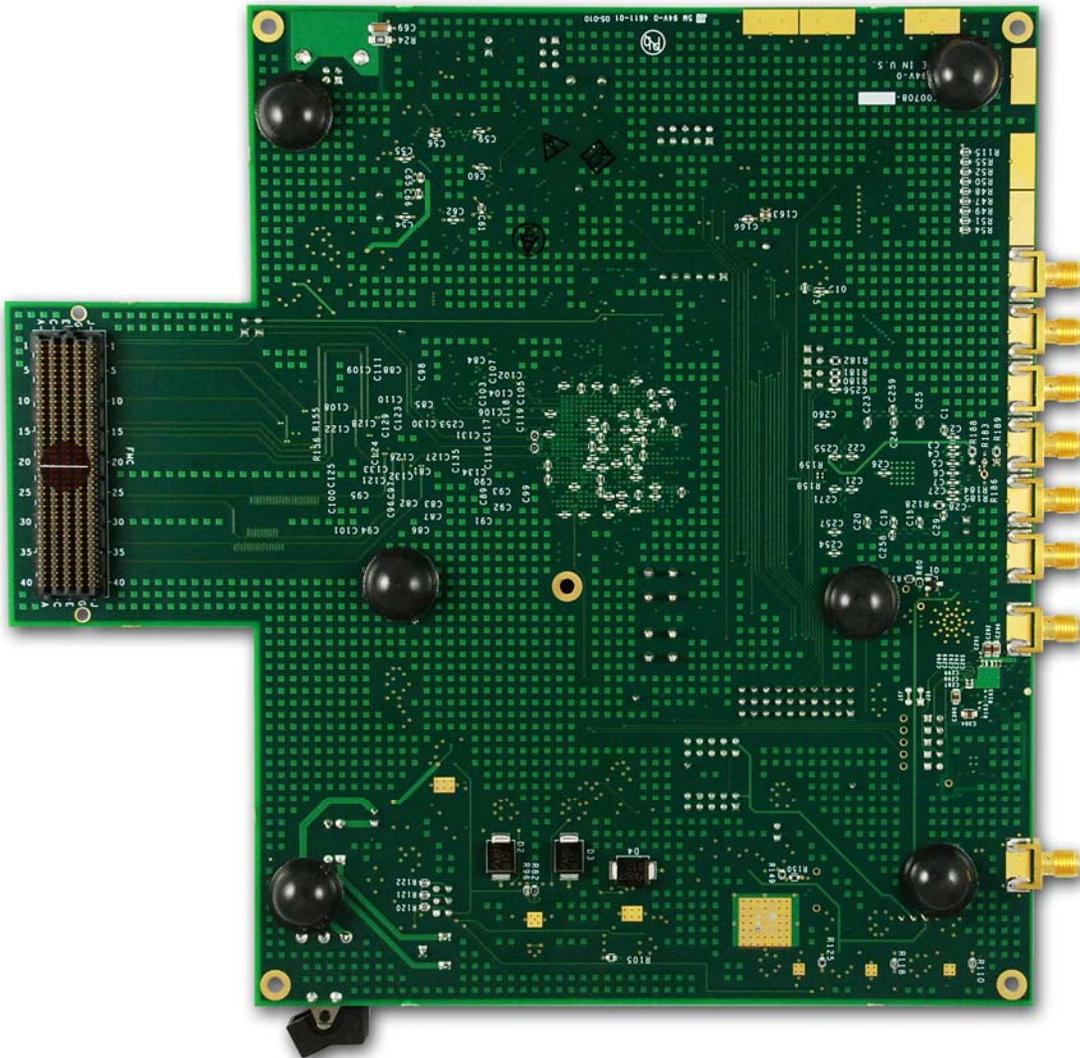


Figure 19: Bottom of ADC0XD1520RB showing FMC port

2.8.4 LM95233 Temperature Sensor

Using the TI LM95233 temp sensor chip; the ambient, ADC0XD1520 and Xilinx FPGA temperatures can be monitored. The temperature readings are available through the WV-5 software.

3.0 Electrical Specification

Power Supply:	Nominal = 12V Minimum = 11.0V, Maximum = 12.5V <i>(Voltages outside these levels can cause damage!!)</i>
Power Consumption:	Nominal = 10 Watts Maximum = 20 Watts
ADC Input Signals:	Maximum Operating Voltage = see datasheet Recommended/initial (full scale) generator setting = 0 dBm <i>(The maximum level at the signal generator is dependent upon the insertion loss from other hardware before the ADC inputs. Care should be taken not to exceed the Operating Ratings at the ADC input.)</i>
Clock Input Signal:	Maximum Operating Voltage = +2.0V Recommended generator setting = +1 dBm <i>(The maximum level at the signal generator is dependent upon the insertion loss from other hardware before the clock inputs. Care should be taken not to exceed the maximum limits at the clock inputs.)</i>
USB Port:	USB 2.0 compliant

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Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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~

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