# Crystal Or Crystal Oscillator Replacement with Silicon Devices

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## ABSTRACT

This application report is a general guide that outlines the advantages of using silicon-based timing devices from Texas Instruments to generate system clocking solutions. This report covers the conventional way to derive system clocks using crystals and crystal oscillators, disadvantages of using these mechanical components, and details on replacing them with silicon-based timing devices from TI. Clock and timing devices from TI help resolve key system problems that are explained in detail in this document.

**Contents**

# 1 Introduction

Most electronic systems require a clock signal to synchronize operation of various components in the system. For digital logic, the clock signal regulates the sequencing of digital state machines. This ensures that the key timing parameters like setup and hold times and propagation delay are within allowable limits. In communication systems, the clock signal regulates the speed of synchronized data transmission over the link. In A/V systems, the clock signal regulates the sound and image reconstruction from digital media to produce time-accurate entertainment. For any modern electronic system, clock signals of multiple frequencies and/or multiple copies of a single frequency in various output formats may be required by various subsystems. Tight control of phase and frequency relationship, synchronization to external frequency sources, modulation to reduce EMI, and redundant switching might be additional system requirements.

## 1.1 Discrete Resonators (Crystals and Crystal Oscillators)

Discrete resonators have historically been used to synchronize such systems due to their cost efficiency and stability over time and temperature. Crystals are designed to work in conjunction with a semiconductor gain circuit that is connected to both terminals of the resonator. The piezoelectric and physical properties of the resonator material allow the vibrating resonator to act as an electronic filter, passing the frequency components in its pass band back to the input of the gain circuit. At the pass band frequency where the loop gain is > 1 and the phase is 360 degrees, the resonator begins to oscillate, producing a stable frequency source at the output of the gain circuit. The most commonly used discrete resonator, to achieve frequencies less than 50MHz, is an AT cut quartz crystal oscillating at its fundamental frequency and with an accuracy of < 50 ppm, inclusive of temperature and aging. When using quartz crystals on a PCB, the parasitic components on the PCB have an effect on the characteristics of the resonator output. Discrete oscillators are used to achieve frequencies higher than 50MHz in a single package that contains a quartz crystal as the resonator oscillating at an overtone frequency along with a bandpass filter and gain circuit. The output of the oscillator is not impacted by the parasitic components on a PCB. Such oscillators are expensive in general.

## 1.2 Phase Locked Loop (Silicon-based Clock Devices)

An alternate way of generating system clock signals is using a silicon based device comprised of a phase locked loop (PLL). A phase-locked loop (PLL) is a closed-loop frequency-control system based on the phase difference between the input clock signal and the feedback clock signal of a controlled oscillator. The PLL responds to variations in frequency and phase of the input by automatically raising or lowering the frequency of the controlled oscillator through feedback until the output is aligned in phase and frequency of the system. PLLs are widely used for synchronization purposes in several communication and consumer domains, radio transmitting, clock recovery and deskewing, spread spectrum, clock jitter reduction, clock generation and clock distribution.

## 1.3 Disadvantages of Discrete Resonators

Although crystals are cost efficient, especially if the system requires less than 4 clock frequencies, they have several disadvantages as listed below and as a result, a more robust hardware design tends to limit their usage. Crystal-based resonators suffer from the following:

- **Cost**: While a single crystal or low frequency crystal oscillator is inexpensive, if a system requires a mix of multiple crystals and/or crystal oscillators and the total frequencies needed are more than 4, it could be more cost effective to use a PLL device with an input crystal to generate all the system frequencies needed.
- **Reliability**: Crystals have a higher failure rate than silicon based devices. Each crystal removed from the system can help increase overall system reliability. Integration also reduces component count on the board, leading to higher stability and lower product return rates.
- **Availability**: Crystals in the range of 10-50 MHz are readily available. However, a high-frequency crystals above 50 MHz are more difficult to manufacture and procure. In such a scenario, crystal oscillator with a higher-order overtone crystal is used and is more expensive. PLL devices use one low-frequency crystal (or an available clock reference) to generate several high-frequency high-performance outputs.

- **Aging**: Crystals are prone to aging, with a +/-2ppm to +/-5ppm error every few years, caused by impurities in the crystal material and on the crystal surface, as well as mechanical stresses between the crystal material and the deposited electrodes. Aging is also different for each crystal and varies from one vendor to another. It may cause slow system-wide degradation that is not the same for every system. PLL devices maintain their accuracy over their entire lifetime across all devices.

- **Programmability**: PLL devices have built-in programmability features that provide flexibility during design. Programmable features include changing output frequencies, drive strength settings, spread spectrum amounts, and pin programming for frequency selection, which implies different frequencies on an output pin based on need. Programmability can be done in-system, typically using an I2C-interface, to modify certain parameters "on the fly". Discrete resonators only offer one frequency and offer very limited flexibility.

- **Component Reduction and Board Space Savings**: PLL devices reduce number of components through integration, as hardware designers migrate towards fewer components to reduce problems caused by routing and maintaining signal integrity. PLL devices have the ability to generate several outputs from a single crystal, thereby reducing the number components used in a system and conserve board space.

- **Inventory Management:** One of the key challenges that procurement teams face today is managing inventory, demand, and forecast planning for every device that goes into a system. Since each OEM has several platforms as well as sub-platforms of products, managing this supply chain could be quite cumbersome. PLL devices resolve this problem by generating different frequencies using software at the designer's desk, which not only simplifies design, but also allows purchasing to procure a single device for multiple platforms.

- **EMI Reduction by Spread-Spectrum Clocking:** PCBs for consumer systems are designed with many layers, with dedicated ground planes for keeping interference low. Several high-speed signals are routed carefully to help improve system performance and avoid crosstalk, skew, and signal integrity issues. PLL devices help alleviate these board design issues by offering features such as spread spectrum that reduce the peak energy of high-speed signals. All consumer products must pass stringent US and international regulations on EMI in order to be released to the market. The spread-spectrum approach reduces, and often eliminates, the need for ferrite beads, filters, coils, and chokes that add to the BOM.

- **Synchronized Outputs:** Some applications may require certain clock signals to be synchronized to each other. This feature is possible with PLL devices, but may not be achievable with discrete crystals only.

- **Power Management:** Programmable PLL-based clock generators can cater to the niche demands of the portable market including gaming, smartphones, personal media players, digital cameras, and camcorders. In these power intensive applications, certain frequencies can be turned off selectively using I2C or pinprogramming. This is not easily achieved with traditional crystal designs.

## 2    Replacing Crystals, Crystal Oscillators with Phase Locked Loops

TI offers a broad portfolio of Clocking ICs designed to meet the diverse needs of our customers. Depending on the customer system requirements on the number of output clock signals and their quality (in terms of jitter, stability), an appropriate device from the TI clocking portfolio can be selected. The CDCE(L)9xx family of devices contain multiple general purpose PLLs that are typically used to replace crystals or crystal oscillators intended for clocking processors and/or medium speed asynchronous serial links. The CDCM6208, LMK03806 and CDCM6100x family of devices contain a high performance PLL capable of producing very low jitter clock outputs and are typically used to replace high performance crystal or SAW oscillators intended for clocking high speed asynchronous serial links, CDCM6208 provides the flexibility to also generate unrelated general purpose clock signals for clocking processors and/or other medium speed asynchronous serial links. The LMK03806 and CDCM6208 can also be used to provide clock signals at their outputs that are sychronized to backplane clock inputs for line cards of sychronous systems like SONET/SDH. LMK03806 is currently the lowest phase noise clock generator in the industry.

## 2.1 *CDCE(L)9xx*

The CDCE(L)9xx family of devices contain multiple general purpose programmable PLLs that are capable of generating up to 9 independent frequencies at each single ended output from a single reference crystal with a total jitter of 60ps, p-p typical and each PLL is capable of generating spread spectrum on the associated clock outputs. The devices also include an on-chip EEPROM that allows for customized startup modes per system needs. For A/V applications that require the ability to tune the clock frequency, the devices can replace use of traditional VCXOs and have in-built capability to act as a VCXO with up to +/-150ppm tuning range (please refer to SCAA085 for more details).

* CDCE913: 1 PLL, 3 LVCMOS outputs, 1.8V core, 2.5V or 3.3V I/O
* CDCEL913: 1 PLL, 3 LVCMOS outputs, 1.8V core and I/O
* CDCE925: 2 PLL, 5 LVCMOS outputs, 1.8V core, 2.5V or 3.3V I/O
* CDCEL925: 2 PLL, 5 LVCMOS outputs, 1.8V core and I/O
* CDCE937: 3 PLL, 7 LVCMOS outputs, 1.8V core, 2.5V or 3.3V I/O
* CDCEL937: 3 PLL, 7 LVCMOS outputs, 1.8V core and I/O
* CDCE949: 4 PLL, 9 LVCMOS outputs, 1.8V core, 2.5V or 3.3V I/O
* CDCEL949: 4 PLL, 9 LVCMOS outputs, 1.8V core and I/O

The CDCE949 has architecture as shown in Figure 1 and is representative of the architecture of its family of products.



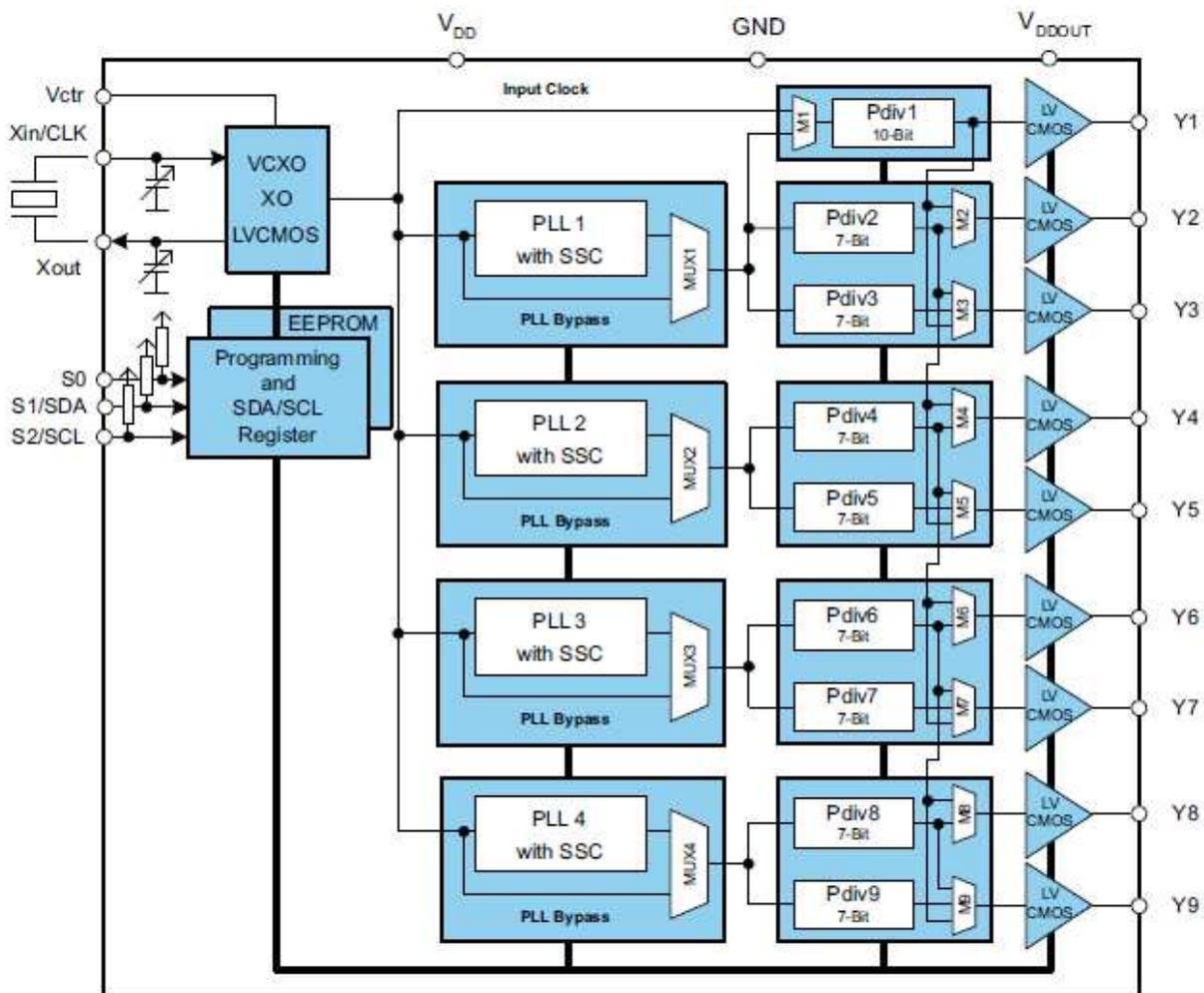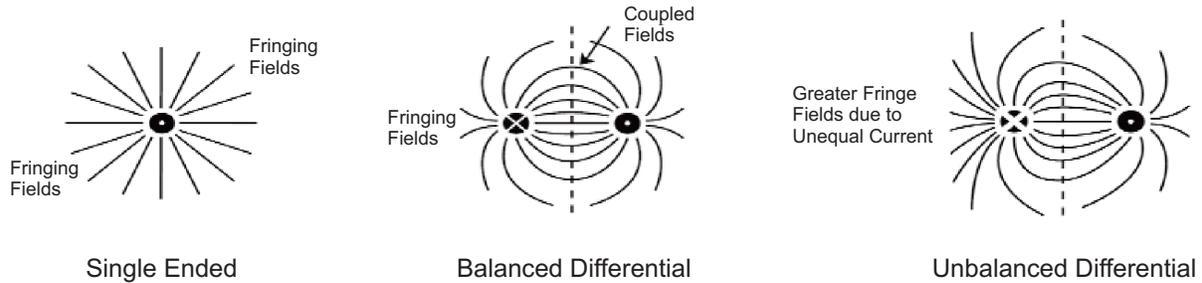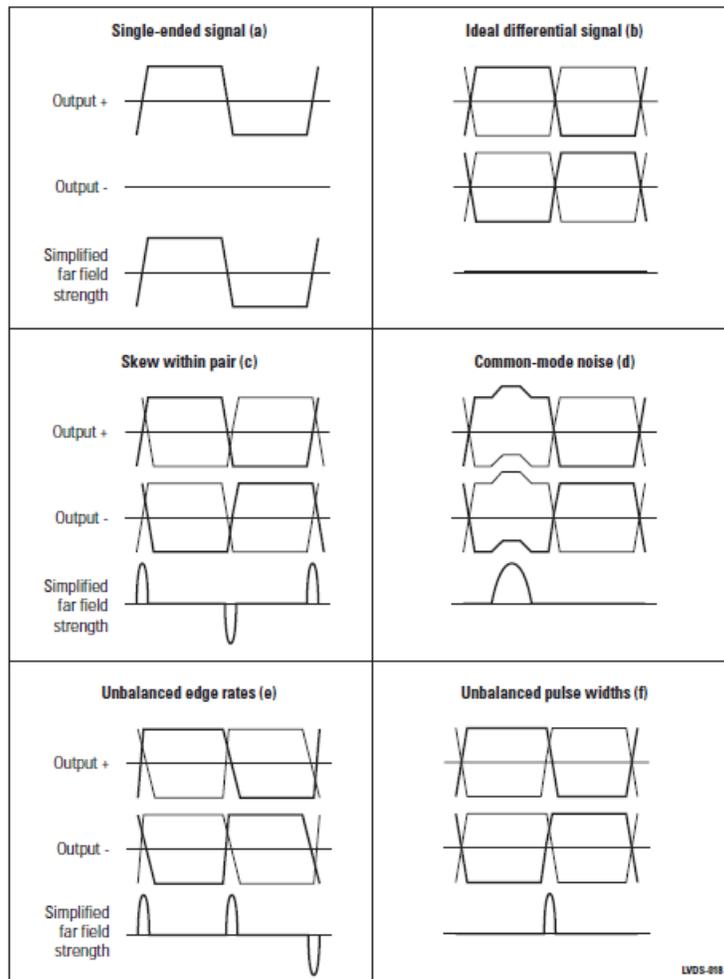**Figure 1. CDCE949 Block Diagram**

### 2.1.1    EMI Fundamentals

EMI is electromagnetic interference, or unintentional radiation of radio signals from an electronic circuit. Clock signals can contribute significantly to measured emissions because of the fast edge rates and any improperly terminated traces carrying clock signals on the PCB. As shown in Figures 2 and 3, single ended signals emit maximum radiation due to its fringe fields that escape in all directions, a fully balanced differential signals do not emit as the fields are canceled and do not escape, whereas unbalanced differential signals emit some radiation due to uncanceled fringe fields that escape.

**Figure 2. Radiation from Single Ended and Differential Signals**

**Figure 3. Far Field Strength from Single Ended and Differential Signals**

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### 2.1.2 CDCE949 Block Diagram

The CDCE(L)9xx family is capable of suppressing EMI on the clock outputs by generating spread spectrum clocking (SSC). SSC can be center-spread or down-spread. SSC is a frequency modulation scheme that reduces EMI without additional external components. When SSC is disabled, the clock signal has its signal power concentrated at its harmonic frequencies. When SSC is enabled, the clock signal is modulated to have its signal power spread around its harmonic frequencies while lowering the peak power and this reduces the EMI emission. CDCE(L)9xx allows the user to select between center-spread SSC and down-spread SSC, modulation frequency, the modulation depth (percentage of the clock spread) and the SSC profile. Figure 4 shows an example of utilizing SSC to meet EMI regulations.
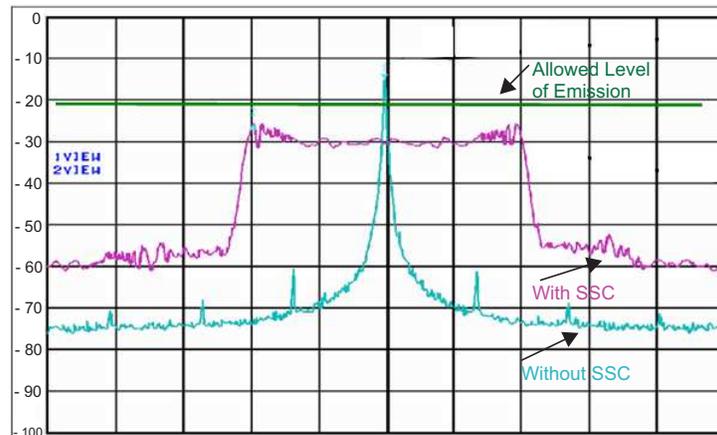


**Figure 4. Example SSC to Meet Regulation Standards**

#### 2.1.2.1 Down-Spread

Upon frequency modulation of output, the highest frequency of modulation is the nominal output frequency. As a result, the actual average output frequency measured across several clock cycles will be lower than the desired nominal output frequency. Figure 5 shows an example of down-spread SSC.
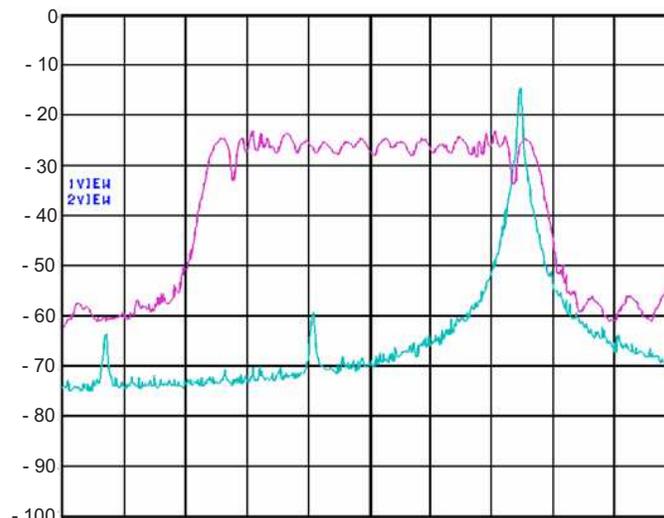


**Figure 5. Down-spread**

### 2.1.2.2    Center-Spread

Upon frequency modulation of output, the frequency of modulation is around the nominal output frequency. As a result, the actual average output frequency measured across several clock cycles will be same as the desired nominal output frequency. Figure 6 shows an example of center-spread SSC.
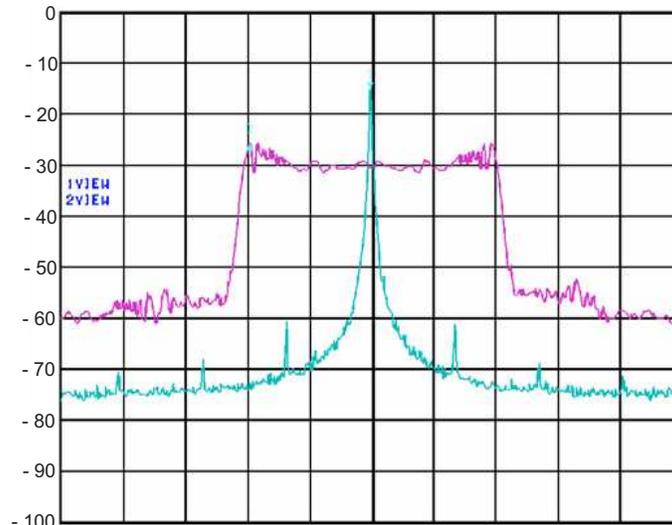


**Figure 6. Center-spread**

### 2.1.2.3    Modulation Depth and Frequency

Modulation depth is the percentage of clock spread and modulation frequency is the frequency with which the signal is changed. Appropriate selection of the modulation depth is important as too-low number would result in interference on audio signals and too-high number would result in unwanted side-effects like too much additive jitter. Figure 7 shows an example of modulation signal.
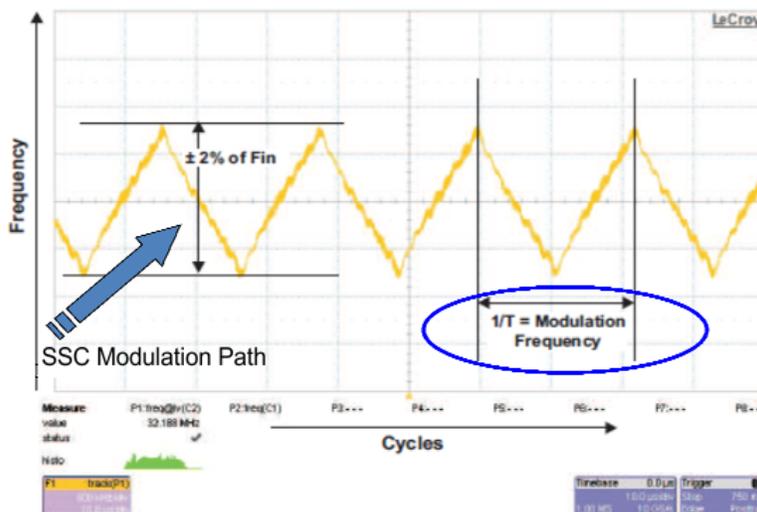


**Figure 7. Example Modulation Signal**

### 2.1.2.4 Spread Function

To allow for a even frequency distribution of the spread signal, one has to use a special function to sweep through the spread frequency range. Common spread functions are sawtooth, hershey, and sinusoidal. The best option is the hershey profile but since it is hard to create in practice, a closely resembling triangular spread is created. One drawback of the triangular spread is that it doesn't create a completely even frequency spectrum. Figure 8 shows the different spread functions.
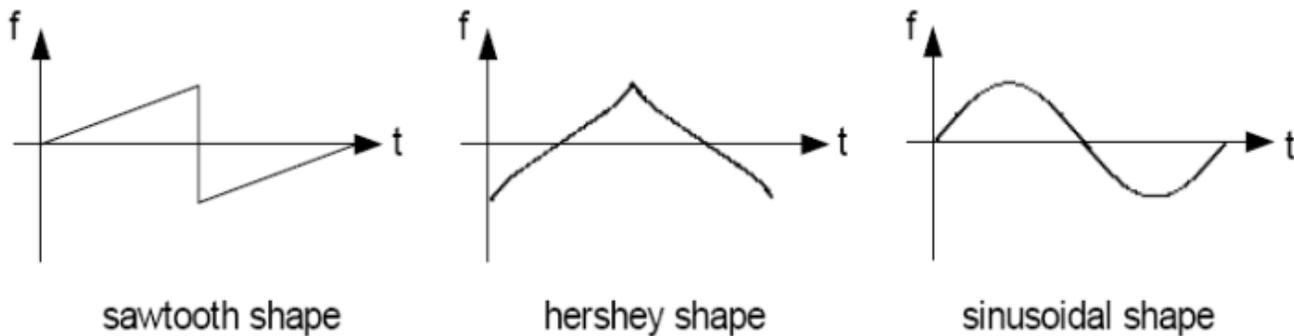


**Figure 8. Spread Functions**

### 2.1.2.5 Maintaining Signal Integrity

For high frequency signals, any trace should be treated as a transmission line if the following condition is met:

$$L \geq \frac{2}{7 \times f_{max} \times 6 \times t_{PR}}$$

where

- L is the trace length
- $f_{max}$ is the maximum signal frequency
- $t_{PR}$ is the signal propagation delay and is between 150ps/inch to 175ps/inch for FR4 PCB dielectric material. (1)

Transmission lines are defined by their characteristic impedance, which is given by the square-root of the ratio of their series inductance per unit length and their shunt capacitance per unit length. Commonly used transmission lines have a 50Ω characteristic impedance. Signal reflections between the source and the receiver occur if their respective impedances are not closely matched to the transmission line's characteristic impedance. In order to avoid these reflections, the LVMOS output needs to have a 50Ω source impedance. The LVCMOS output drivers in CDCE(L)9xx family have an 32Ω nominal output impedance. Thus a series termination resistor of 18Ω is recommended on all output clock traces to ensure proper termination and avoid reflections. In addition, it is recommended for the clock traces to be routed on internal layers to minimize any emissions and adjacent clock traces that are not pairs should be adequately spaced to minimize crosstalk. Figure 9 shows the recommended source termination.
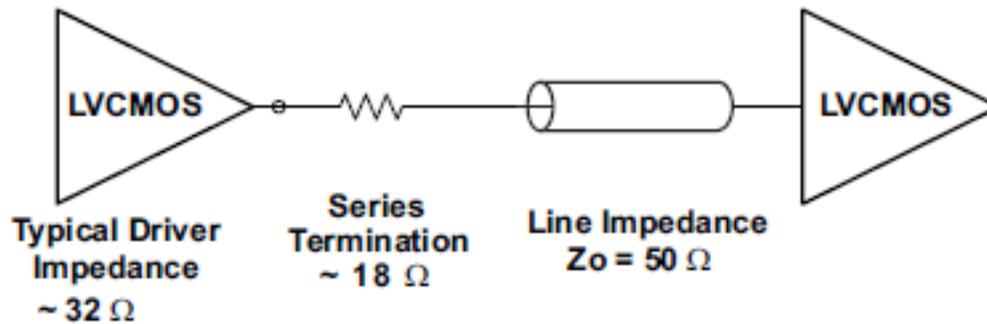


**Figure 9. Recommended Source Termination for CDCE(L)9xx**

To minimize coupling between LVCMOS signals, % of return current density (which is the path of least resistance and least inductance for return currents) through the reference plane for each trace should be minimized to less than 4%. The return current density is a function of the ratio of distance from edge of signal trace (D) to depth of reference place from signal trace (h). It is recommended to keep a ratio of 5 to ensure a return current density of 4%. A ratio of 10 ensures a return current density of 1%. Figure 10 shows the return current path for LVCMOS signals. Return current density is given by:

$$J_{RP} = \frac{i}{h \times \pi \left( 1 + \left( \dfrac{D}{h} \right)^2 \right)}$$
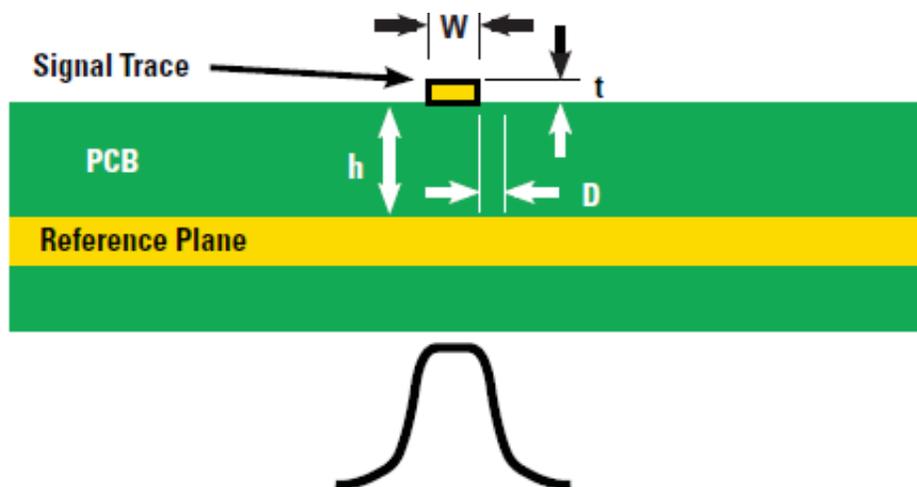
(2)



**Figure 10. Return Current Path for LVCMOS Signals**

## 2.2  *CDCM6208, LMK03806, CDCM6100x*

The CDCM6208 contains high-performance low-jitter programmable PLL with 4 output fractional dividers that are capable of generating up to 6 independent frequencies and up to 5 unrelated frequencies at each differential or single ended output from a single crystal or external clock source at the input with a total jitter of 15ps, p-p using integer dividers and 60ps, p-p using fractional dividers. The CDCM6208 has architecture as shown in Figure 11.
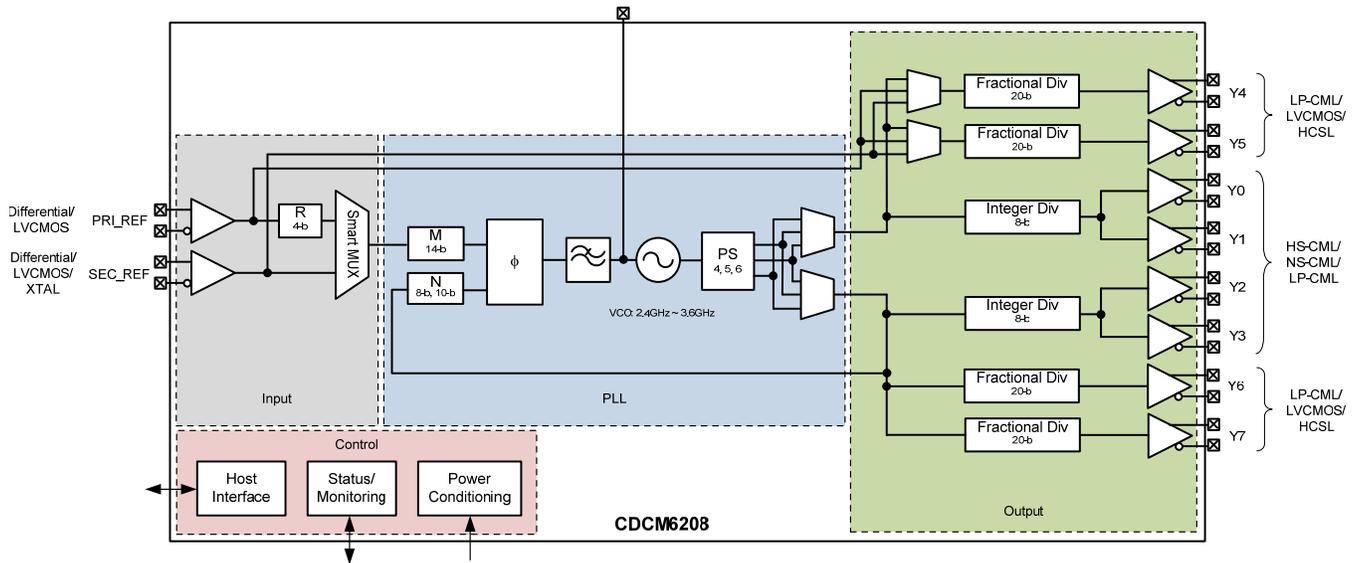


**Figure 11. CDCM6208 Block Diagram**

The LMK03806 contains high-performance ultra low-jitter programmable PLL that are capable of generating up to 7 independent frequencies at each differential or single ended output from a single crystal or external clock source at the input with a total jitter of 5ps, p-p. The LMK03806 has architecture as shown in Figure 12.
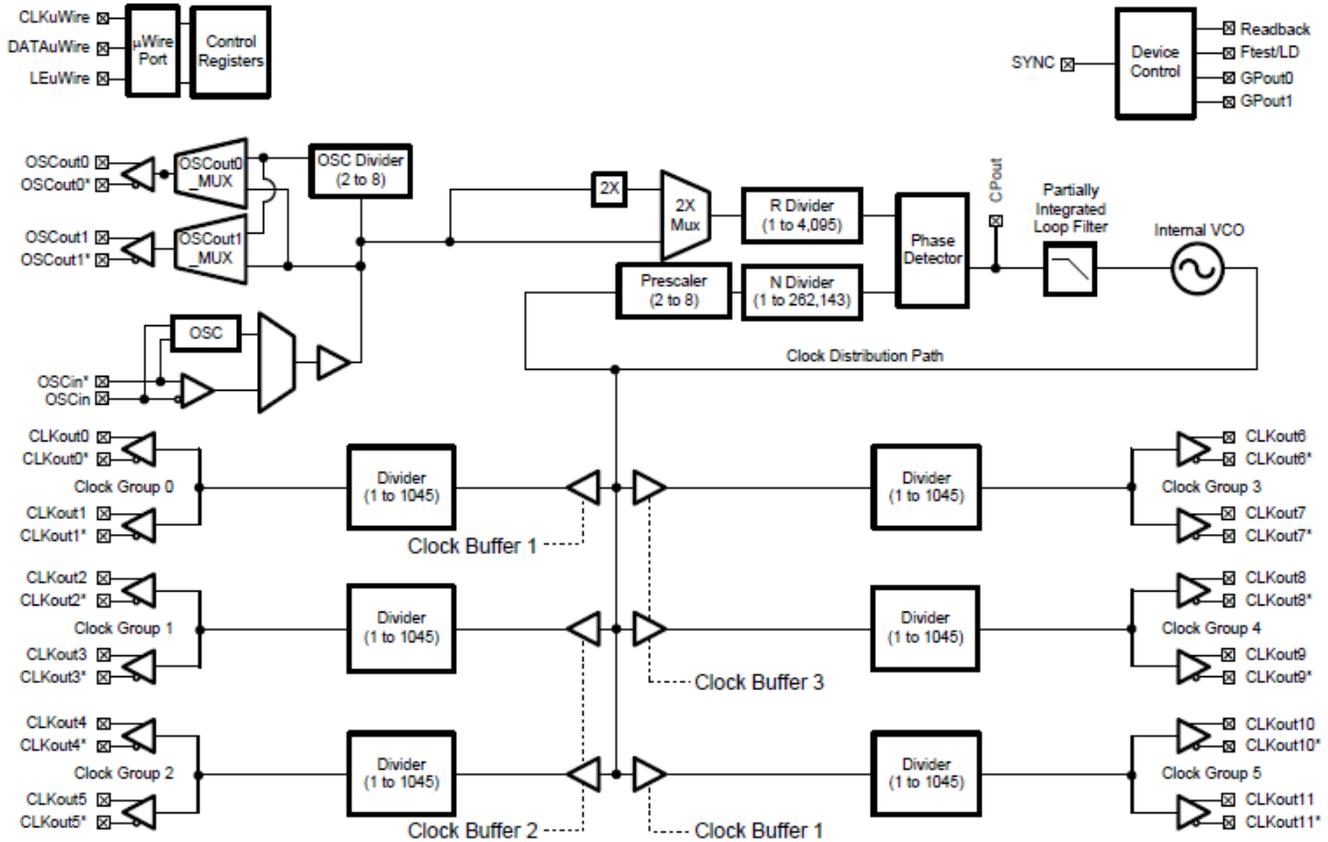


**Figure 12. LMK03806 Block Diagram**

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The CDCM6100x family of devices contains high-performance low-jitter pin-programmable PLL that are capable of generating a frequency at all differential or single ended output from a single crystal or external clock source at the input with a total jitter of 20ps, p-p.

The devices that make up this family are:
- CDCM61001: 1 PLL, 1 pair of differential outputs or 2 LVCMOS outputs, 1 LVCMOS bypass output.
- CDCM61002: 1 PLL, 2 pairs of differential outputs or 4 LVCMOS outputs, 1 LVCMOS bypass output.
- CDCM61004: 1 PLL, 4 pairs of differential outputs or 8 LVCMOS outputs, 1 LVCMOS bypass output.

The CDCM61004 has architecture as shown in Figure 13 and is representative of the entire family.



**Figure 13. CDCM61004 Block Diagram**

## 2.2.1    EMI Suppression

As shown in Figure 2 and Figure 3, single ended signals emit maximum radiation due to its fringe fields that escape in all directions, fully balanced differential signals do not emit as the fields are canceled and do not escape, whereas unbalanced differential signals emit some radiation due to uncanceled fringe fields that escape. Impedance mismatches on single ended or differential signals result in reflections that increase emission.

### 2.2.1.1    *Single-ended Clock Signals*

Maintaining signal integrity is of paramount importance and the techniques discussed in Section 2.1.2.5 is relevant for CDCM6208, LMK03806 and CDCM6100x devices. In addition to matching clock signal output impedance and its routing on internal layers, CDCM6208 offers the flexibility to control the slew rate of LVCMOS outputs. When the output slew rate is reduced, the harmonic powers are reduced in amplitude and lowers emission. Figure 14 shows the impact of slew rate control on signal harmonics.
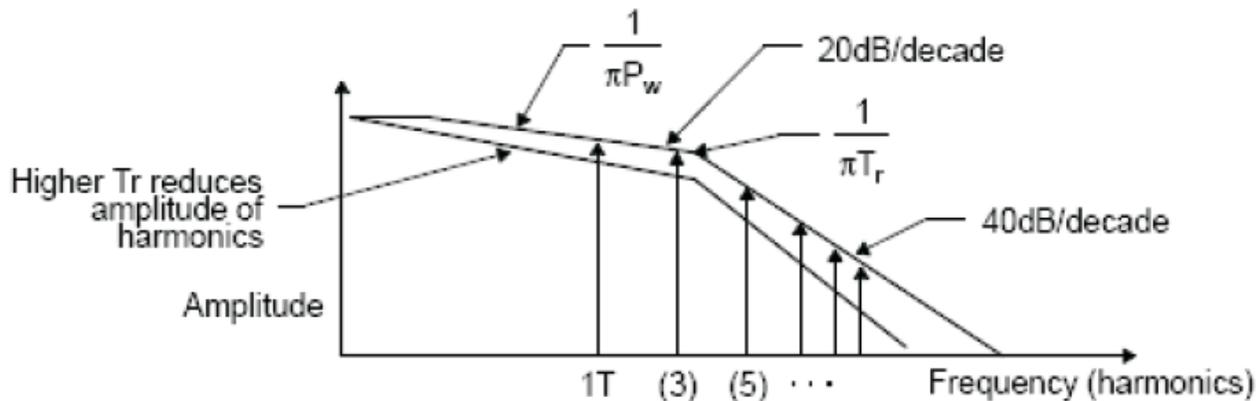


**Figure 14. Slew Rate Control of LVCMOS Outputs**

### 2.2.1.2    *Differential Clock Signals*

In order to avoid unbalanced differential clock signals as shown in Figure 2 and Figure 3, the following guidelines should be followed in PCB design and layout for a differential clock signal pair:

• Minimize output impedance mismatch in signals of every pair

• Tightly couple and symmetrically route signals in every pair

• Closely match the length of each signal trace in every match to minimize output skew

• Route the clock signals on internal layers of board and increase separation between adjacent clock traces that are not pairs to minimize coupling

• Follow proper termination guidelines to eliminate reflections (AC termination resistors should be close to the source output pins and DC termination resistors should be close to the receiver input pins)

Figure 15 shows part of PCB design with a differential pair that follows the aforementioned recommendations. W represents the trace width of each leg of the pair, S is the separation between each leg of the pair, t is the trace thickness, and x is the separation of another signal trace from the differential pair.
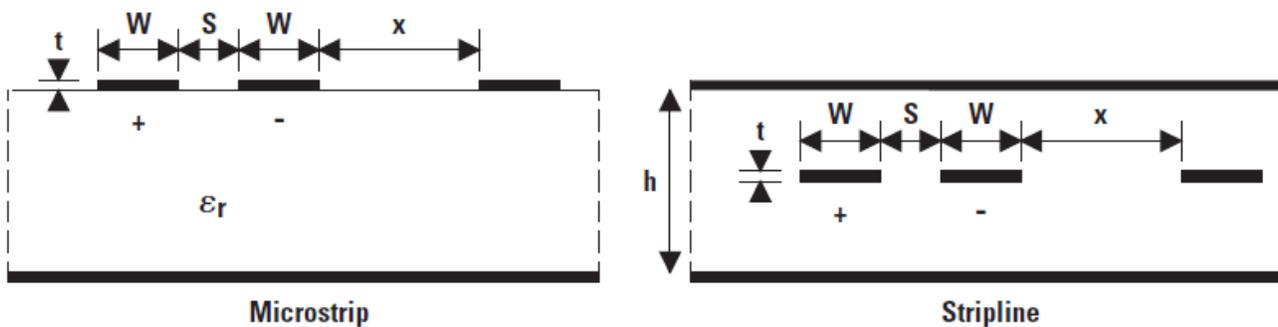


For good coupling, make $S < W$, $S < h$, and $x \geq 2W$ and $2S$

**Figure 15. Good PCB Design Techniques for Differential Signals**

## 3    End-equipment Examples and Device Recommendations

Table 1 lists TI clocking IC recommendations in various end-equipments to replace crystals and/or crystal oscillators.

**Table 1. End-equipment Currently Using Crystals/crystal Oscillators**
**and Recommendations Of TI PLL Devices**

| DESCRIPTION of EE | OPPORTUNITIES for CLOCKING | TI CLOCKING OPTIONS |
|---|---|---|
| Core Switch | Main control unit: CPU Clock, PCIe clock, Sys clock | CDCE62005, CDCM6208, CDCM6100x, CDCE(L)913, CDCE(L)925, LMK00304 |
| | Switch card: CPU, Switch, FPGA | CDCM6208, LMK03806, CDCE(L)913 |
| | Line card: Network processor, 10G port | CDCM6208, LMK03806, LMK04906, LMK00301, LMK00101, CDCLVPxxx |
| Data Concentrator, Collector and PLC | Applications Processor, Power Line Communication and Connectivity module | CDCE(L)913, CDC3S04 |
| Industrial PLCs - DCS | Analog Input module: One clock per ADC, one clock for microcontroller | CDCE(L)9xx, CDCLVCxxxx |
| | Analog output module: One clock for microcontroller, one clock per data converter | CDCE(L)9xx, CDCLVCxxxx |
| | Digital Input / Output module | CDCE(L)9xx |
| | Controller board: One clock per processor, replace crystals | CDCE(L)9xx |
| Inverter and Servo System | Servo driver - controller & driver: Clocking for FPGA, C2000 DSP | CDCE(L)9xx |
| Patient Monitoring System | Data acquisition cards (may need JESD204B support), processors | CDCE(L)9xx, CDCLVCxxxx |
| Power Automation | Data acquisition platform: Clock gen for processor, FPGA, ADC | CDCE(L)9xx |
| | Optical CT / PT: Clock source for all ADC's, FPGA's. Use one clock generator with multiple outputs or use one buffer with large fan-out | CDCE(L)9xx, CDCLVCxxxx |
| TV System | Clock for main processor with spread spectrum | CDCS501/3, CDCE(L)913, CDCE(L)925 |
| Ultrasound | Clock generator, clock buffer, jitter cleaner | LMK04906, LMK048xx, CDCLVPxxxx, LMK01010, LMK0030x |
| Video Security | Clock for main processor with spread spectrum | CDCM9102, CDCS501/3, CDCE(L)913, CDCE(L)925 |

Table 2 lists the integrated phase noise and jitter requirements on the reference clock for serial IO applications that are currently addressed by crystals and/or crystal oscillators. The table also includes the PLL device recommendations from Texas Instruments.

**Table 2. Serial Link Standards Currently Using Crystals/crystal Oscillators and Recommendations Of TI PLL Devices[1]**

| STANDARD | REF CLOCK FREQUENCY (MHz) | SIGNAL RATE (Gbps) | MAX REF CLOCK JITTER (ps, p-p) | MAX REF CLOCK STABILITY (ppm) | OFFSET FREQUENCIES (Mhz) | | PLL DEVICE RX – MINIMUM RECOMMENDATION |
|---|---|---|---|---|---|---|---|
| | | | | | RX – MINIMUM RECOMMENDATION CDR BANDWIDTH (hgh-pass char) | TX – MAXIMUM PLL BANDWIDTH (low-pass char) | |
| Fibre Channel (SAN) | 106.25 132.8125 212.5 | 4.25 8.5 14.025 | 12.2 7.3 6.4 | ±100 | 0.637 | 10 | CDCM6208, LMK03806, CDCE6200x, CDCM6100x |
| Serial ATA (SATA) Serial SCSI (SAS) | 75 100 | 3 6 | 16 8 | ± 100 | 1.8 1.8 | 7.5 7.5 | |
| 10/100/1000 Mb Ethernet | 25 125 | 1.25 | 55 | ± 100 | 0.637 | 2.5 12.5 | CDCE(L)9xx |
| 10 Gb Ethernet | 156.25 161.1328125 | 3.125 (4 lanes) 10.3125 | 22 5.4 | ± 100 | 1.875 0.08 | 20 80 | LMK048xx, LMK03806, CDCM6208 |
| Infiniband | 100 200 | 2.5 5 | 24 12 | ± 100 | 1.5 | 10 | LMK03806, CDCM6208, CDCM6100x, CDCE6200x, CDCM9102 |
| XAUI | 156.25 | 3.125 | 22 | ± 100 | 1.875 | 20 | |
| RapidIO | 156.25 | 3.125 | 32 | ± 100 | 1.875 | 20 | |
| USB 3.0 | 50 250 | 5 | 40 | ± 500 | 3 | 5 25 | |
| USB 2.0 | 24 48 | 0.48 | 420 | ± 500 | 0.5 | 5 | CDCE9xx |
| PCI Express | 100 200 400 | 2.5 5 8 | 80 (Gen 1) 43 (Gen 2) 14 (Gen 3) | ± 300 | 0.1 1.5 1 | 1.5 Fref/2 20 | CDCM6208, LMK03806, CDCM6100x, CDCM9102, CDCE6200x |

[1] total jitter requirements for each standard is assumed to be 20% of the valid bit period)

## 4    Example Use Case with TI PLL Devices

Figure 16 shows an application example of a media streaming system where current implementation using crystals and a crystal oscillator can be replaced with CDCE949 and CDCE913.
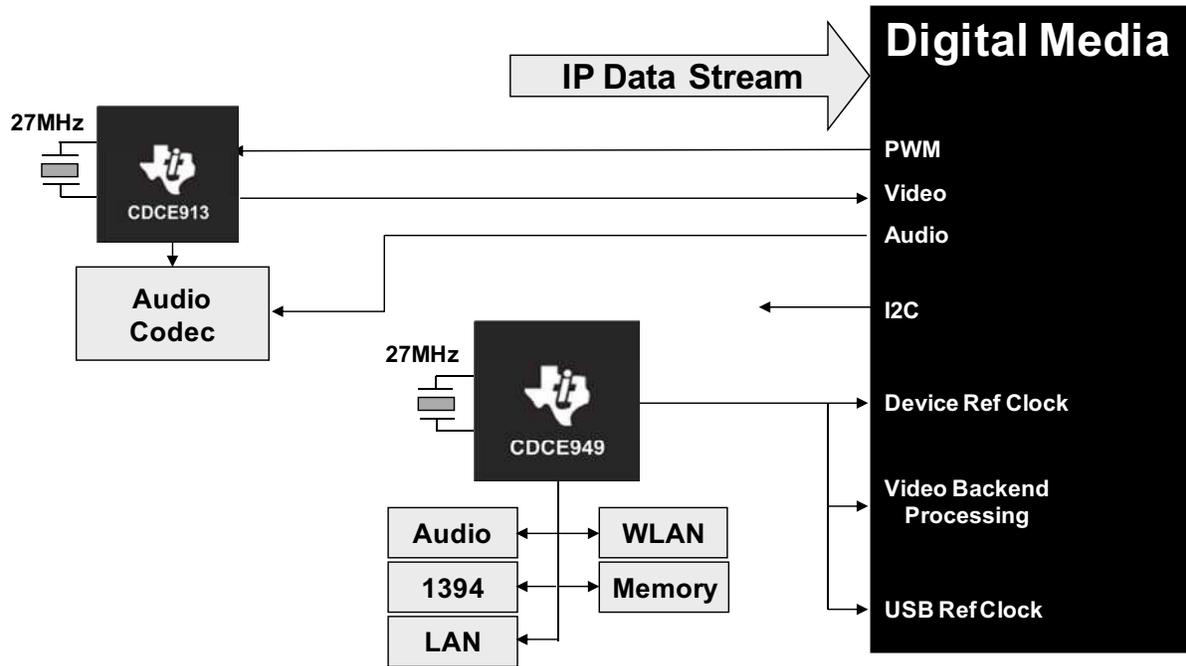
**Figure 16. Streaming Media Example with CDCE949, CDCE913**

Figure 17 shows an application example of a 10G ethernet switch where current implementation using crystals and crystal oscillators can be replaced with CDCM6208 or LMK03806.
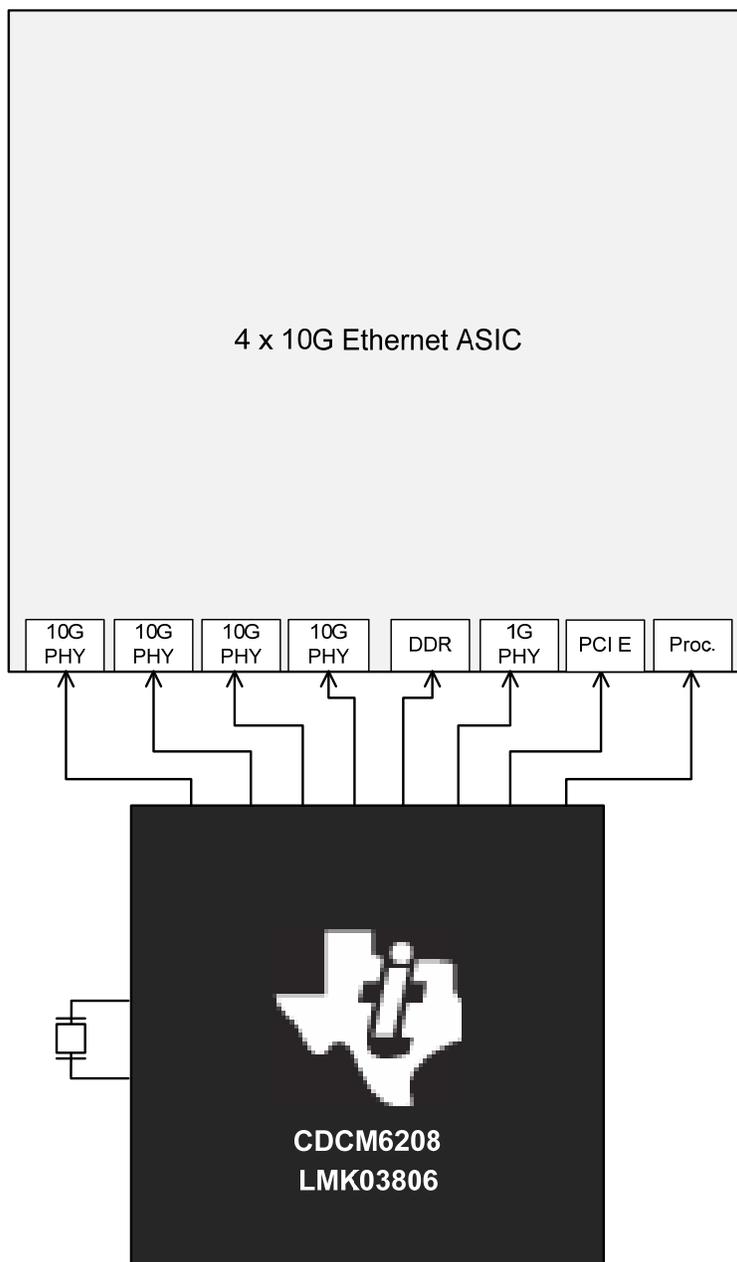


**Figure 17. 10 G Ethernet Switch Example with CDCM6208 or LMK03806**

# 5    PCB Design and Layout Guidelines

Following sections describe PCB design and layout guidelines for optimal performance of silicon based PLL devices.

## 5.1    *Signal Routing: Minimizing Coupling and Crosstalk*

Signal coupling happens when a signal affects another signal and results in reduced functionality or performance. In every situation there is an aggressor and a victim and many times they might exchange roles. Impedance, Signal Power and Isolation play a big role in determining the isolation between two signals. Isolation is the inverse of coupling. So to maximize isolation, coupling should be minimized.
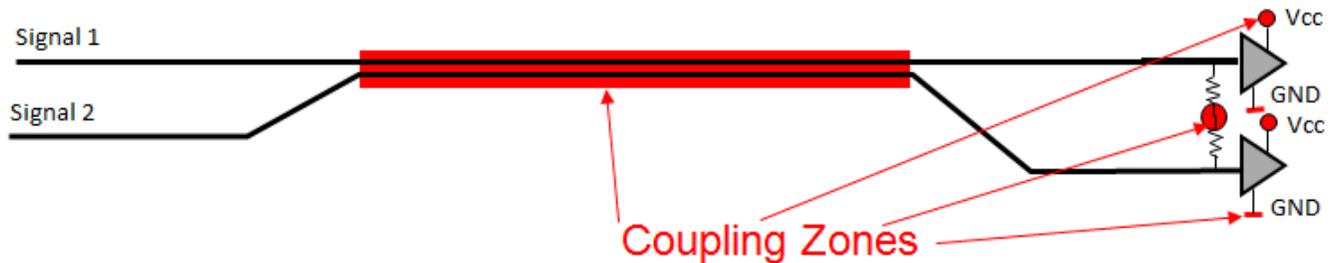


**Figure 18. Possible Coupling Zones Between 2 Signals**

Figure 18 shows various regions marked in red where coupling could happen between 2 signals. To reduce coupling:

- Increase Isolation between aggressor and victim. Guidelines for LVCMOS signals are given in Section 2.1.2.5 and guidelines for differential signals are given in Section 2.2.1.2.
- Isolate the power supplies. Guidelines for supply design are given in Section 5.2.
- Watch out for Ground Bounce. Ensure that the device grounds are connected to the system ground with minimal inductance. Figure 19 shows a recommendation of proper connection in a QFN package of device ground to PCB ground layer through thermal vias and thermal slug for good contact with the package thermal pad. No solder mask should be present in the thermal dissipation pad.
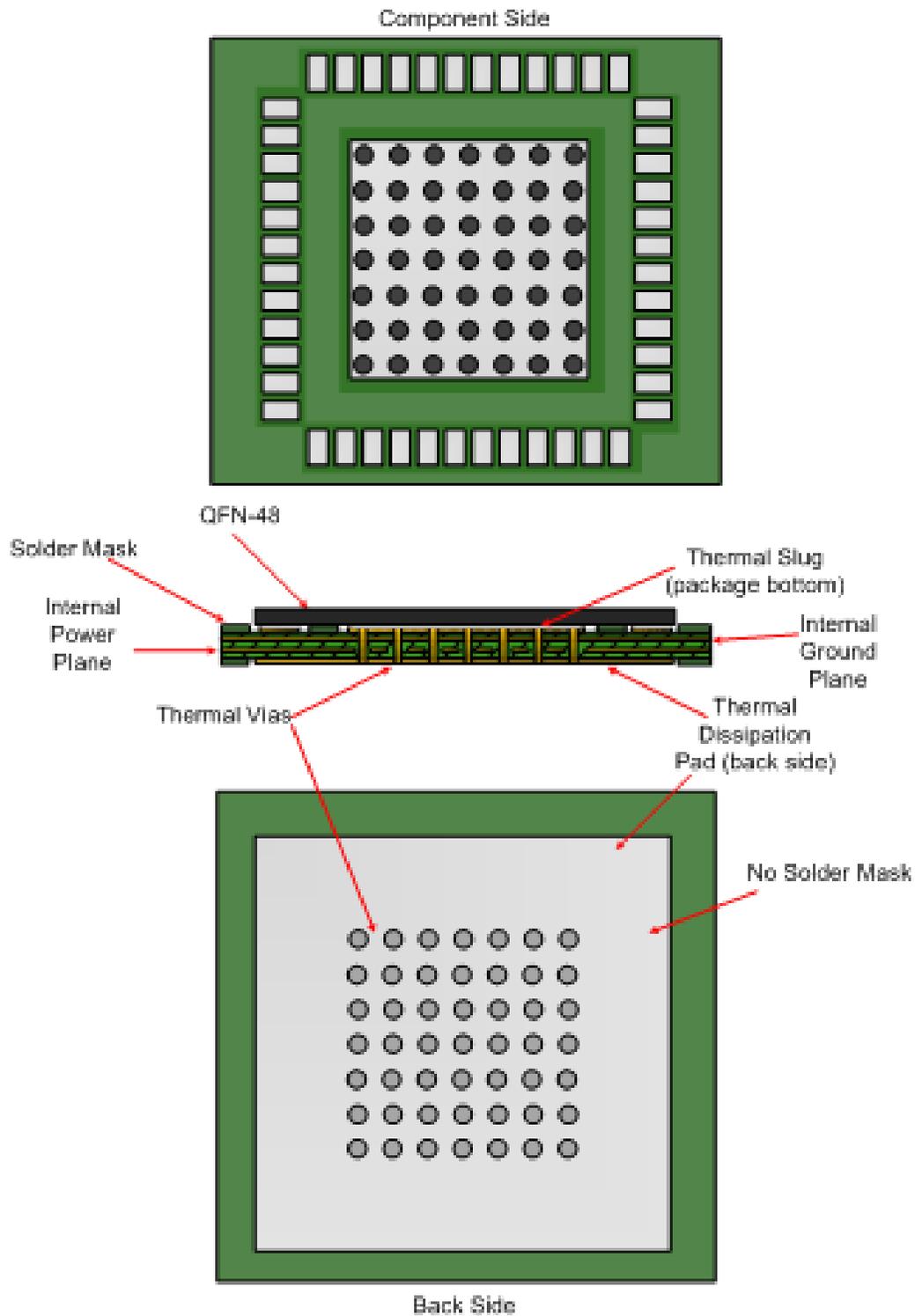
**Figure 19. Recommendation to Avoid Ground Bounce on QFN Package**

## 5.2 *Power Supply Design*

Section 5.2.1 and Section 5.2.2 detail the design of power supplies for PLL devices.

### 5.2.1 Power Supply Filtering

Power supply filtering is essential on any design in order to prevent board supply noise from leaking into the device and to prevent device supply noise from leaking to the board supply. PLL devices are very sensitive to noise on the power supply, which can dramatically increase the jitter of the PLL. It is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications. A PLL could, in certain cases depending on the source of coupling of the power supply noise, be able to significantly attenuate it.

Low frequency decoupling capacitors are used to eliminate the low frequency noise from the power supply for critical blocks of the PLL where as local bypass capacitors provide the very low impedance path for high frequency noise and guard the power supply system against the induced fluctuations. Inserting a ferrite bead between the board power supply and the chip power supply isolates the high frequency switching noises generated by the clock driver, preventing then from leaking into the board supply. A typical power supply filter is shown in Figure 20. For PLL devices with separate supplies for each output, they have to be supplied right at each output supply pin to minimize output frequency injection into the power network.
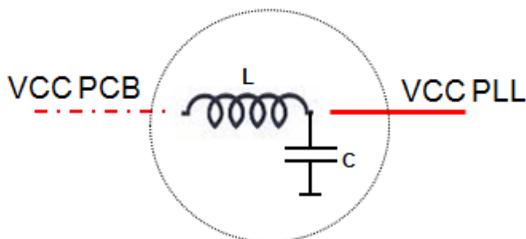


**Figure 20. Power Supply Filter**

### 5.2.2 Power Supply Decoupling

When a load is suddenly applied to a voltage source, the current through the power supply tries to suddenly increase, but its inductance acts to oppose that increase by lowering the voltage of the power supply. The job of a decoupling capacitor is to supply short bursts of current when the IC needs it. That is, it acts as a battery in the short term.

Decoupling capacitors between the power supply and ground lower the distributed impedance of a system, reduce the system noise and lower EMI. The values of the decoupling capacitors are chosen to provide the lowest impedance at the frequencies of interest. To ensure lowest impedance over a wide range, an array of closely spaced decoupling capacitors might be required. Figure 21 shows typical impedance characteristics across frequency of several capacitors with parisitics as indicated.
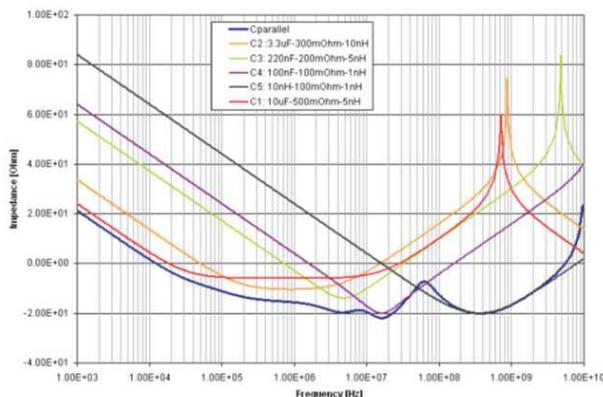


**Figure 21. Typical Capacitor Impedance Characteristics**

Good layout practices for routing decoupling capacitors are to avoid vias between them and the active device. Vias should instead be routed into the decoupling capacitors and then followed by the active device. Also best results are obtained when the decoupling capacitors are on the same layer as the active device. It is recommended to use more vias and widen trace widths. The distance between decoupling capacitors and active device should be minimized. Trace length to trace width should not exceed 3:1. Figure 22 shows an example of bad routing and Figure 23 shows an example of good routing.
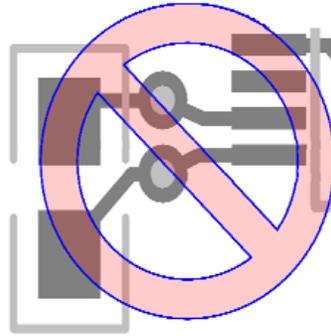


**Figure 22. Poor Routing of Decoupling Capacitors**
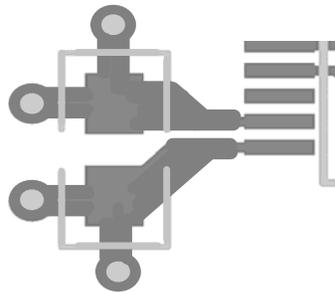


**Figure 23. Good Routing of Decoupling Capacitors**

# 6    Summary

Crystal based clocking solutions suffer from various drawbacks that affect the system performance, reliability and cost as outlined in this report. To overcome these system-level concerns, TI has a broad portfolio of silicon based PLL devices from which an appropriate device can be chosen based on the application requirements.

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