AN-1784 LMV1022 / LMV1023 Digital Output PDM Microphone Amplifier Demo Board

This application report describes the use of the LMV1022/LMV1023 Digital Output PDM Microphone Amplifier demo board.

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1 Introduction

The LMV1022/LMV1023 demo board provides a means for easy evaluation of digital PDM microphone amplifiers like the LMV1022, LMV1023, LMV1024 and LMV1026. The demo board has the LMV1022 and the LMV1023 in the 6 pin DSBGA package mounted ready for evaluation. This demo board also provides the means by using the DIP socket (U3) to evaluate parts on DIP conversion boards and offers a four pin interface (J16) to connect other digital PDM sources like microphones containing LMV1022 alike parts.

Starting at Version 1.3, the LMV1022 / LMV1023 demo board is designed for adding a small daughter board that can convert the digitized microphone signals from the I^2S interface at J19 back to analog audio. Adding the A/D daughter board enables easier demonstration of the digital microphones. The daughter board can also be used to perform measurements of the performance of the digital microphone in the analog world. The header at J22 is for the to supply to the daughter board.

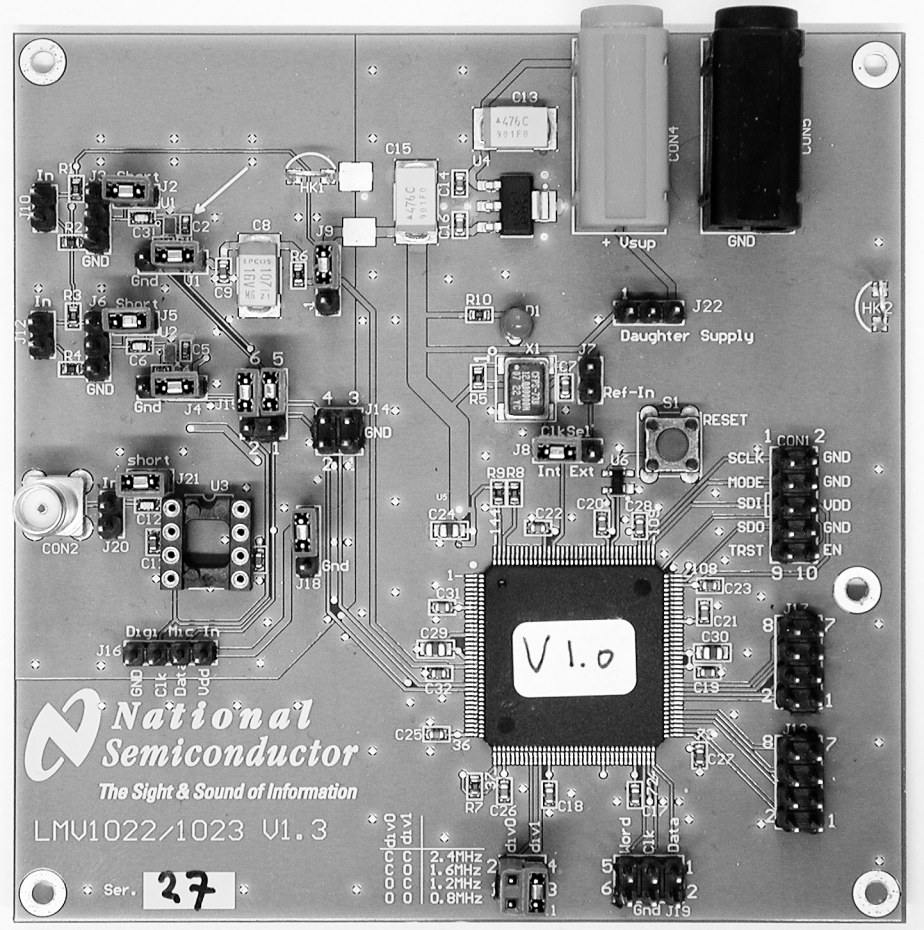

Figure 1. LMV1022 / LMV1023 Digital Output PDM Microphone Amplifier Demo Board

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2 General Description

The LMV1022 and LMV1023 integrate a pre-amplifier and a Sigma-Delta modulator which may be placed inside an electret condenser microphone (ECM). The output is a digital serial bit stream, ideal for 4-wire ECM. The LMV1022 and the LMV1023 are complementary stereo devices. The difference between the two devices is that the LMV1022 outputs the data on the rising edge of the clock signal while the LMV1023 does so on the falling edge. This makes these devices very suitable for stereo microphone applications, where the two microphones connect on the same bus

This next generation digital ECM containing parts like the LMV1022 and LMV1023 produces an over sampled single bit stream to be connected directly to a DSP in a digital audio system. The clock input of the LMV1022 / LMV1023 is a user adjustable clock frequency ranging between 960kHz and 2.4MHz. The LMV1022 / LMV1023 enable a very robust output of an ECM by eliminating the sensitive, low-level analog signal forming the output of a conventional JFET ECM. This also improves the RF immunity, eases system design, and reduces external components. Furthermore this different system partitioning of the Analog-to-Digital conversion enables an all-digital baseband processor in mobile communication systems.

By changing the clock frequency the LMV1022 and LMV1023 can be used in a wide range of applications ranging from the limited 3.4kHz voice bandwidth to full 20kHz audio bandwidth.

3 Operating Conditions

Temperature Range	$-40°C \le T_A \le 85°C$
LMV1022 / LMV1023 Power Supply Voltage	$1.6V \le V_{DD} \le 3.6V$
Demo board Power Supply Voltage	$4.5V \le V_{sup} \le 5.5V$

4 Board Features

The LMV1022 / LMV1023 Digital Output PDM Microphone Amplifier demo board has an on board voltage regulator (U4) converting the 4.5-5.5V (≈120mA) to the internal 3.3V supply voltage required for the FPGA . The demo board is equipped with a 12MHz XTAL oscillator (X1) which can generate the FPGA clock.

The demo board provides the means of easy evaluation of connected PDM microphones at four different frequencies by using the on board clock generator. J11 is used to select which of the four clock frequencies (960kHz, 1.2MHz, 1.6MHz, or 2.4MHz) is used. For testing at other clock frequencies an external clock source can be connected on the board at J7.

The FPGA has two decimation filters implemented in hardware and converts the PDM signal from the microphones to the standard I^2S signals which can easily be evaluated using test equipment like the Audio Precision.

The demo board provides two µSMD parts already mounted on the PCB for easy evaluation of the LMV1022 and the LMV1023 It also provides an interface to connect four wire PDM microphones for testing demonstration and evaluation.

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5 Block Diagram

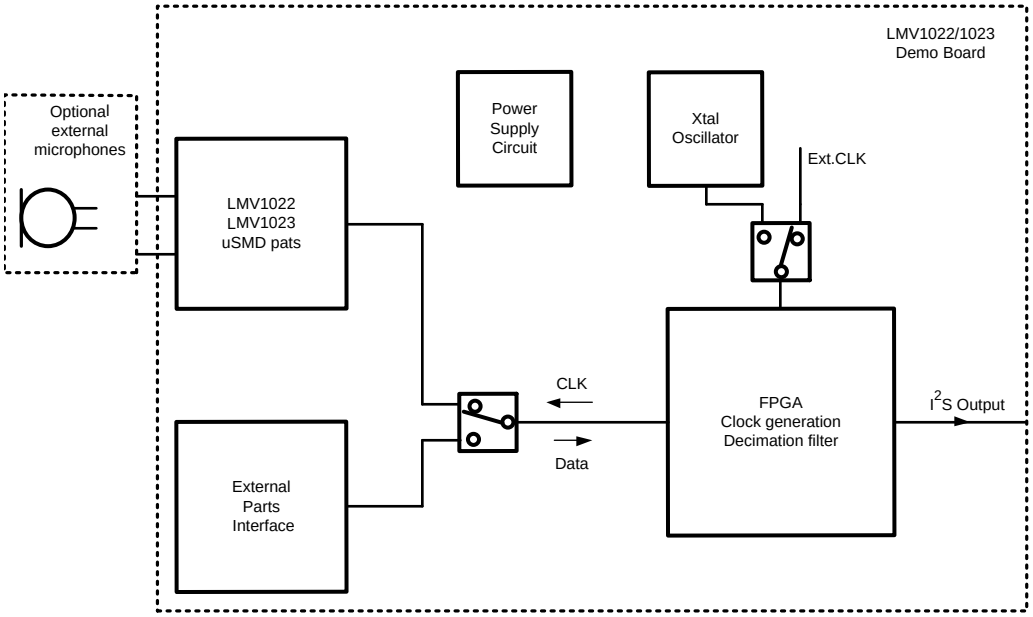

Figure 2. LMV1022 / LMV1023 Digital Output PDM Microphone Amplifier Demo Board Block Diagram

6 Evaluating the On-Board LMV1022 /LMV1023

The output signals of the LMV1022 and LMV1023 mounted on the board can be evaluated by connecting an I^2S slave to the I^2S outputs on J19, for example, the programmable Serial Interface of an Audio Precision PSIA2722, (see Section 11 and Section 14).

With the settings from Table 1, stereo operation of the on board LMV102 and LMV1023 can be evaluated for an audio bandwidth of 20kHz. These settings are illustrated in Figure 3.

Table 1. Default setting for evaluating the on board µSMD part

Designator	Function or Use	Connect
J1, J4	Power supply U1, U2	Short 2-3
J2	Input capacitor short circuit U1	Short
J3	Input for Audio test signal U1	Pin2 signal, Pin1=GND
J5	Input capacitor short circuit U2	Short
J6	Input for Audio test signal U2	Pin2 signal, Pin1=GND
J8	Clock source selection FPGA	1-2 = internal 12MHz
J9	DUT supply voltage	Internal analog supply =2-3 Short External analog supply = connected to 1-2
J11	Sample frequency 48kHz, see Table 5	2.4MHz microphone clock
J15	Selection of the source for FPGA input.	3-5 + 4-6 = both on board uSMD parts

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With the above settings, the board is ready to operate the two on board parts (LMV1022 and LMV1023) at the internal 3.3V power supply. For evaluation at other supply voltages, see Section 7.

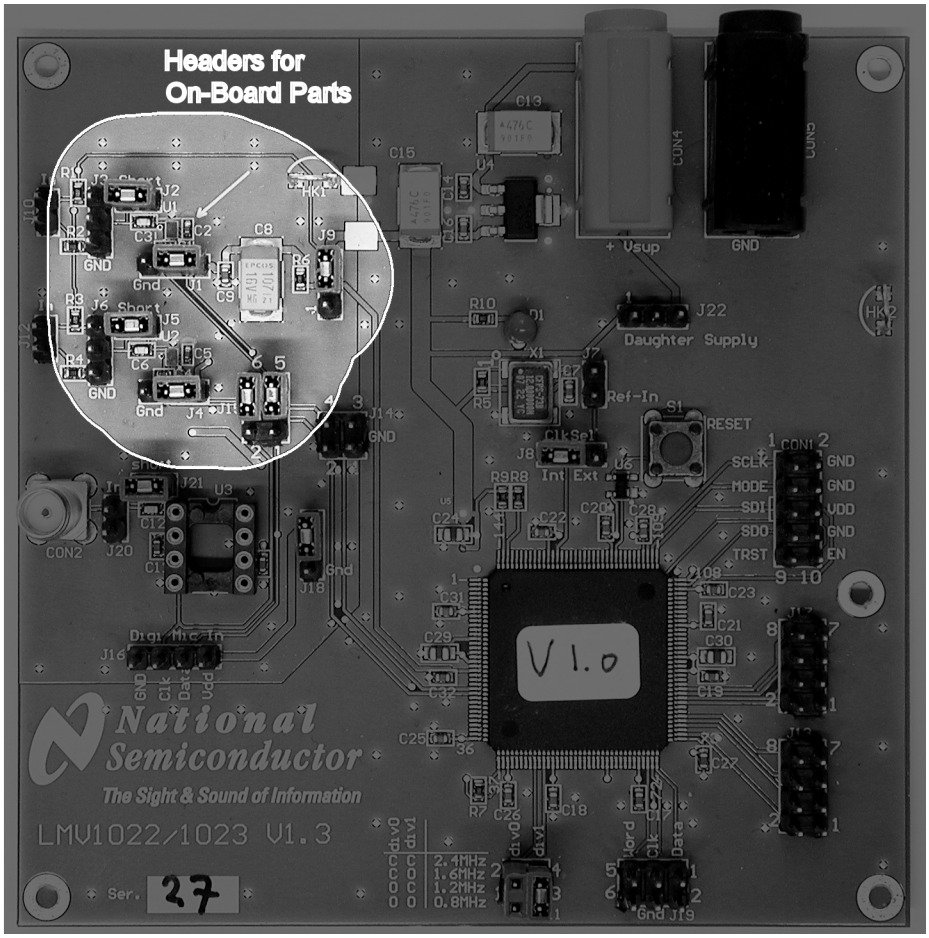

Figure 3. Setting for Testing the On Board LMV1022 and LMV1023

7 Evaluating at Other Supply Voltages

The LMV1022 and LMV1023 parts have a supply voltage range from 1.6V to 3.6V. The power supply on the demo board has a constant output voltage of 3.3V. The demo board also supports the external control of the microphone voltage. The board changes for external microphone voltages are as follows:

1. Remove the jumper from J9 (pin 2-3)
2. Apply external supply voltage within the 1.6V to 3.6V range at J9 between pin 1 and pin 2. Pin1=GND, Pin2=+V_{DD}

See Figure 4.

This will automatically adjust the thresholds and levels for the digital input- and output signals for the on board FPGA I/O and the device under test

When evaluating the parts at other supply voltages than the on board 3.3V supply, the FPGA is powered from the on board 3.3V voltage regulator Via +Vsup and GND. Only the I/O part interfacing with the device under test will follow the external supply voltage for correct logical threshold voltages. This only uses a few milliampere from the external supply source.

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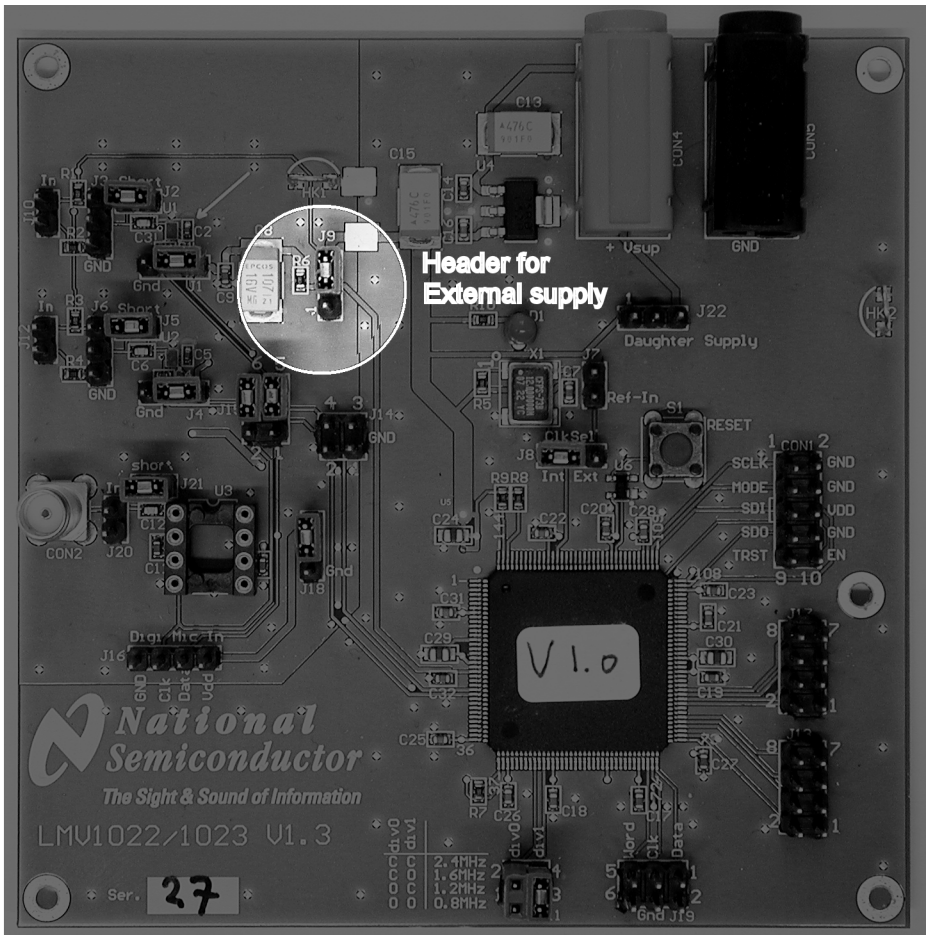

Figure 4. External Controlled Supply Voltage

8 Evaluation Using the DIP Socket

The LMV1022 / LMV1023 demo board is equipped with a DIP socket (U3). This can be used to evaluate and test parts on a conversion board or in a DIP8 socket see Table 3. The output signal from the part in the DIP socket can be evaluated by connecting an I^2S slave to the I^2S outputs on J19, for example, the programmable Serial Interface of an Audio Precision, PSIA2722. (see Section 11 and Section 14).

When the settings from Table 2 are used, the board is ready to operate the parts in the DIP socket at the internal 3.3V power supply. With these settings, operation of the part can be evaluated for an audio bandwidth of 20kHz (see Figure 5).

Table 2. Default setting for evaluating the part in the DIP socket

Designator	Function or Use	Connect
J8	Clock source selection FPGA	1-2 = internal 12MHz
J9	DUT supply voltage	Internal analog supply =2-3 Short External analog supply = connected to 1-2
J11	Sample frequency 48kHz, see Table 5	2.4MHz microphone clock
J15	Selection of the source for FPGA input.	1-3 + 2-4 = DIP socket U3 and PDM Microphone interface connector J16
J18	Power supply U3	Short 2-3
J20	Input for Audio test signal Part in DIP socket U3	
J21	Input capacitor short circuit U3	Short for noise measurement

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Table 2. Default setting for evaluating the part in the DIP socket (continued)

Designator	Function or Use	Connect
CON2	Coaxial input for connection to AC audio signal generator when testing with part in DIP socket U3	

Evaluation at supply voltages other then 3.3V is possible by using the settings from Section 7.

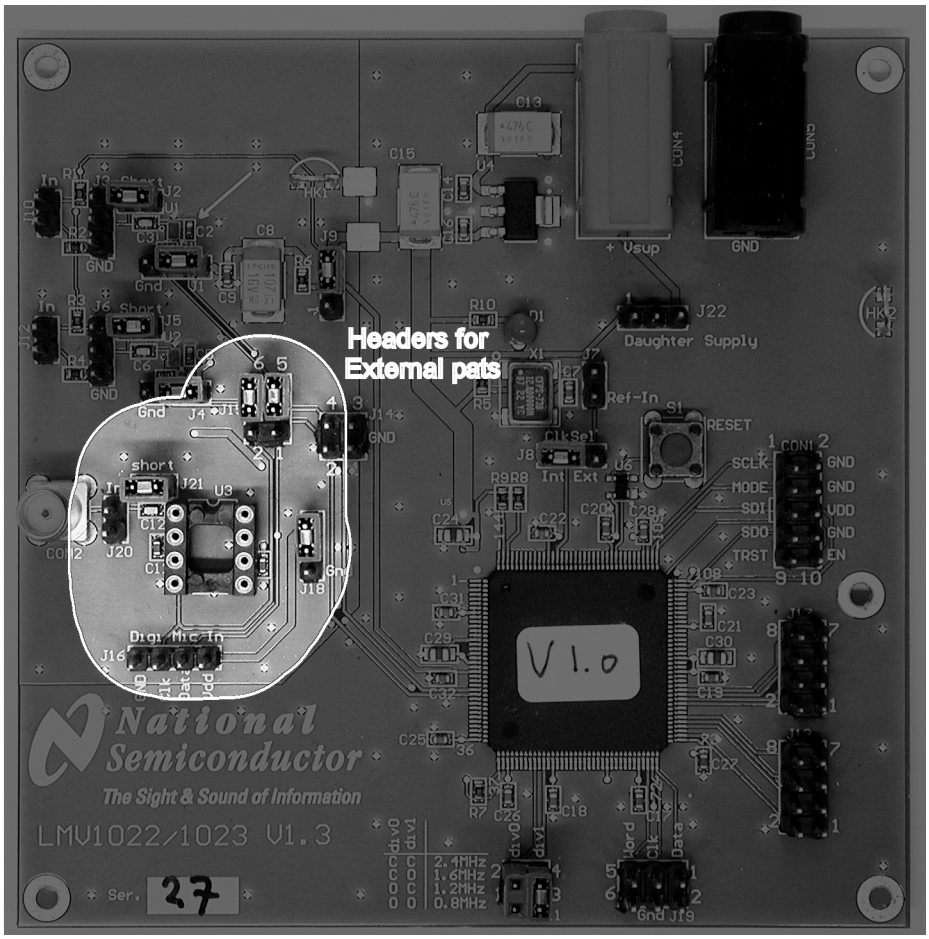

Figure 5. Settings for External Parts Connected to the Demo Board

Table 3. Dip Socket Pin Out

PIN	Function
1	Input
2	GND
3	V_{ref}
4	CLK
5	NC
6	V_{DD}
7	Data
8	NC

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9 Evaluation of Other PDM Parts and Microphones

The settings for evaluating other PDM parts and PDM microphones are the same as for evaluation using the DIP socket, as described in Section 8. The only difference is that the signals are now connected to J16 with the signals to the proper pin:

1. Ground (GND)
2. Clock (CLK)
3. Data
4. Supply (Vdd)

With the settings from Table 4, mono and stereo operation of the part(s) connected to J19 can be evaluated at an audio bandwidth of 20kHz.

Table 4. Default Setting for Evaluating other PDM Parts and Microphones

Designator	Function or Use	Connect
J8	Clock source selection FPGA	1-2 = internal 12MHz
J9	DUT supply voltage	Internal analog supply =2-3 Short External analog supply = connected to 1-2
J11	Sample frequency 48kHz, see Table 5	2.4MHz microphone clock
J15	Selection of the source for FPGA input.	1-3 + 2-4 = DIP socket U3 and PDM Microphone interface connector J16

Evaluation at supply voltages other then 3.3V is possible using the settings from Section 7.

10 On-Board Clock Generator

The clock frequency of the PDM microphone can be selected by placing the correct jumpers on header J11 as shown in Table 5. This header can be found at the bottom side of the PCB below the FPGA. See Figure 6.

Table 5. PDM Microphone Clock Frequency Selection

J11 Pins 1-2 / 3-4 (1)	Sample Frequency (kHz)	Clock Frequency (MHz)
C/C	48	2.4
C/O	32	1.6
O/C	24	1.2
O/O	16	0.8

(1) C = header Closed, O = header Open

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Figure 6. Clock Rate and I2S Interface

11 Connections to the Audio Precision (PSIA2722)

The demo board can be connected to the AP digital interface (PSIA2722) by using J19 and the connections as described in Table 6.

Table 6. Connections to an Audio Precision

Header-pin	Audio Precision Connector	Comment
J19-1	Data in	
J19-3	Bit Clk in	
J19-5	Frame Clk in	
J19-2,4,6	GND	
J7	Master CLK	See Section 12

12 Testing at Other Clock Frequencies

Header J7 can be used for applying an external clock signal to the FPGA. This will require that J8 is changed to use the external clock source 'EXT' (see Figure 7) When using the external FPGA clock there is more freedom in choosing the clock frequency used by the decimation filter and the clock frequency of the LMV1022 / LMV1023 . In this mode of operation of the demo board, the formula below gives the resulting clock frequency assuming both jumpers on J11 are closed.

The duty cycle of the external clock signal must be between 45% and 55% .

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$$\text{LMV1022 clock frequency} = \frac{\text{Applied Clock J7}}{5} \quad (1)$$

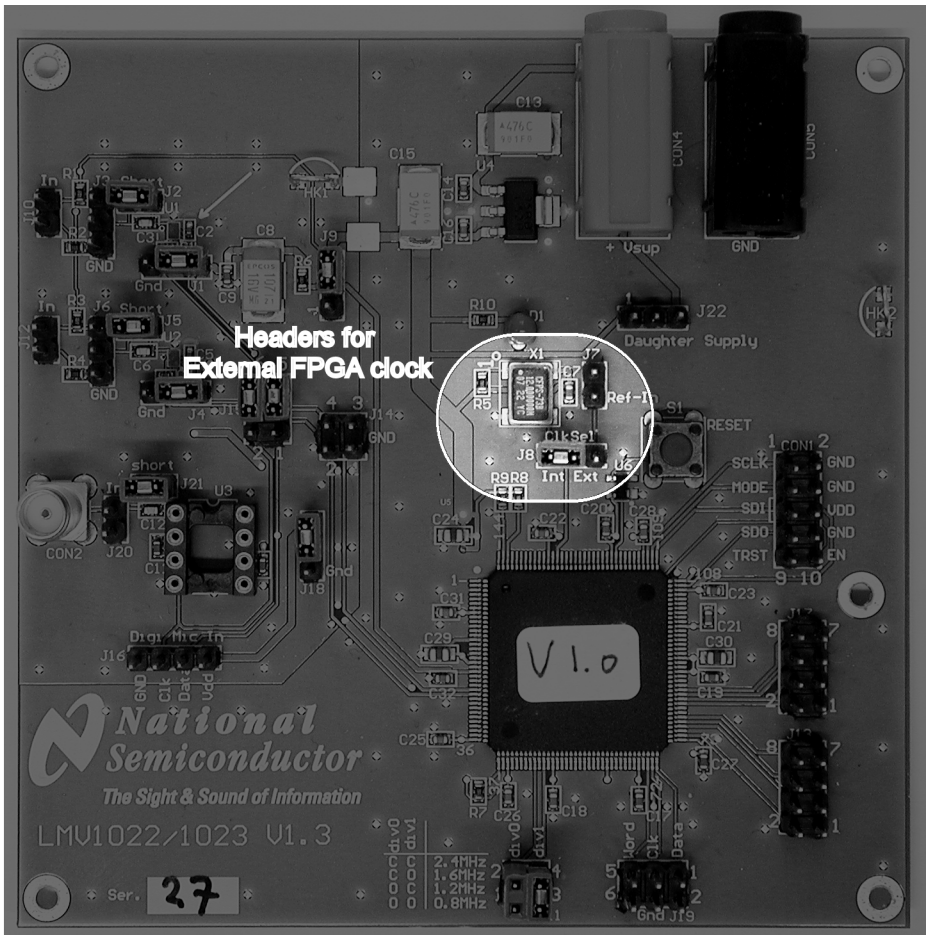

Figure 7. External FPGA Clock

13 Description of Jumpers and Connectors on the LMV1022 / LMV1023 Demo Board.

Most of the functions that are controlled by the jumpers on the LMV1022 / LMV1023 demo board are also indicated on the PCB in silk-screen as shown in Figure 1 and Figure 13.

Table 7. Connector/Header Function

Designator	Function or Use	Comment
HK1, HK2	Ground connection for probes	
J1	Power supply U1	1-2 = Connect External Analog supply 2-3 = Short, Internal Analog supply
J2	Input capacitor short circuit U1	Short for noise measurement
J3	Input for Audio test signal U1	
J4	Power supply U2	1-2 = Connect External Analog supply 2-3 = Short, Internal Analog supply
J5	Input capacitor short circuit U2	Short for noise measurement
J6	Input for Audio test signal U2	From an Audio precision source.
J7	External clock input FPGA	
J8	Clock source selection FPGA	1-2 = internal 12MHz 2-3 = external clock

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Table 7. Connector/Header Function (continued)

Designator	Function or Use	Comment
J9	DUT supply voltage	1 -2 connect external supply 2-3 Short, internal supply
J10	Microphone input part U1	
J11	Microphone Clock divider Frequency selection header.	See Table 5
J12	Microphone input part U2	
J13	General purpose outputs	Not Used
J14	Monitor output for digital microphone digital interface signals	1-2 = Microphone clock 3-4 = microphone Data
J15	Selection of the source for FPGA input.	3-5 + 4-6 = on board µSMD parts 1-3 + 2-4 = DIP socket U3 and PDM Microphone interface connector J16
J16	PDM Microphone interface connector	To connect one or two (stereo) PDM digital microphones (LMV1022 + LMV1023 or LMV1024 + LMV1026)
J17	General purpose inputs	Not Used
J18	Power supply U3	1-2 = External Analog supply 2-3 = Internal Analog supply
J19	I^2S interface	See Table 6
J20	Input for Audio test signal Part in DIP socket U3	
J21	Input capacitor short circuit U3	Short for noise measurement
+RED	+ Supply voltage	4.5V < V_{sup} < 5.5V
- Black	- Supply voltage	
CON1	JTAG interface	Programming the FPGA
CON2	Coaxial input for connection to AC audio signal generator when testing with part in DIP socket U3	

14 Settings of the Audio Precision SYS2722/ PSIA2722

When using the AP-SYS2722, it is important to use the correct settings. These settings are shown in Figure 8.

The digital I/O must be set as shown in Figure 9.

Sometimes the PSIA has a problem getting a stable lock on the input signal; therefore, it is preferred to use the *'DIO Rate Ref' setting'* for the *'Scale frequency by :'* parameter.

In the digital Analyzer, the different parameters can be measured as shown in Figure 10. Make sure that The DSP audio analyzer is selected and that the input from the *Digital @ ISR* is selected.

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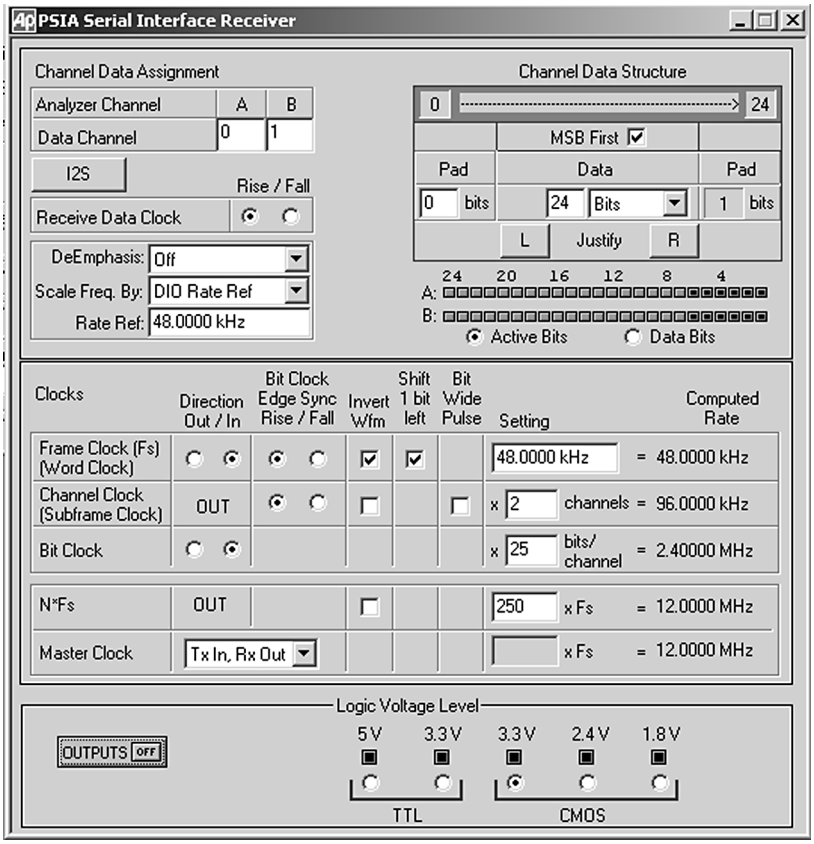

Figure 8. PSIA 2722 Settings

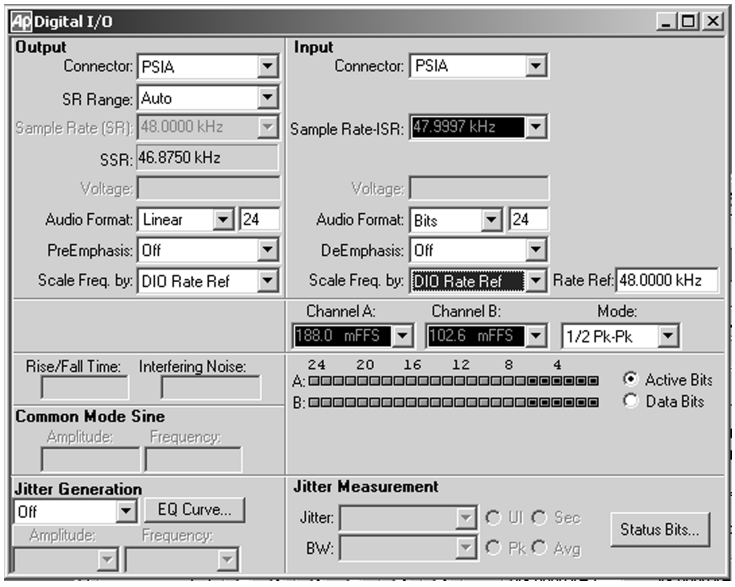

Figure 9. Audio Precision Digital I/O Setting

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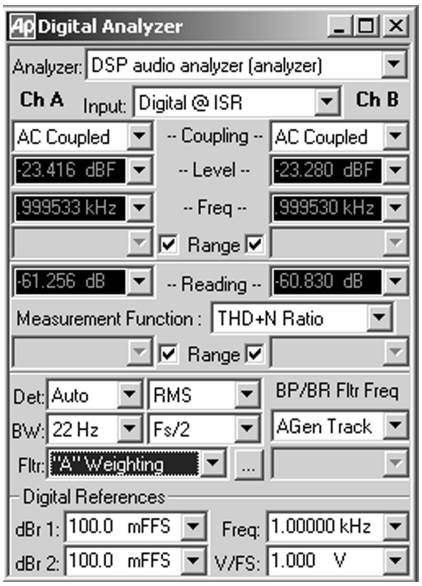

Figure 10. Digital Analyzer

15 D/A Converter Daughter Board

Starting at version 1.3, the LMV1022 / LMV1023 demo board provides the means to plug on a small D/A convertor daughter board. The mounted D/A daughter board is shown in Figure 11.

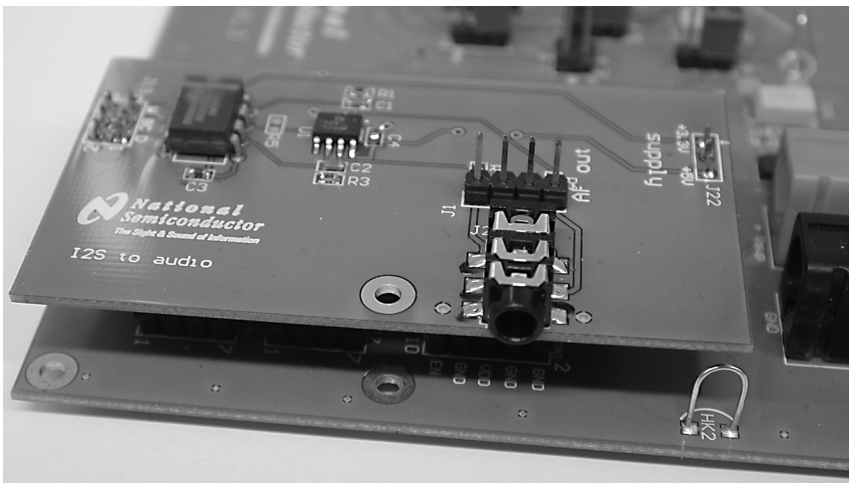

Figure 11. D/A Converter Daughter Board

The daughter board consist of a 1543 I^2S stereo D/A converter and a high performance audio operational amplifier (LM4562) that are supplied from the main LMV1022 / LMV1023 demo board PCB via the J22 (only for demo boards V1.3 or higher) . This board can be plugged on the headers J19 and J22 (see Figure 12 for the location of these headers). The output signal of the D/A converter board at J1 and J2 is DC coupled with a DC level of about 3V. For this reason, it is NOT advised to plug in a headphone directly in the 3.5mm jack connector. J2 is intended to be used to drive a small stereo amplifier.

The schematic for this A/D daughter board can be found in Figure 22

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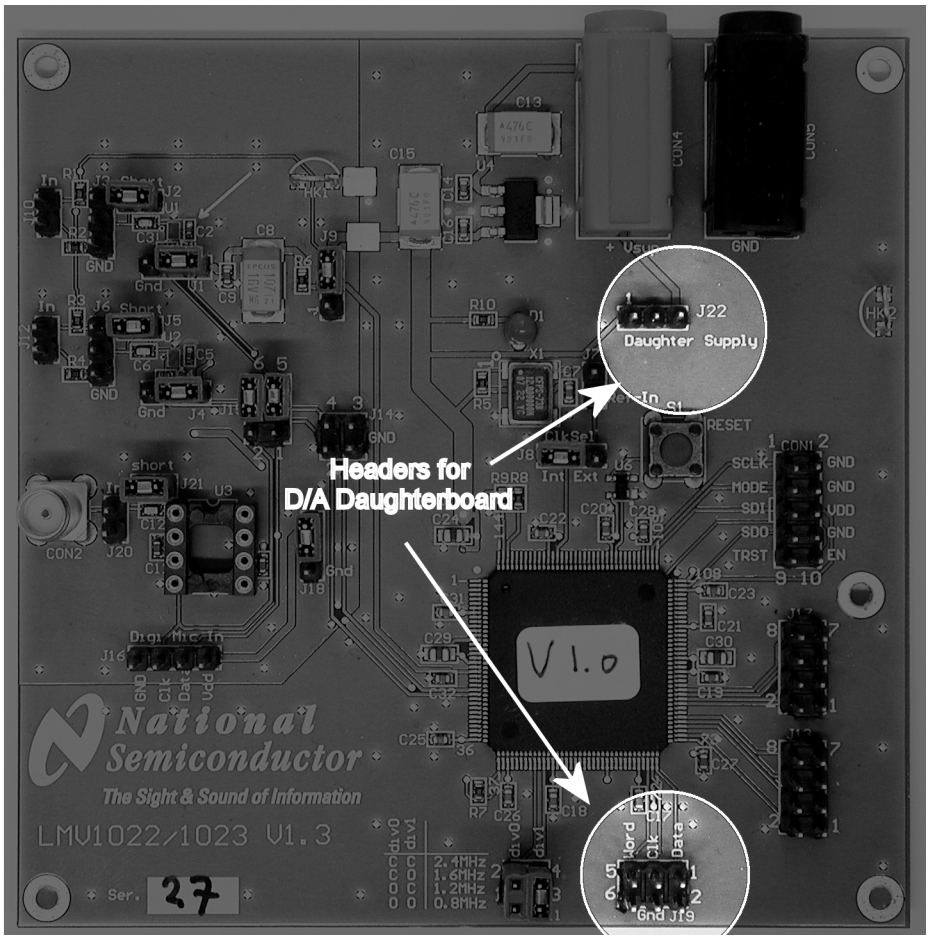

Figure 12. Connections for D/A Daughter Board

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16 Board Layer Views LMV1022 / LMV1023 Demo Board

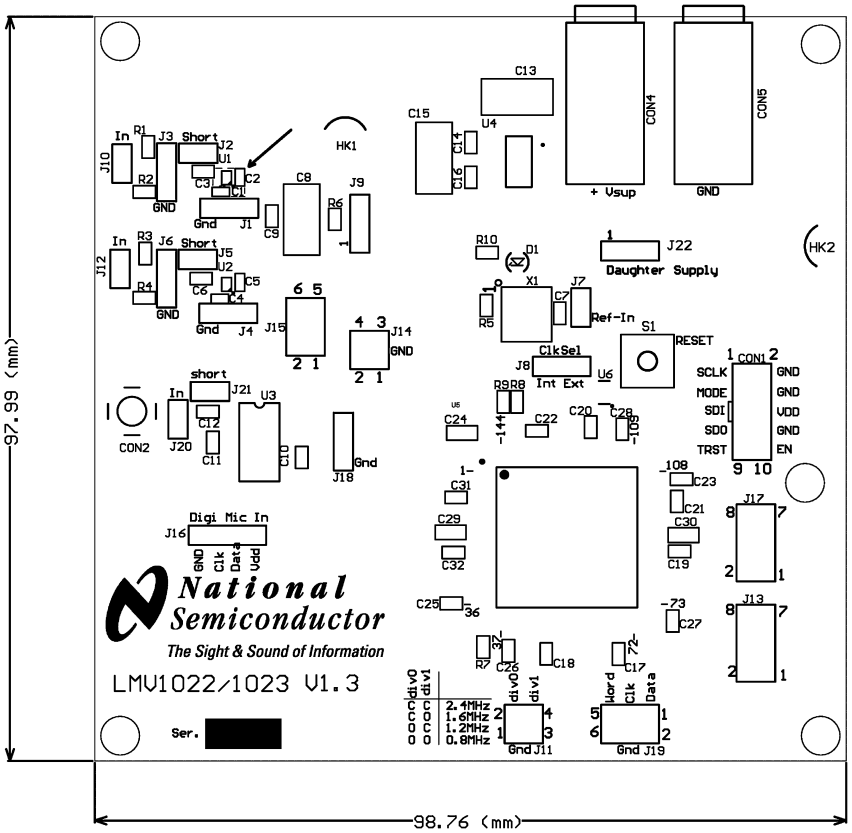

Figure 13. Silk-screen LMV1022 / LMV1023 Demo Board

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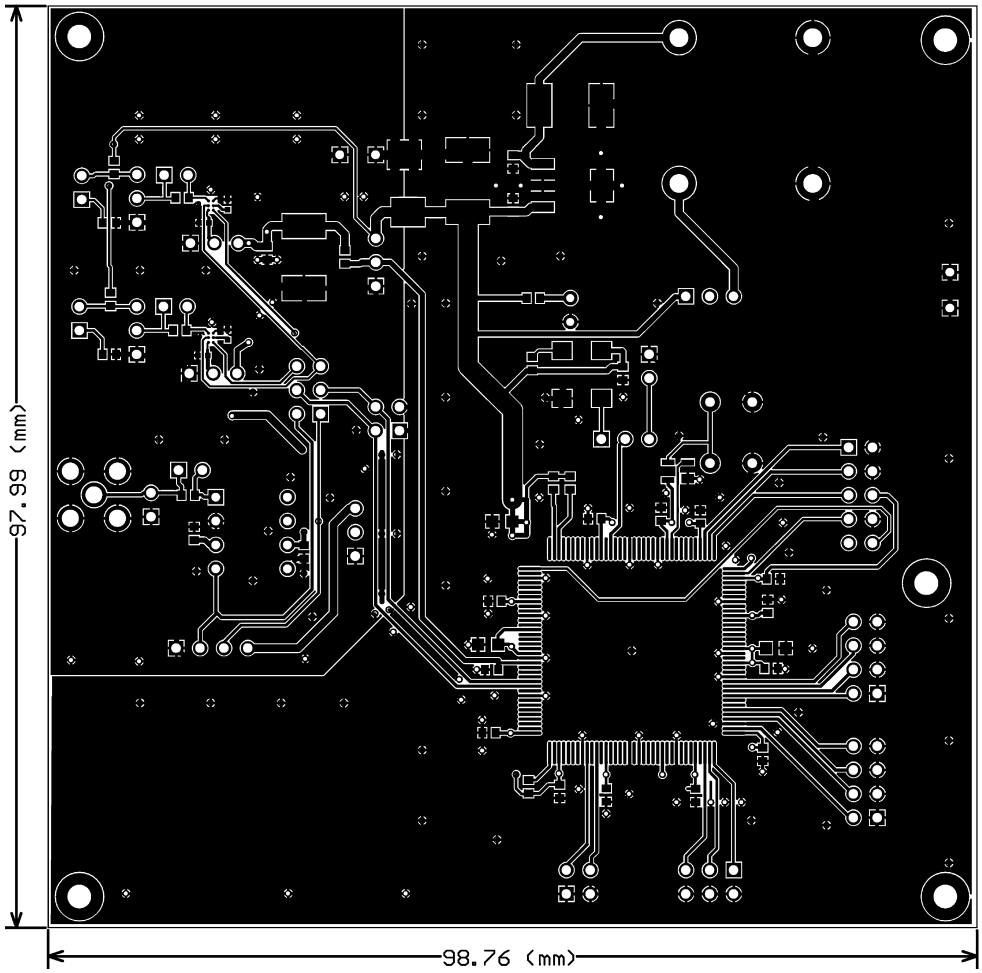

Figure 14. Top Layer LMV1022 / LMV1023 Demo Board

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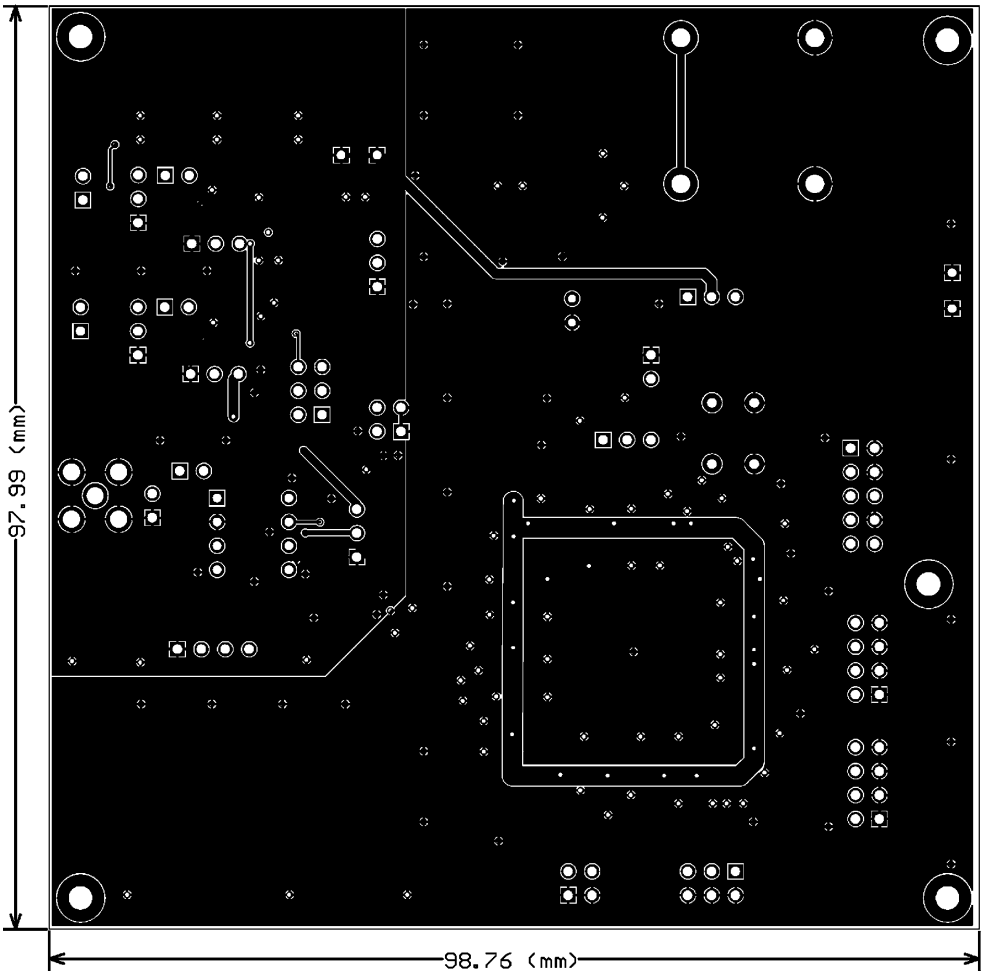

Figure 15. Bottom Layer LMV1022 / LMV1023 Demo Board

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17 Board Layer Views D/A Daughter Board

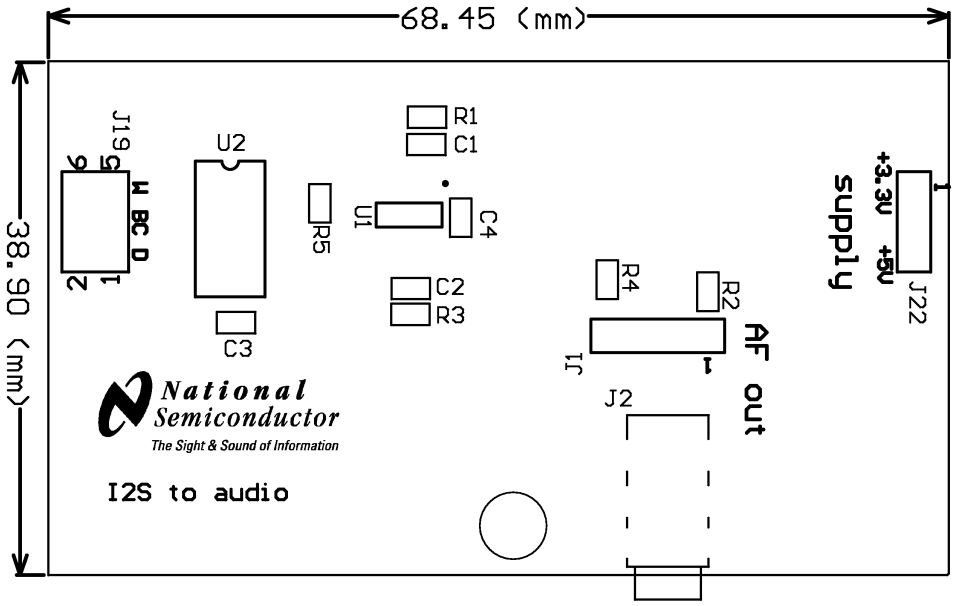

Figure 16. Silk-screen D/A Daughter Board

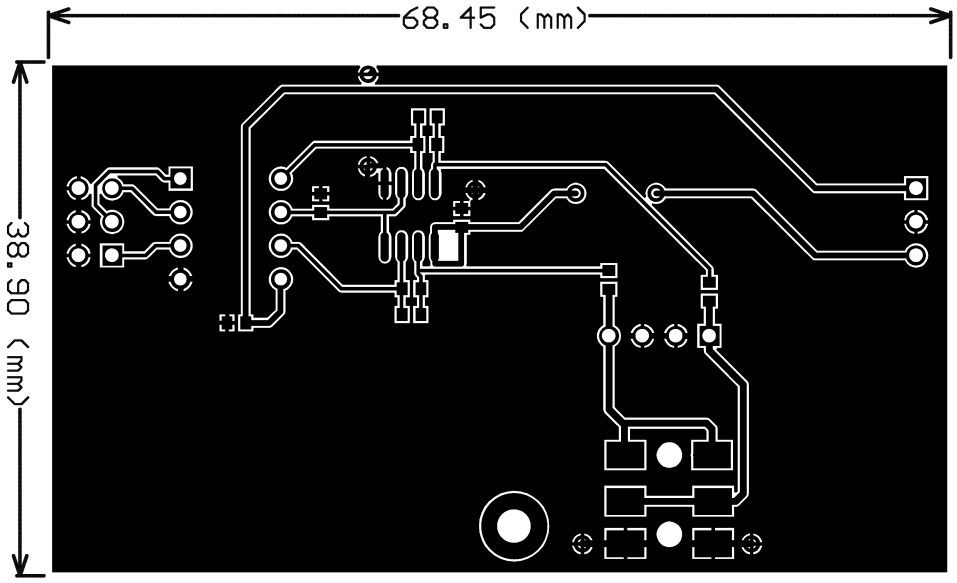

Figure 17. Top Layer D/A Daughter Board

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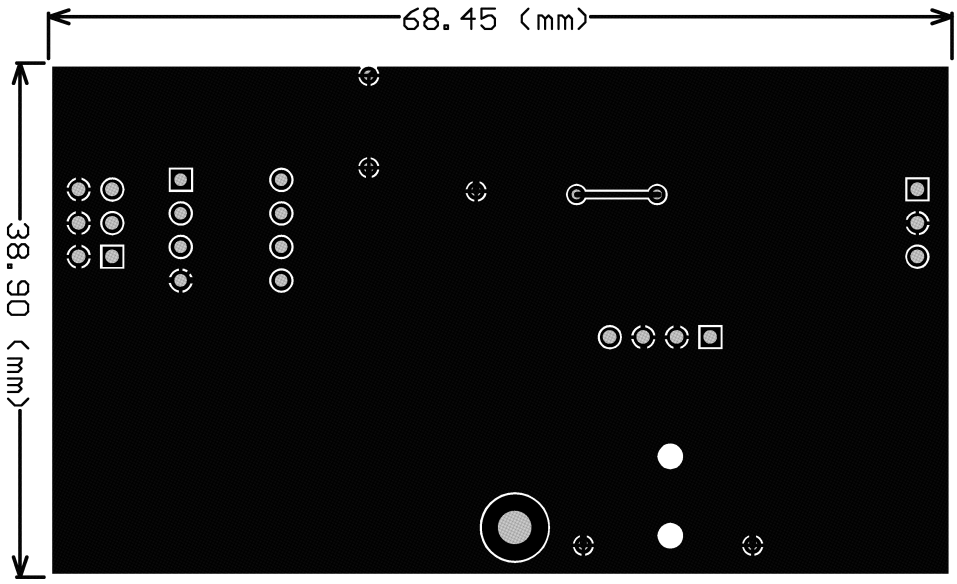

Figure 18. Bottom Layer D/A Daughter Board

18 Schematic Diagrams LMV1022 / LMV1023 Demo Board

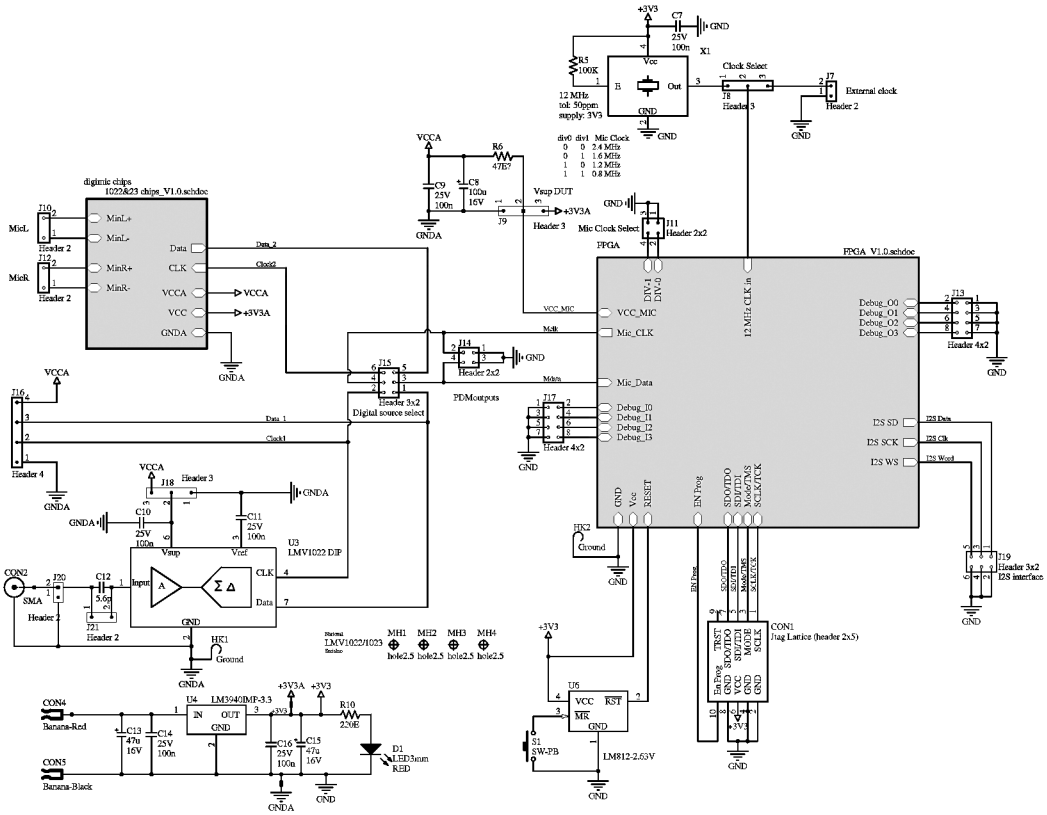

Figure 19. Top Level LMV1022 / LMV1023 Demo Board

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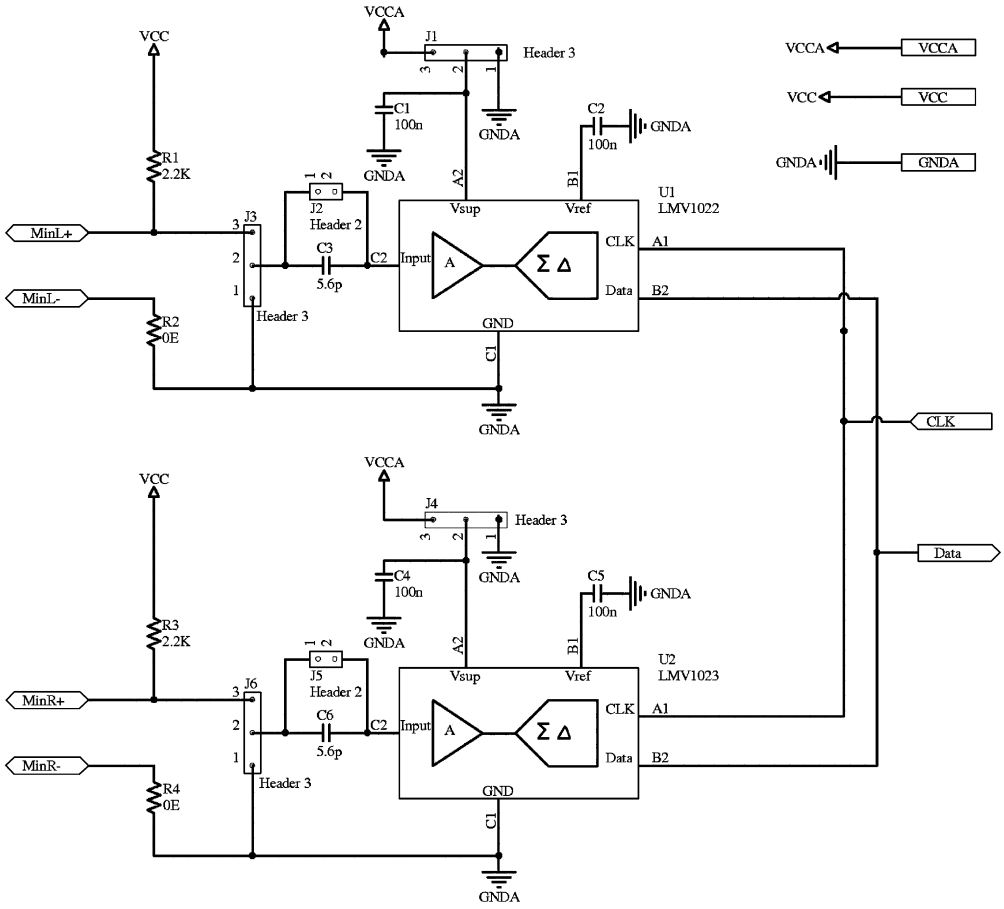

Figure 20. On-board Parts LMV1022 / LMV1023 Demo Board

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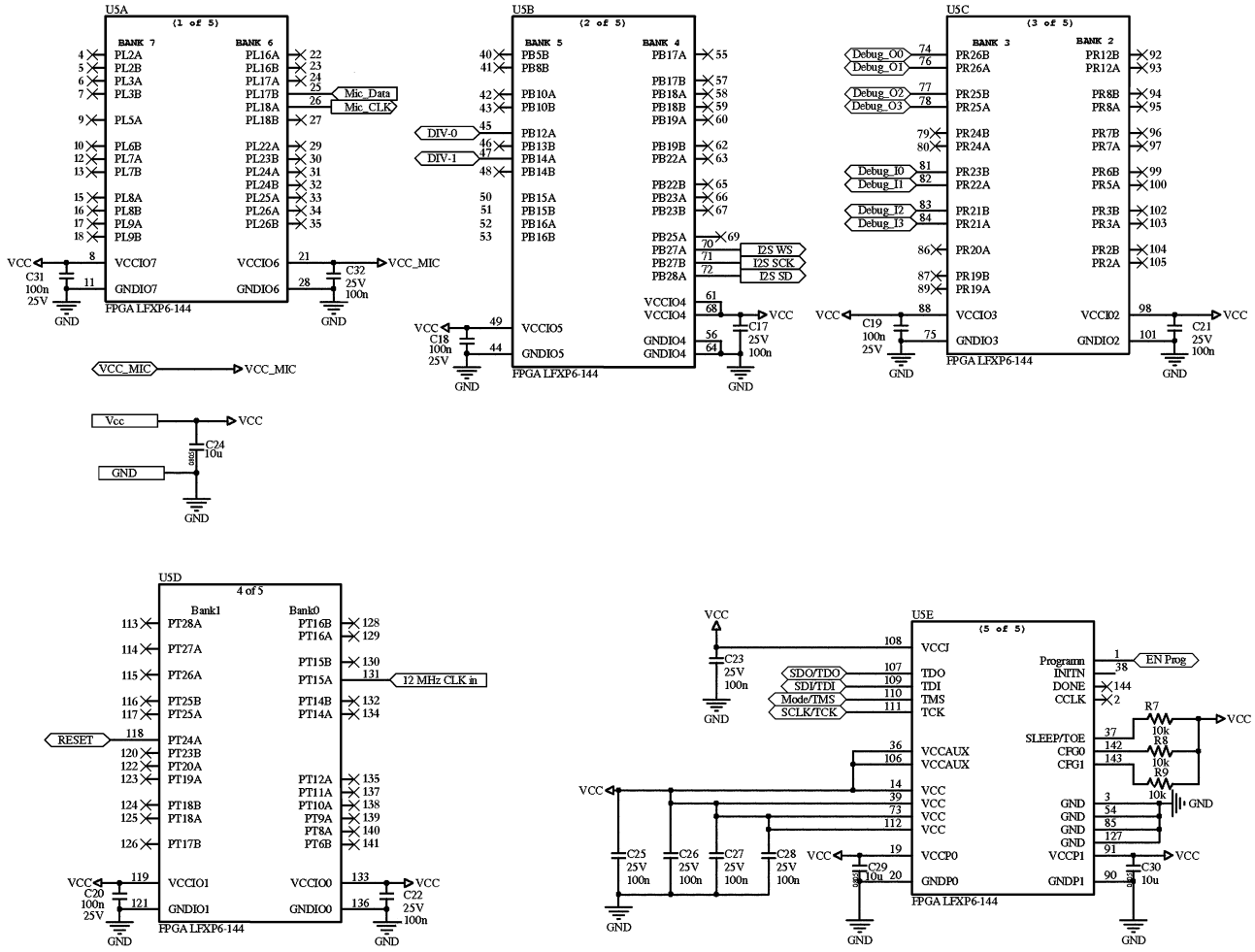

Figure 21. FPGA LMV1022 / LMV1023 Demo Board

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19 Schematic Diagram A/D Daughter Board

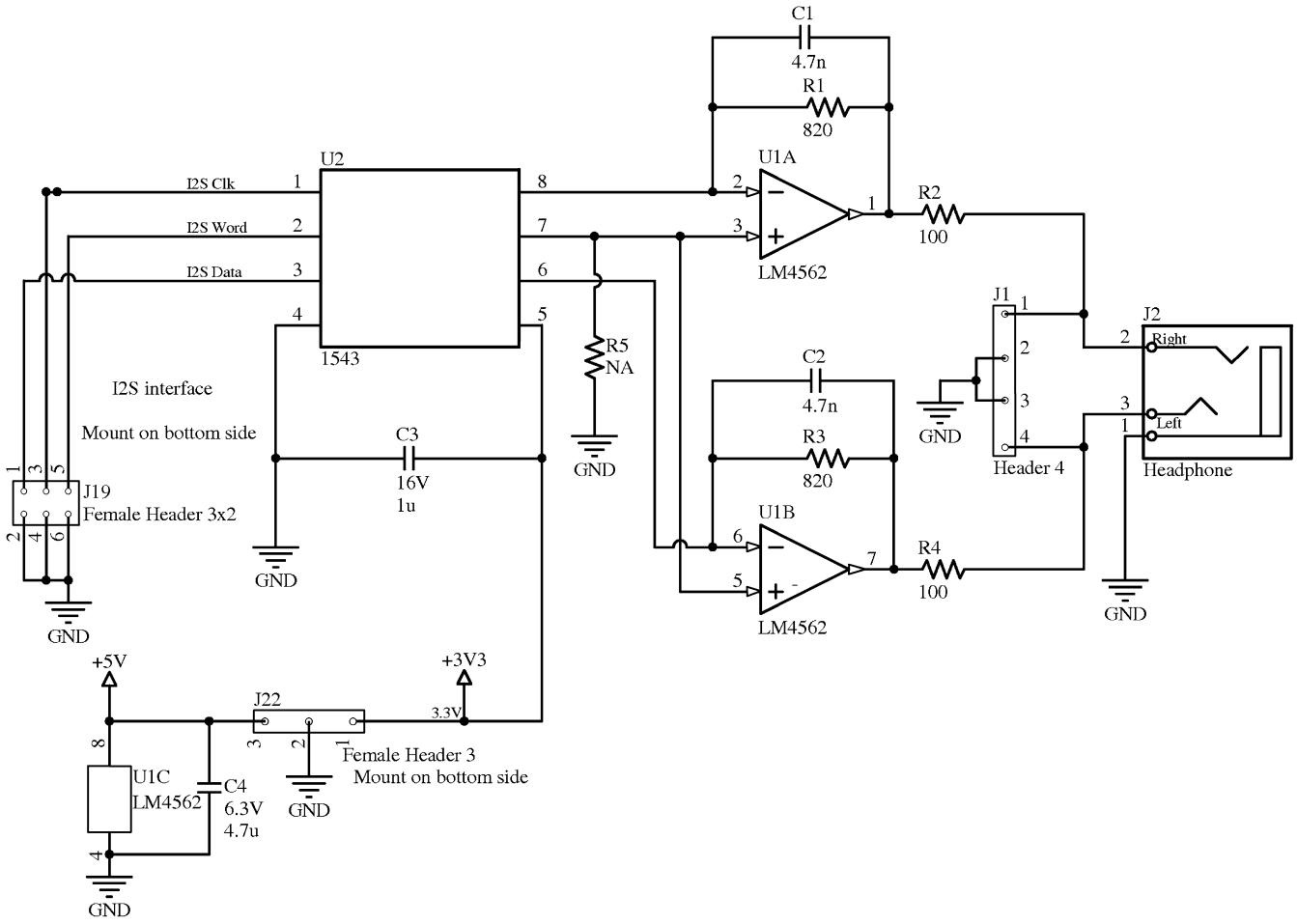

Figure 22. A/D Daughter Board

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20 BOM LMV1022 / LMV1023 Demo Board

RefDes	Part Description	Value	Tolerance	Rating	Package Type
C1, C2, C4, C5	Multilayer Ceramic Capacitor	100nF	20%	10V	0402
C3, C6, C12	Ceramic Capacitor	5.6pF	10%	16V	0603
C7, C9, C10, C11, C14, C16, C17, C18, C19, C20, C21, C22, C23, C25, C26, C27, C28, C31, C32	Multilayer Ceramic Capacitor	100nF	20%	25V	0603
C8	Tantalum Capacitor	100µF		16V	Case D
C13, C15	Tantalum Capacitor	47µF		16V	Case D
C24, C29, C30	Multilayer Ceramic Capacitor	10µF		16V	0805
CON1	Jtag Lattice (header 2x5)				Header 2x5
CON2	SMA				SMA
CON4	Banana-Red				
CON5	Banana-Black				
D1	LED3mm				
HK1, HK2	Ground connection (jumper 5mm high)				
J1, J3, J4, J6, J8, J9, J18	Header 3				HDR1X3
J2, J5, J7, J10, J12, J20, J21	Header 2				HDR1X2
J11, J14	Header 2x2				HDR2X4
J13, J17	Header 4x2				HDR2X3
J15, J19	Header 3x2				Header 3x2
J16	Header 4				HDR1X4
J22	Daughter Supply				HDR1X3
R1, R3	Resistor SMD	2.2KΩ	5%		0603
R2, R4	Resistor SMD	0Ω			0603
R5	Resistor SMD	100KΩ	5%		0603
R6	Resistor SMD	47Ω	5%		0603
R6	Resistor SMD	10kΩ	5%		0603
R10	Resistor SMD	220Ω	5%		0603
S1	Push button switch				SW-PB
U1	LMV1022				DSBGA-6x0.5pitch
U2	LMV1023				DSBGA-6x0.5pitch
U3	DIP part socket				DIP-8
U4	LM3940IMP-3.3				SOT232
U5	FPGA LFXP6-144				SQFP50P2250 X 2250 X 165-144M
U6	LM812-2.63V				SOT143
X1	Xtal Osc 12 MHz				CMAC CFPS

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21 BOM A/D Daughter Board

RefDes	Part Description	Value	Tolerance	Rating	Package Type
C1, C2	Multilayer Ceramic Capacitor	4.7nF	±10%	16V	0603
C3	Multilayer Ceramic Capacitor	1µF	±20%	16V	0603
C4	Multilayer Ceramic Capacitor	4.7µF	±20%	6.3V	0603
J1	Header 4x1				HDR1X4
J2	3,5 mm stereo output				3.5mm stereo
J19	Female Header 3x2				HDR2X3
J22	Female Header 3x1				HDR1X3
R1, R3	Resistor	820Ω	±5%		0603
R2, R4	Resistor	100Ω	±5%		0603
R5	Resistor	N.A.			0603
U1	High Performance Opapm	LM4562			SOIC_1.27 pitch
U2	I2S DAC	TDA1543			DIP-8

22 Revision History

Rev	Date	Description
1.0	03/06/08	Initial release.

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