ISSUE 3, 2024

Texas Instruments

Analog Design JOURNAL

Exploring fast frequency hopping in RF sampling data converters in test and measurement applications

An overview on basic operational amplifier stability

Powering an offboard capacitive load in automotive zone-based power distribution systems

The art of passive matching a high-speed ADC analog-input front end

Table of contents

ISSUE 3, 2024

Exploring fast frequency hopping in RF sampling data converters in test and measurement applications

Chase Wood
Application Engineer
High-Speed Data Converters

Introduction

As data converters continue evolving, it's a challenge to meet multiband requirements in systems such as software-defined radios, wireless testers and spectrum analyzers. System designers are reevaluating traditional frequency-hopping methods as devices become more complex and capable of faster transitions between numerically controlled oscillator (NCO) frequencies.

In this article, I'll explore the evolution of frequency-hopping techniques, comparing traditional and advanced methods such as general-purpose input/output (GPIO) and fast reconfiguration interface (FRI). Understanding these advancements can help you gain valuable insights into optimizing frequency hopping for both single- and multiband applications. But to fully grasp how modern systems meet multiband requirements, it's essential to first understand the fundamentals of frequency hopping.

What is frequency hopping?

In modern communication systems, such as Wi-Fi® 6 and 7 or quadrature amplitude modulation (QAM)-encoded signals, the spectrum is inherently multiband, meaning that the radio-frequency (RF) domain consists of multiple channels within each frequency band. For instance, Wi-Fi 6 and 7 operate across several channels within the same frequency band to dynamically maximize bandwidth and data throughput, while QAM involves encoding data into different phase offsets and amplitude levels within a single channel. **Figure 1** shows an example frequency band containing 7 QAM channels.

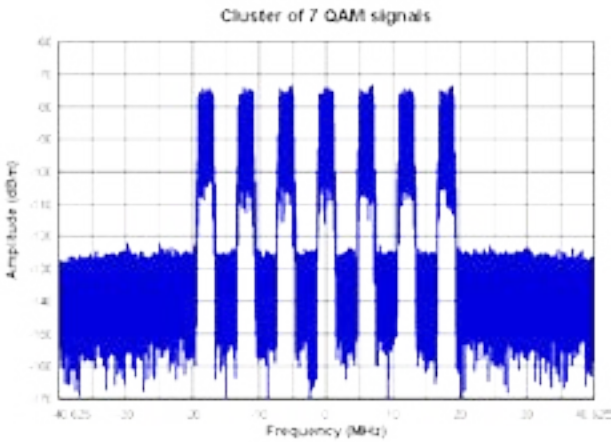

Figure 1. *Multitone signals in the frequency domain.*

Direct RF-sampling analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) incorporate many digital features. One of the most important features enabling direct RF sampling is the digital downconverter (DDC) in ADCs and the digital upconverter (DUC) in DACs.

In an ADC, the DDC consists of three main components: an NCO, digital mixer and decimator block. The NCO serves as the digital counterpart of the local oscillator in traditional receiver signal chains and mixes with the input signal to provide a signal in baseband (Nyquist zone 1), along with unwanted images. The decimator block filters out the images through a finite impulse response (FIR) decimation filter and then reduces the signal bandwidth by downsampling. The decimator block is the digital equivalent of an intermediate frequency (IF) filter.

In a DAC, the DUC comprises an interpolator, an NCO and a digital mixer. The interpolator, unlike in an ADC,

upsamples the lower-bandwidth input signal and then passes it through a FIR filter to suppress images. After the interpolator stage, the output signal feeds into a digital mixer to mix with the NCO, allowing the DAC to operate over a wide Nyquist zone with a lower input signal bandwidth.

The number of DDCs active on any given input of an RF sampling converter determines whether a converter operates in single- or multiband output. This article's focus will be on the ADC aspect of frequency hopping.

Figure 2 shows an example of the DDC from the Texas Instruments (TI) **ADC32RF55**, an RF-sampling ADC capable of dual-channel, quad-band operation at 3GSPS.

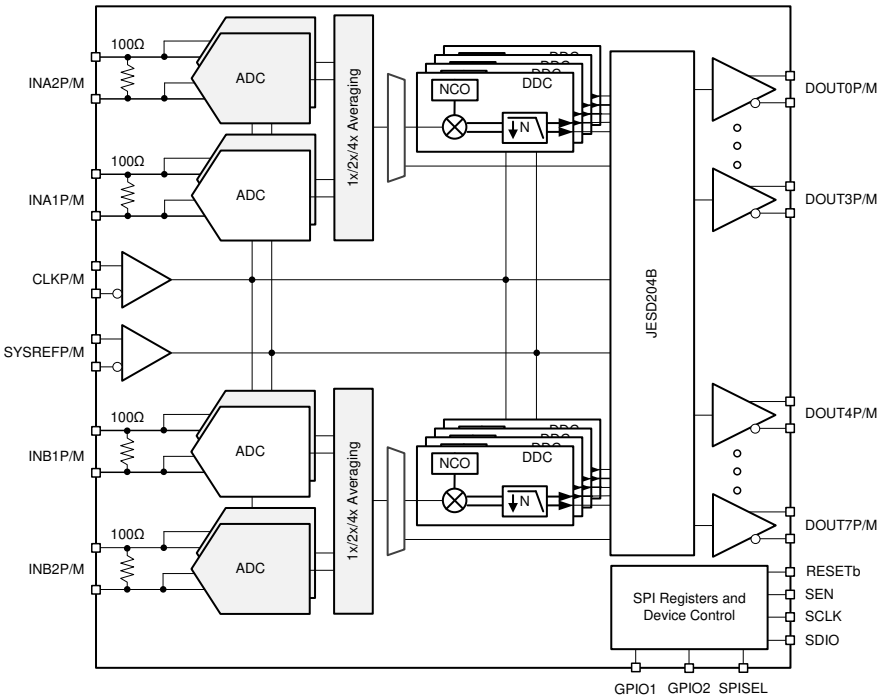

Figure 2. *Functional block diagram of the ADC32RF55 (four DDCs per channel).*

Often, the frequency band of interest may change: Instead of switching an entirely unique signal chain for each band, the same RF sampling converter can simply adjust the NCO frequency to match the new frequency band. This is a major advantage of modern RF-sampling converters. The act of changing the NCO from one frequency to a different frequency is what is known as frequency hopping.

The NCO does not produce an analog frequency directly; instead, it generates a digital representation of the desired frequency with high resolution. Each NCO receives a digital word – typically 48 bit or higher – which when combined with an NCO phase accumulator can represent a signal suitable for the digital mixing stage. When programming an NCO, the digital representation corresponding to the desired IF is what gets programmed, not an actual frequency. The NCO frequency range is most commonly supported between –Fs/2 and Fs/2, where Fs represents the converter's sampling frequency. Negative frequency words are used for even Nyquist zones, while positive frequency words are used for signals in odd Nyquist zones.

To determine where a higher-order NCO frequency falls into baseband, your first task is to perform a modulus

operation between the intended frequency and the sample rate to remove any multiple of Fs. The intended NCO frequency is now between 0Hz and the converter sample rate, Fs.

If the NCO frequency is less than the Nyquist frequency (Fs/2), then the intended NCO frequency translates to an odd Nyquist zone, as shown in **Equation 1**:

$$\mathrm{NCO_{word}} = \mathrm{f_{NCO}} \times \frac{2^{48}}{\mathrm{F_S}}, \text{ for } 0 \text{ to } \mathrm{F_S}/2 \qquad (1)$$

If the calculated NCO frequency is above the Nyquist frequency, then the frequency lands in an even Nyquist zone, as shown in **Equation 2**:

$$\mathrm{NCO_{word}} = (\mathrm{f_{NCO}} + F_S) \times \frac{2^{48}}{\mathrm{F_S}}, \text{ for } -\mathrm{F_S}/2 \text{ to } 0 \qquad (2)$$

Figure 3 shows how a fundamental signal (Fund.) and its second-, third- and fourth-order harmonics (HD2, HD3 and HD4) will fold back into the first Nyquist zone, despite the actual frequency component landing in higher-order Nyquist zones.

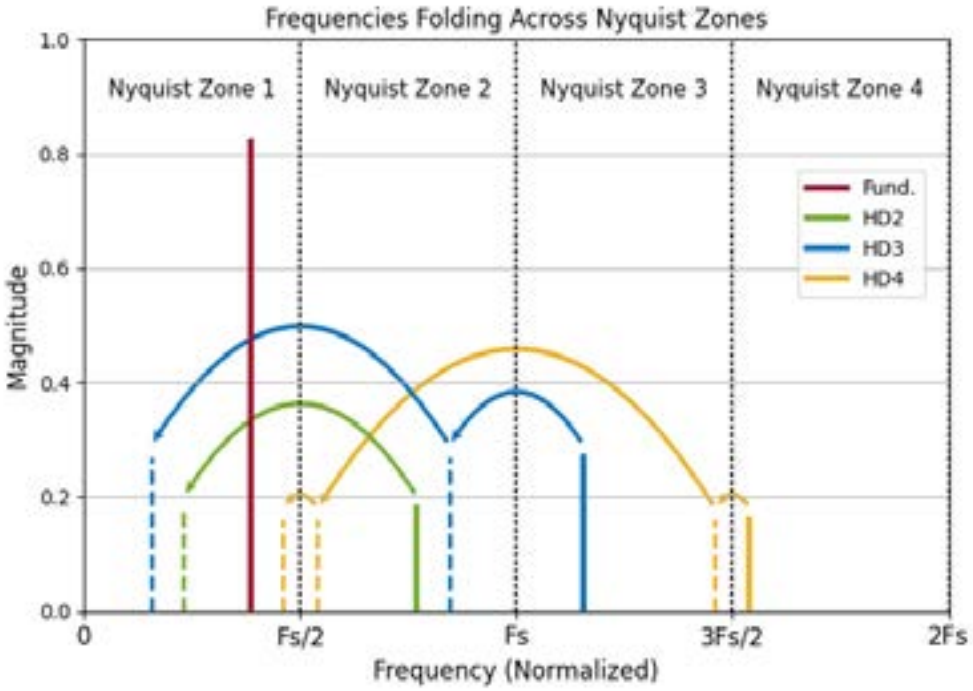

Figure 3. *Harmonics folding across high-order Nyquist zones into Nyquist zone 1.*

One advantage of RF-sampling ADCs over traditional ADCs is that the hardware does not need to change in order to switch frequency bands. This inherent flexibility allows RF-sampling ADCs to quickly adapt to new frequency bands without requiring additional hardware components, simplifying system design and reducing costs. This process is not instantaneous, however. In early designs of RF-sampling ADCs, only a single NCO word option was available for each NCO and subsequent DDC. As a result, hopping to another frequency required multiple register-write operations.

The new NCO word must be written through the Serial Peripheral Interface (SPI), followed by another register write to push the new NCO word into the DDC block,

where it actually takes effect. Several factors influence the time required to hop frequencies, including the length of the NCO word and the SPI transaction speed. Often, the register size of ADCs is limited to 8 bits, so you will need a total of seven register writes to update a 48-bit NCO: six register writes for the NCO word itself and one additional register write to update the DDC.

After considering the overhead for each SPI transaction (typically a 16-bit address for each register write), the transaction time triples. Assuming a 20MHz serial clock signal (SCLK) rate, **Equation 3** calculates the time to frequency hop, assuming a nonstop stream of SPI data:

$$t_{hop} = \frac{1}{20 \times 10^6\,(\text{Hz})} \times 7\,(\text{transactions}) \times \frac{24\,(\text{bits})}{(\text{transaction})} \quad (3)$$
$$= 8.4\mu s$$

Evolution of frequency-hopping techniques

RF converters are now designed with multiple NCO words per DDC, allowing preprogramming of NCO words. This innovative approach enables faster frequency hopping by preloading several frequency values into the converter's memory. This concept of storing precalculated NCO words is where the "fast" in fast frequency hopping comes from.

Figure 4 shows the 48-bit NCO register addresses by NCO index and word index for the **ADC32RF55**. Despite the addresses being the same for channel A and B, the frequency words are unique, as this device implements register map paging, which masks registers not included on the active page from any read and write operations.

Channel A		Channel B	
NCO1	NCO3	NCO1	NCO3
1: 0x100..0x105 2: 0x108..0x10D 3: 0x110..0x115 4: 0x118..0x11D	1: 0x140..0x145 2: 0x148..0x14D 3: 0x150..0x155 4: 0x158..0x15D	1: 0x100..0x105 2: 0x108..0x10D 3: 0x110..0x115 4: 0x118..0x11D	1: 0x140..0x145 2: 0x148..0x14D 3: 0x150..0x155 4: 0x158..0x15D
NCO2	NCO4	NCO2	NCO4
1: 0x120..0x125 2: 0x128..0x12D 3: 0x130..0x135 4: 0x138..0x13D	1: 0x160..0x165 2: 0x168..0x16D 3: 0x170..0x175 4: 0x178..0x17D	1: 0x120..0x125 2: 0x128..0x12D 3: 0x130..0x135 4: 0x138..0x13D	1: 0x160..0x165 2: 0x168..0x16D 3: 0x170..0x175 4: 0x178..0x17D

Figure 4. *NCO word addresses by channel and NCO index of the ADC32RF55.*

Now that the words are programmed, how do you actually select a specific one? Changing the NCO word simply requires selecting a new NCO word for the DDC, which you can do through SPI or GPIO pins. **Table 1** shows an example of how to select an individual word for the specified DDC in the **ADC32RF55**, depending on the number of active bands. In a standard configuration, this ADC has four unique NCO words per DDC; however, in single-band modes, the neighboring DDC's four NCO words can supply the active NCO as well, meaning that each channel's DDC has access to eight preprogrammed NCO words.

# of bands	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
Single	0x3B	0	0	0	0	NCO2 CHA[1:0]	0	NCO1 CHA[1:0]	
	0x41	0	0	0	0	NCO2 CHB[1:0]	0	NCO1 CHB[1:0]	
Dual	0x3B	0	0	0	0	NCO2 CHA[1:0]		NCO1 CHA[1:0]	
	0x41	0	0	0	0	NCO2 CHB[1:0]		NCO1 CHB[1:0]	
Quad	0x3B	NCO4 CHA[1:0]		NCO3 CHA[1:0]		NCO2 CHA[1:0]		NCO1 CHA[1:0]	
	0x41	NCO4 CHB[1:0]		NCO3 CHB[1:0]		NCO2 CHB[1:0]		NCO1 CHB[1:0]	

Table 1. *NCO word selection on the ADC32RF55 by NCO index.*

The time required to perform a frequency hop varies by converter. Typically, the SPI method requires the duration of just a single SPI transaction, instead of seven as in **Equation 3**. The speed of the SPI method is further limited by the maximum clock rate of the SPI and the overhead involved with serial data transmission. Assuming the same 20MHz SCLK, **Equation 4** shows the time required before the device initiates an NCO word change:

$$t_{hop} = \frac{1}{20 \times 10^6 \left(\text{Hz}\right)} \times 1\ (\text{transaction}) \times \frac{24\ (\text{bits})}{(\text{transaction})} \quad (4)$$
$$= 1.2\mu s$$

In contrast, the GPIO method can be as fast as the GPIO inputs can be updated. Once the voltage crosses its high- or low-level thresholds, the NCO word change begins.

In either method, once the device receives the NCO word change, the internal NCO word updates instantly; however, the decimation filter has to flush out all old values, so there is some added delay as a result based on the decimation factor.

Table 2 shows the time required by the **ADC32RF55** to flush its decimation filter with data from mixing with the new NCO frequency.

Decimation setting	NCO switching time
/4	~250ns
/8	~350ns
/16	~600ns
/32	~1µs
/64	~2µs
/128	~4µs

Table 2. *Decimation filter flush times on the ADC32RF55.*

Generally, the GPIO approach will be faster than an SPI approach for frequency hopping because of the inherent parallel aspect of a GPIO interface vs. a serial interface. However, there is one consideration: In GPIO word-selection mode, the same word index will apply to all active DDCs. The device cannot use word 1 on DDC1 while using word 3 on DDC2; the GPIO interface will set all DDCs to the same word index.

Another method, FRI, involves sending data over specific device pins at a much faster rate than what standard SPI supports. Some devices, such as the TI **DAC39RF12**, can support FRI communication up to 200MHz, which you can use for selecting the active NCO word.

Applications in test and measurement

Supporting multiple frequency bands is essential for test and measurement equipment given the diverse and evolving needs of various applications. Wideband test equipment's ability to operate across multiple frequency ranges makes it a versatile tool for comprehensive testing across different systems and technologies. As technology advances and new frequency bands are introduced, the need for equipment that can quickly adapt and switch between multiple bands becomes increasingly important.

In spectrum analyzers, fast-frequency-hopping techniques enable fast and accurate measurements by reducing sweep times and improving the ability to detect transient signals. The rapid switching capabilities of advanced ADCs with multiple NCOs or fast reconfiguration methods such as FRI enable more efficient analysis across broad frequency ranges, enhancing the overall performance and utility of spectrum analyzers in both research and field applications.

For wireless testers, fast-frequency-hopping techniques play a crucial role in characterizing and troubleshooting communication systems. By enabling rapid transitions between frequencies, these techniques improve signal fidelity and reduce testing cycles. This capability is particularly valuable in assessing the performance of wireless devices under multiple frequency conditions.

Beyond spectrum analyzers and wireless testers, fast-frequency-hopping techniques offer significant benefits in many other test and measurement applications. General-purpose signal analyzers and RF signal generators, for example, can leverage these techniques to provide more flexible and accurate testing across multiple frequency bands. Multiband receivers also benefit from the ability to quickly switch between bands, ensuring reliable performance in dynamic testing environments.

Conclusion

By enabling rapid and precise transitions between frequencies, fast-frequency-hopping techniques provide increased flexibility, improved accuracy, and better adaptability to evolving technological needs. As the demands on test and measurement equipment continue to grow, understanding and implementing fast-frequency-hopping methods will be crucial for maintaining cutting-edge performance and ensuring comprehensive testing capabilities.

Related Websites

1. Wood, Chase. 2024. "**ADC Decimation: Addressing High Data-Throughput Challenges**". Embedded Computing Design, February 5, 2024.
2. Wood, Chase. 2024. "**ADC Decimation: Unlocking RF Potential with Downconverters**". Embedded Computing Design, February 29, 2024.
3. Wood, Chase. 2024. "**ADC Decimation: Analyzing High-Bandwidth Spectrum Clusters**". Embedded Computing Design, May 9, 2024.
4. **TI ADC32RF55 data sheet**
5. **TI DAC39RF12 data sheet**

An overview on basic operational amplifier stability

Jerry Madalvanos
Applications Engineer
Precision Signal Conditioning

One of the most common issues with operational amplifier (op amp) circuits is stability. In this article, I'll answer three important questions with regards to stability:

- How much phase margin do you need for a reliable design?
- How do you compensate an unstable circuit?
- What drop-in solutions are available for stability issues?

How much phase margin do you need?

Op-amp loop stability is measured in phase margin, which is the difference in the output signal phase shift from 360 degrees when the output closed-loop gain goes below unity. Some shift is inherent to every op amp (for example, the dominant pole), while additional shift depends on the application and components surrounding the amplifier.

Different rules of thumb recommend 30, 45 or even 60 degrees of phase margin, but how much do you really need to ensure reliable performance? For traditional Miller-compensated op amps, it is possible to simulate typical process variations and observe the resulting impact on phase margin.

Figure 1 approximates the open-loop gain (Aol) and output impedance (Zo) of an op amp with a 1MHz unity-gain bandwidth and Zo = 300Ω. Over process variation, the value of the Miller capacitor (C26) can vary approximately ±30%, and an additional ±30% (approximate) over temperature. This variation gives a total error of ±30% × ±30%, which is the same as ±30% + ±9%, or ±39% variation. Since the value of the Miller capacitor changes the placement of the dominant pole in the Aol of the op amp, this variation can significantly impact the unity-gain bandwidth and phase margin, which is why these specifications are always given as typical values, even for precision amplifiers and high-speed amplifiers.

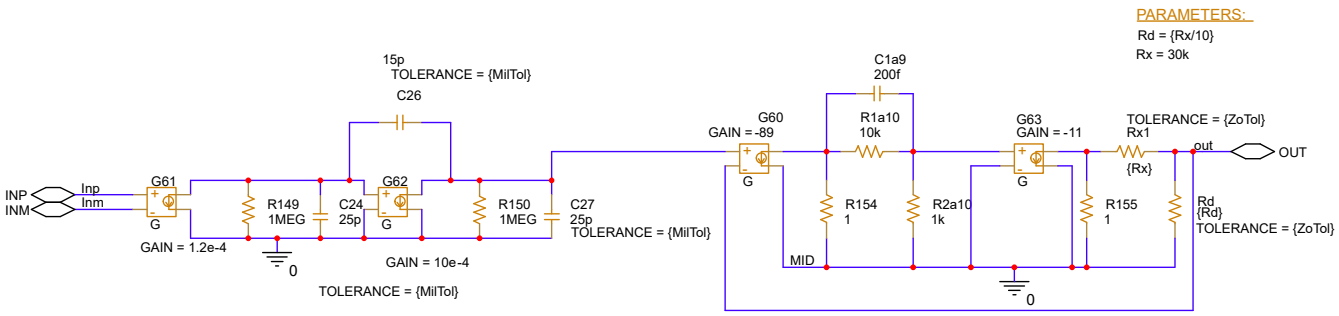

Figure 1. *Open-loop gain and output impedance PSpice® for TI circuit*

The amplifier in **Figure 1** is set with a load resistance and capacitance so that the feedback loop has 45 degrees of phase margin. Running a Monte Carlo analysis on the dominant factors of the loop stability – the Miller capacitor, open-loop output impedance and passive devices surrounding the amplifier – will show an estimate of how changes over process variation and temperature will impact the phase margin of the circuit.

Figure 2 plots the resulting phase margin. For this analysis, I applied ±40% variation to the Miller capacitor, ±15% variation for Zo, ±10% for the load capacitor and ±5% for the load resistor. These are the expected internal tolerances for the Miller capacitor and Zo, as well as typical component precision for many general-purpose applications.

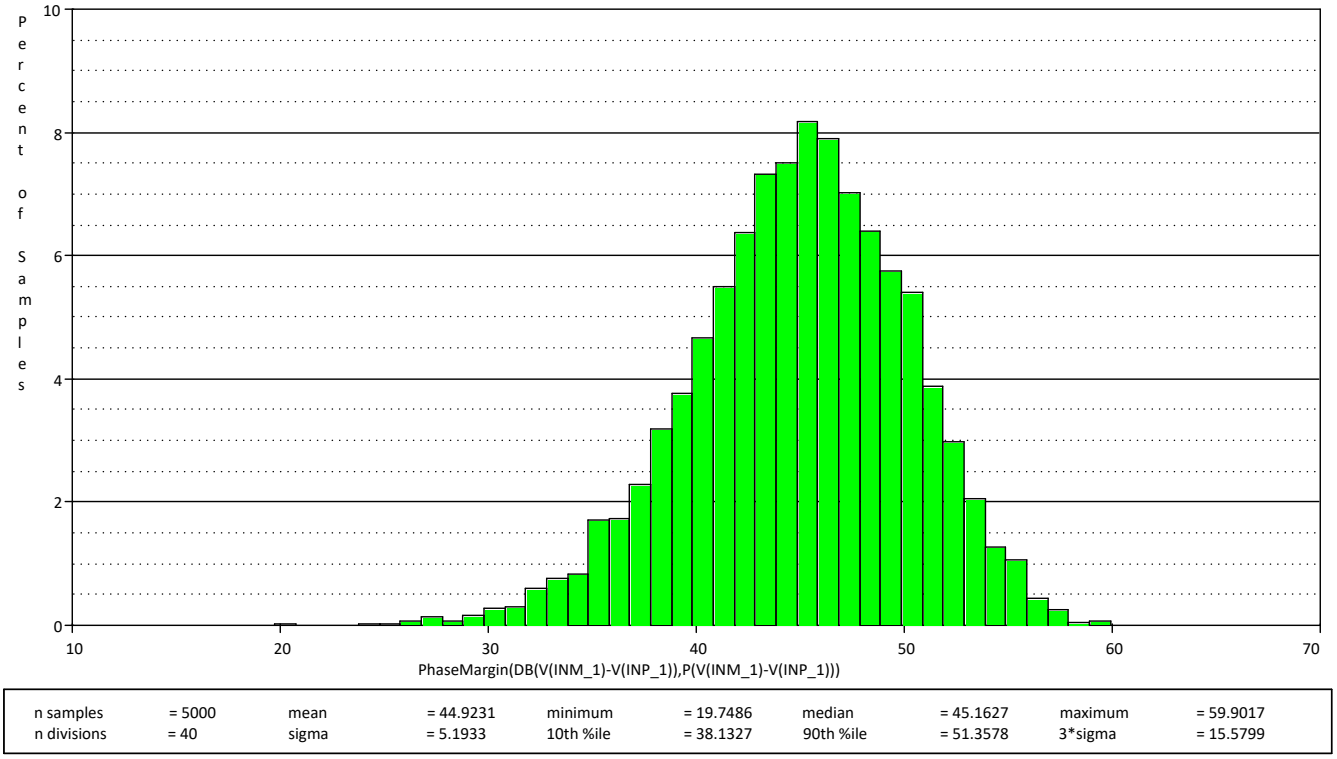

Figure 2. *5,000-run Monte-Carlo analysis across estimated process variation and temperature shifts*

Across this variation, the phase margin of the feedback loop sees a minimum phase margin of 19 degrees, a 26 degree shift from 45 degrees. Over process variation and temperature, the circuit would remain stable if it had approximately 27 degrees of phase margin, although 45 degrees will offer both good transient performance and settling time. The closer the phase margin gets to 0 degrees, the more the output will overshoot the final value, and the longer it will take to settle to the final output value. 45 degrees of phase margin provides enough design tolerance to allow a shift in phase margin without compromising settling time or seeing excessive overshoot.

While these simulations are helpful in understanding the effects of Miller capacitor variation on performance, it's the circuit designer who is ultimately responsible for the performance of their design. Simulations are only as accurate as the included nonidealites, assuming many ideal properties in order to make the calculation less intensive.

Compensation schemes

There are cases where it is not possible to reduce a capacitor on the output of an op amp, for either voltage rail regulation, filter capacitance for an analog-to-digital converter, or other circuit needs. In such cases, how do you achieve proper phase margin? There are multiple compensation schemes that can increase phase margin, but in this article, I'll focus on two, shown in **Figure 3** and **Figure 4**: an isolation resistor (Riso) and Riso dual feedback. When designing these circuits, it can be difficult to determine what value of Riso you need to stabilize the feedback loop.

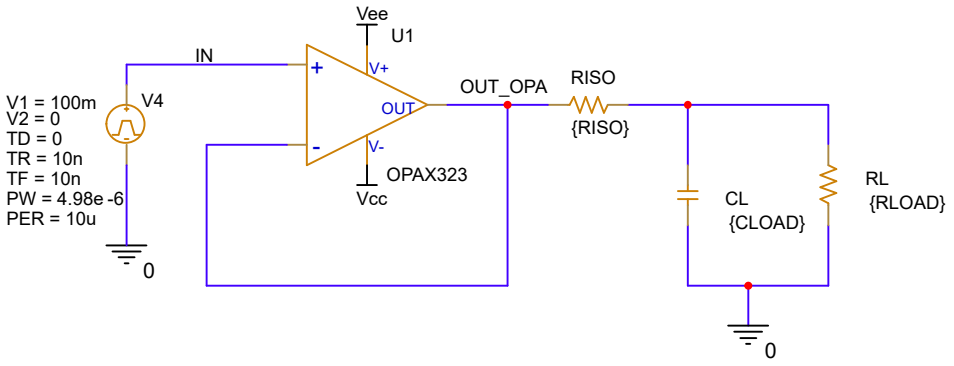

Figure 3. *Riso compensation scheme.*

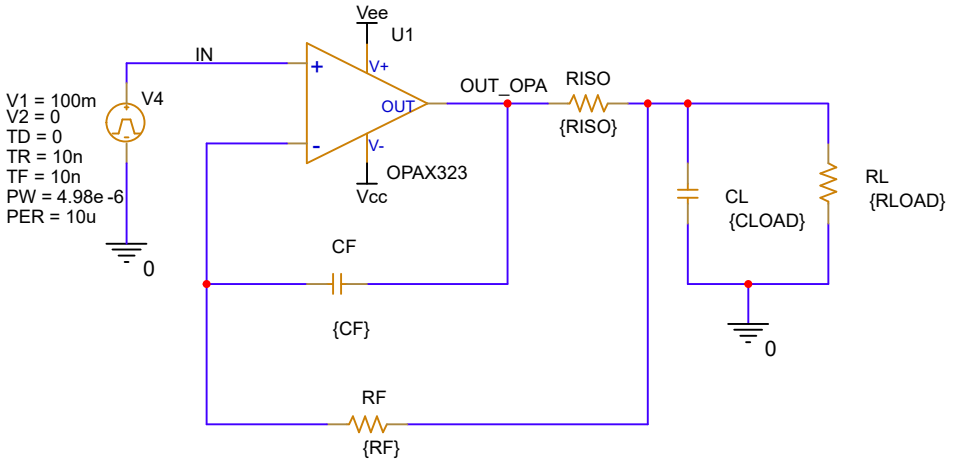

Figure 4. *Riso dual feedback scheme.*

Riso is the simplest method for isolating the phase lag introduced by the load capacitance. It involves placing a resistor between the feedback loop and the load capacitor. One drawback, however, is decreased DC accuracy when the output has a load current. The amount of DC error will be the value of the isolation resistor multiplied by the output current.

The Riso dual feedback compensation scheme overcomes this DC inaccuracy. The circuit enables a high-frequency path through the feedback capacitor to stabilize the feedback loop and a DC path that allows the op amp to compensate for the I × R drop over the isolation resistor. You can find these values either mathematically or through simulation by trying different values of Riso and seeing where there is stable operation.

Let's try an approach that uses mathematical analysis with simulated results.

The two main components for accurate modeling of amplifier loop stability are the open-loop gain and open-loop output impedance. TI's standard op-amp macromodel, the Green-Williams-Lis (GWL) model, accurately characterizes these parameters for all op amps released after 2016. Many of the more popular op amps, such as the **LM2904** and its newer version, the **LM2904B**, also have GWL macromodels created for them. The library file for the SPICE macromodels includes a header that details what parameters are accurately reflected in the SPICE model. If the open-loop gain and open-loop output impedance are modeled, it is likely that the stability of the model will reflect the silicon's performance.

Ensuring the accuracy of the SPICE model enables you to analyze the loop stability of your circuit and mathematically calculate the best value for Riso. The value of Riso that ensures 45 degrees of phase margin should create a zero in the feedback loop at the intersection point of the feedback factor (1/beta) and the amplifier open-loop gain. For extra assurance, setting the zero where the open-loop gain is 20dB, you can see the maximum positive phase shift from the zero in the feedback loop.

Compensation	Formula
Large capacitive load	
R_{ISO} (minimum)	$R_{iso} = \frac{1}{2\ \pi\ f_{AOL\ Loaded\ =\ 0dB}\ C_{LOAD}}$
R_{ISO}	$R_{iso} = \frac{1}{2\ \pi\ f_{AOL\ Loaded\ =\ 20dB}\ C_{LOAD}}$
R_{ISO} plus dual feedback	$R_F \geq R_{ISO}\ 100$ $\frac{5 \times R_{iso} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{iso} \times C_L}{R_F}$

Table 1. *Formulas for calculating isolation resistor value and feedback components for Riso dual feedback.*

Part of the power of PSpice for TI is you can set up, archive, and share simulations and equations for later schematics. Since the evaluation for Riso and Riso dual feedback are formulaic and easily repeatable, you can leverage these template projects to eliminate the need to remember the formulas to calculate Riso or the Rf/Cf for the Riso dual feedback circuit across four common op-amp circuits. Simply download the PSpice for TI project, drop in the op amp you want to analyze, enter the parameters that complete the specific circuit that needs stabilizing, and run the simulation to find the appropriate value of Riso that you need. These projects can also compensate circuits that are unstable from capacitance on the inverting terminal, or those with very large feedback resistors.

Circuit Type	PSpice for TI Project
Buffer Amplifier	**https://www.ti.com/lit/zip/sbomcj2**
Inverting Amplifier	**https://www.ti.com/lit/zip/sbomcj0**
Non-inverting Amplifier	**https://www.ti.com/lit/zip/sbomci9**
Difference Amplifier	**https://www.ti.com/lit/zip/sbomcj1**

The drop-in solution

There is also a solution when you don't want extra compensation circuitry, or it's not feasible to add it. TI's **OPA994** device family has a special compensation structure that is stable across capacitive loads, which is possible because the bandwidth of the device changes when the output sees different capacitive loads. Keeping the bandwidth constantly lower than the pole introduced by the output impedance and capacitive load will maintain the stability of the amplifier, regardless of what capacitor you place on the output. **Figure 5** illustrates the phase margin for different values of load capacitance with no external compensation resistor, taken from the **OPA994** data sheet.

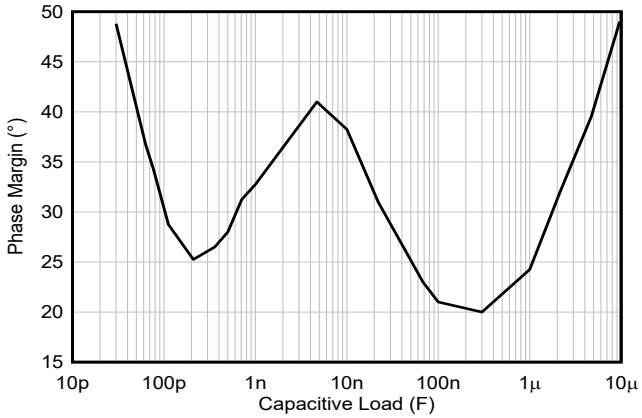

Figure 5. *Phase margin over various capacitive loads in unity gain.*

Every design decision comes with a cost in addition to a benefit, and the **OPA994** device family is no different. A more complex design results in a larger device, which can be more costly than simpler devices. Additionally, this means that the device cannot fit into TI's smallest packages, such as the 0.64mm^2 extra-small outline no-lead (X2SON) package. This design is currently only available in a bipolar amplifier, so if you require the low-input bias current of a complementary metal-oxide semiconductor (CMOS), this device may have too high of an input bias current.

There are many benefits associated with a bipolar amplifier, including lower noise and more bandwidth, for less quiescent current than CMOS devices. The full trade-off of bipolar vs. CMOS can be weighed on a circuit-by-circuit basis [**1**]. Overall, the **OPA994** can in many cases serve as a drop-in solution for stability.

Conclusion

In the initial design stage, the main question is how much phase margin is sufficient for reliable performance over process variation and temperature. If the phase margin of the initial implementation is not sufficient, multiple compensation schemes are available to increase the phase margin to an acceptable level. These solutions are given through pre-configured, easy-to-use projects in PSpice for TI. Finally, if there is a project already in production that does encounter a stability issue, use the drop-in solution proposed.

References

1. **Trade-Offs Between CMOS, JFET, and Bipolar Input Stage Technology** – Marek Lis

Powering an offboard capacitive load in automotive zone-based power distribution systems

Dilip Jain
Systems Manager
Power Switches

Rakesh Panguloori
Applications Manager
Power Switches

Introduction

The transition of vehicle architectures from domain- to zone-based is significantly changing automotive power distribution, with semiconductor switch-based solutions (see **Figure 1**) replacing the traditional melting fuses used for wire harness protection. These solutions offer benefits such as less variability in fuse-time currents, which can then potentially reduce the cable diameter, weight and cost of the wire harness. Semiconductor switches are also resettable remotely, which means that the fuses do not have to be easily accessible, giving designers the ability to place the fuses in locations that can reduce cable lengths from the power source to the load.

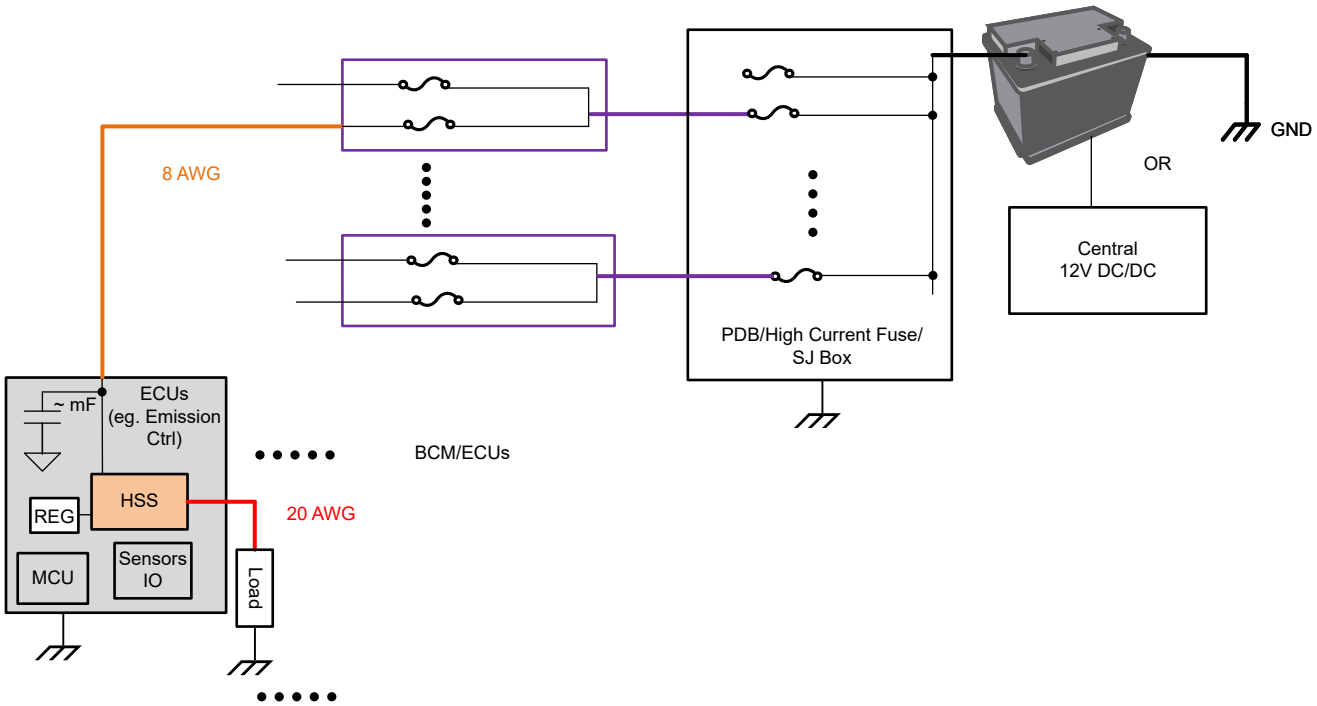

Figure 1. *Domain-based Power distribution architecture.*

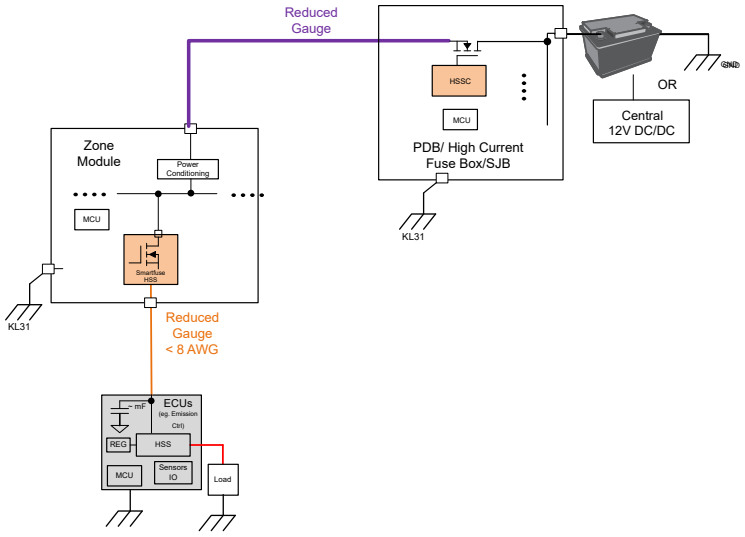

Figure 2. *Zone-based Power distribution architecture.*

The system design challenges when using semiconductor switches as smart fuse devices include lowering the quiescent current when the switch is in the on state, as well as turning on outputs powering large capacitive loads typically seen at the load (the electronic control unit [ECU] input). ECUs have an input capacitance ranging from 47µF to 5mF and startup time considerations (fast charging time <1ms, medium charging time <10ms, slow charging time <50ms) based on the ECU type and number of ECUs connected together on each Power Distribution Box (PDB) output. Charging these ECU input capacitors through the metal-oxide semiconductor field-effect transistor (MOSFET) switch within the ECU startup time is one of the primary system design challenges of a zone-based architecture.

In this article, we'll discuss various techniques to address the challenge of driving capacitive loads using high-side switch controllers.

Output-voltage slew-rate control

In this method, placing the capacitor (C) between gate-GND, the slew rate of the gate and the output voltage limits the inrush current. The circuit configuration with output voltage slew-rate control is shown in **Figure 3**.

Equation 1 and **Equation 2** calculate the inrush current and power dissipation at startup as:

$$I_{INR} = C_{OUT} \times \frac{dV_{OUT}}{dt} \quad (1)$$

$$P_{D(Vout = 0)} = V_{IN} \times I_{INR} \quad (2)$$

Because the MOSFET is operating in a saturation region, the inrush current should be low enough to keep the power dissipation within its safe operating area (SOA) during startup. MOSFETs can handle more energy (1/2 $C_{OUT}V_{IN}^{2}$) when their power dissipation is reduced and spread over longer durations. Thus, the inrush interval needs to stretch out over a longer period of time to support higher capacitive loads.

This method is suitable for slow charging requirements (for example, 5mF and 50ms), but the design must always include a trade-off between C_{OUT}, the FET SOA, the charging time and the operating temperature. For example, charging 5mF to 12V takes 40ms with an inrush current limit of 1.5A using TI's high-side, switching controller, the **TPS1211-Q1** as gate driver. Reference [**11**] iterates a procedure on how to check the FET SOA during startup using this method, while reference [**2**] is an online tool for estimating the SOA margin for a specific MOSFET.

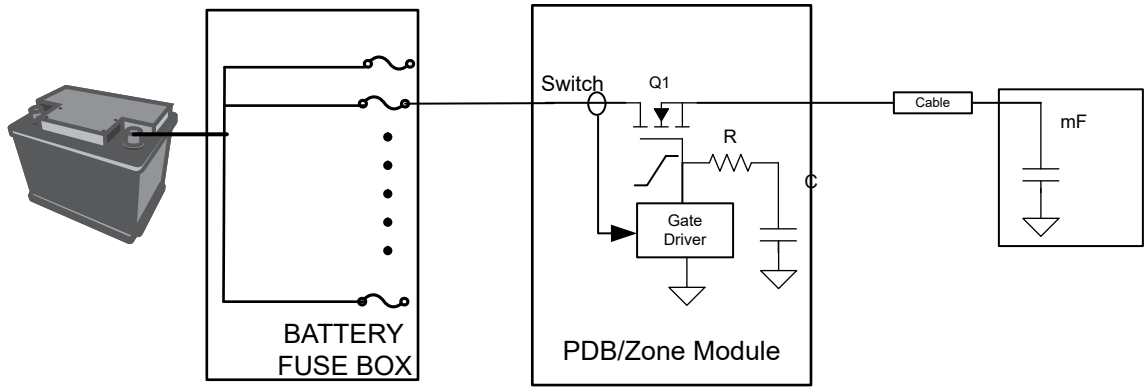

Figure 3. *Circuit for output voltage slew-rate control.*

Parallel precharge path

This approach is typically used in high-current parallel FET-based designs that need an additional gate driver to drive a precharge FET, as shown in **Figure 4**. You can use **Equation 3** to select the precharge resistor (Rpre-ch) in the precharge path to limit the inrush current to a specific value:

$$R_{pre-ch} = \frac{V_{IN}}{I_{INR}} \quad (3)$$

Because the precharge resistor handles all of the power stress during startup, it should be able to handle both average and peak power dissipation, expressed by **Equation 4** and **Equation 5**:

$$P_{avg} = \frac{E_{pre-ch}}{T_{pre-ch}} = \frac{0.5 \times C_{OUT} \times V_{IN}^2}{5 \times R_{pre-ch} \times C_{OUT}} \quad (4)$$

$$P_{peak} = \frac{V_{IN}^2}{R_{pre-ch}} \quad (5)$$

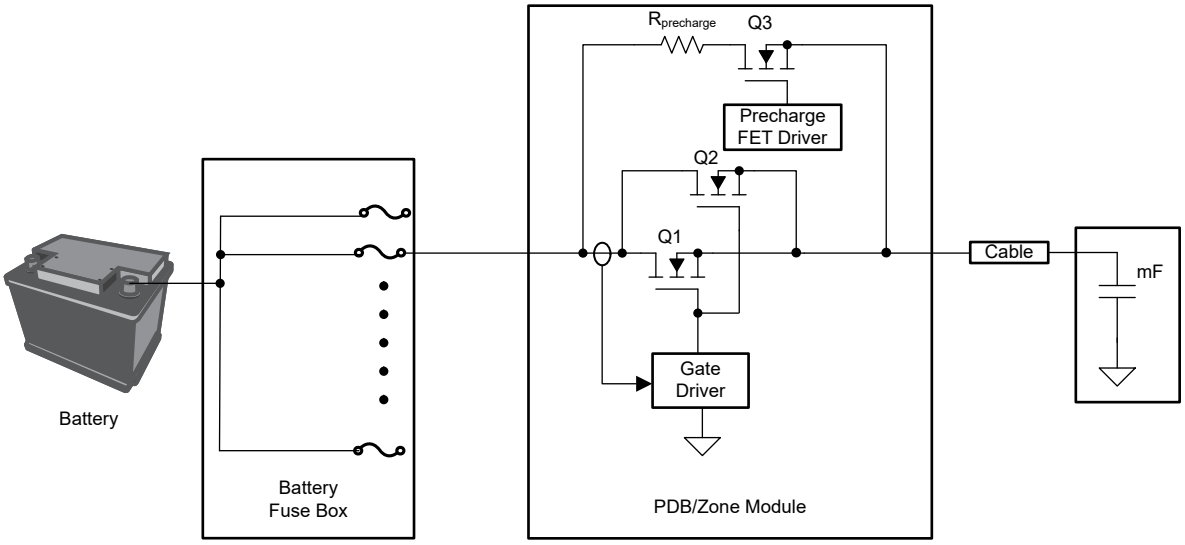

Figure 4. *Circuit with a precharge resistor and FET in a parallel path.*

In this case, fast output charging is possible – at the cost of a very bulky precharge resistor. For example, charging 5mF to 12V in 10ms would require a 0.4Ω precharge resistor at a 36W rating with a peak power-handling capacity of 360W, resulting in a bulky wire-wound resistor. Thus, this solution is not viable for many types of end equipment, as there are many channels on the same PCB. Each channel would need a bulky resistor, resulting in a space-inefficient solution.

Automatic PWM-based capacitor charging

As shown in **Figure 5**, the high-side driver outputs in the PCB connect to remote ECUs through lengthy cables varying from 1m to several meters. As an example, a 50A wire (8AWG) harness has 2mΩ-per-meter and 1.5µH-per-meter characteristics. The D1 diode is a part of the system design that allows the freewheel path for the cable harness inductive current. The high-side drivers have strong gate-drive outputs capable of driving FETs in parallel with short (<1µs) turnon and turnoff times, providing overcurrent and short-circuit protection. The cable parasitic, D1 diode and high-side MOSFETs form a typical buck regulator configuration.

During startup, the uncharged output capacitor draws inrush current and triggers a short-circuit event when the inrush current hits the short-circuit protection threshold (I_{SCP}). The high-side driver turns off the power path and reinitiates turnon after a retry period ($T_{AUTO-RETRY}$). This process continues until the output capacitance is fully charged, as shown in **Figure 6**, after which the high-side driver goes into normal operation and drives the load.

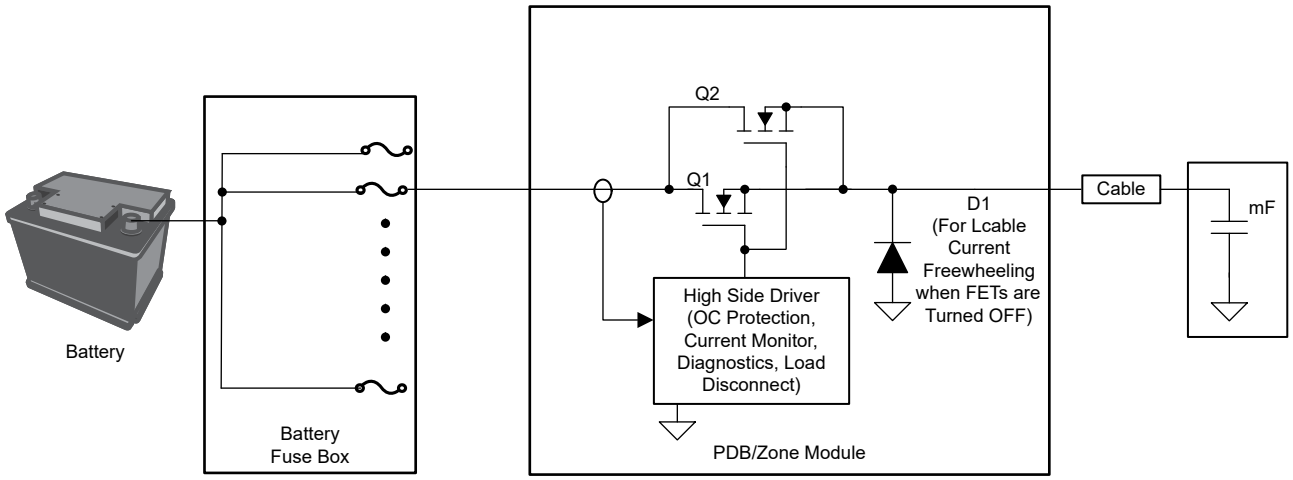

Figure 5. *Circuit representation for pulse-width modulation (PWM) charging using a high-side driver.*

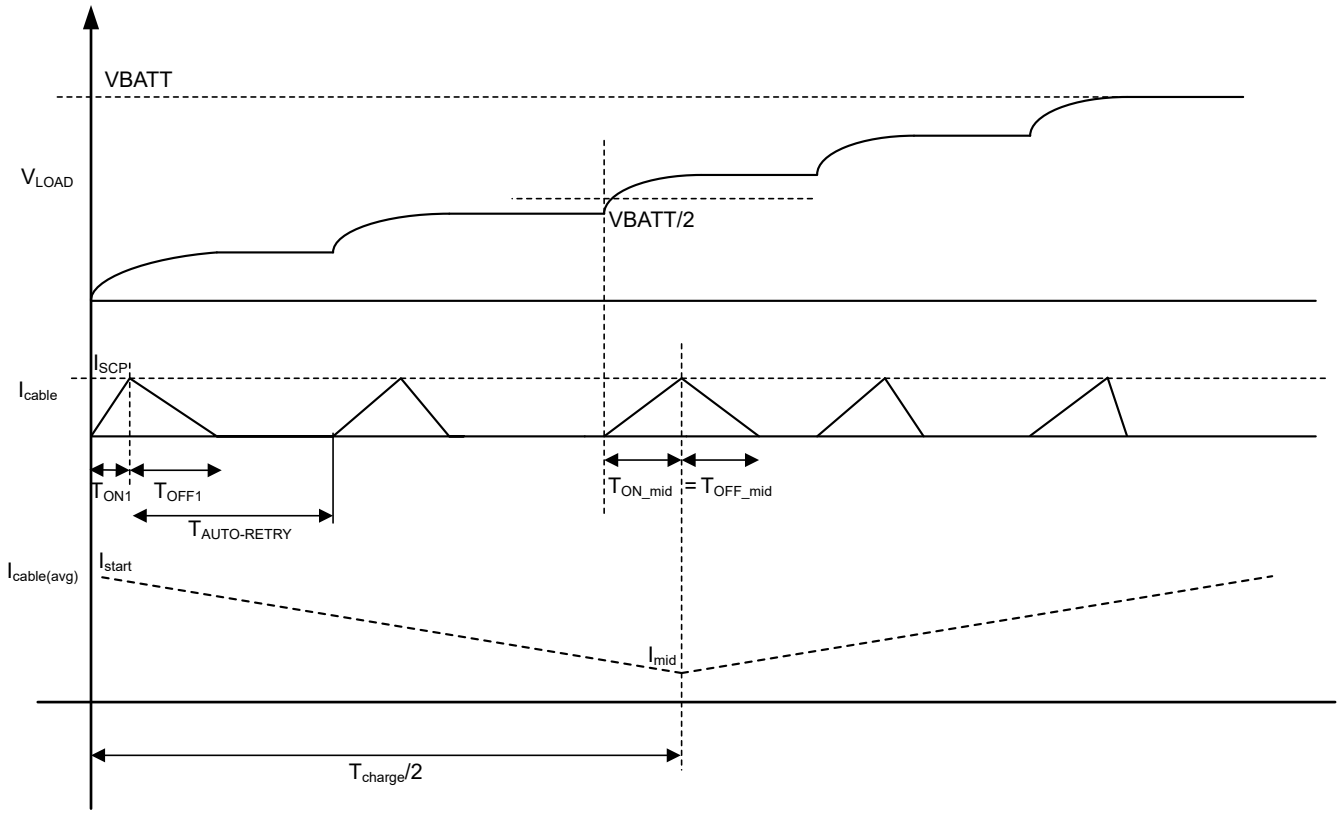

Figure 6. *PWM charging method conceptual waveforms during startup.*

Figure 7 illustrates the control operation. As you can see, this approach has two variables, I_{SCP} and $T_{AUTO-RETRY}$, which need to be set for the high-side driver based on the input voltage (V_{IN}), load capacitance and required charging time. A higher I_{SCP} threshold or a shorter $T_{AUTO-RETRY}$ delay allow faster output charging, making the solution universal for any value of load capacitance.

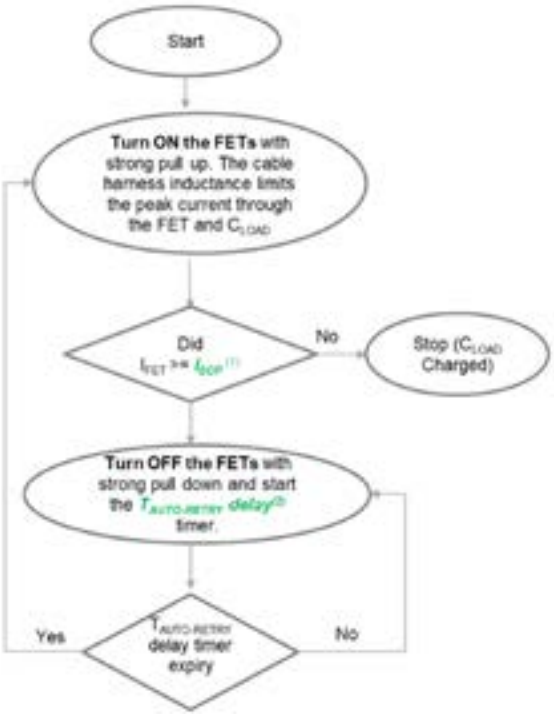

Figure 7. *Flow chart of the PWM charging control method.*

This solution leverages the existing available real estate in a typical high-side driver system (the cable harness inductance and D1 diode) and creates an efficient charging method by operating the high-side MOSFETs in switching mode. Unlike traditional approaches, the proposed solution no longer depends on the FET SOA and does not require bulky precharge resistors, nor a precharge FET and driver. The solution uses the inherent short-circuit protection feature of the high-side driver and runs autonomously without any external control signals or complex algorithms.

Design considerations and test results

Consider this system design example for a 50A load:

- Battery voltage (V_{BATT}) = 12V.
- Load capacitance (C_{LOAD}) = 5mF.
- 1.5m cable = 8AWG connecting the high-side driver to the ECU, leading to L_{cable} = 2.25µH.
- Charging time (T_{charge}) = 10ms
- Freewheeling diode drop (V_{D1}) = 0.7V.

The design involves selecting the I_{SCP} and $T_{AUTO\text{-}RETRY}$ parameters. For a 50A load design, the I_{SCP} threshold is usually set at 20% above the maximum load current, so in this example, that would be 50A × 1.2 = 60A.

Now, to compute $T_{AUTO\text{-}RETRY}$, see **Figure 6** and use the current-voltage relationship of the capacitor at the midpoint of $T_{charge}/2$ to get **Equation 6**:

$$\frac{(I_{start} + I_{mid})}{3} \times \frac{T_{charge}}{2} = C_{LOAD} \times \frac{V_{BATT}}{2} \quad (6)$$

where:

$$I_{start} = \frac{I_{SCP} \times (T_{ON1} + T_{OFF1})}{2 \times (T_{ON1} + T_{AUTO-RETRY})} \quad (7)$$

and

$$I_{mid} = \frac{I_{SCP} \times 2 \times T_{ON\_mid}}{2 \times (T_{ON\_mid} + T_{AUTO-RETRY})} \quad (8)$$

The time intervals TON1, TOFF1 and TON_mid can be calculated using **Equation 9** to **Equation 11**:

$$T_{ON1} = \frac{L_{cable} \times I_{SCP}}{V_{BATT}} \quad (9)$$

$$T_{OFF1} = \frac{L_{cable} \times I_{SCP}}{V_{D1}} \quad (10)$$

$$T_{ON\_mid} = \frac{L_{cable} \times I_{SCP}}{\left(\frac{V_{BATT}}{2}\right)} \quad (11)$$

Substituting the known parameters V_{BATT}, L_{cable}, I_{SCP}, V_{D1} and C_{LOAD} and solving for $T_{AUTO\text{-}RETRY}$ gives a retry delay of <200µs to achieve a charging time of 10ms.

Figure 8 and **Figure 9** show the application schematic and test setup to charge a 5mF load capacitance using the TPS1211-Q1 high-side driver. $T_{AUTO\text{-}RETRY}$ is 180µs, which results in a charging time of 7ms, as shown in **Figure 10**.

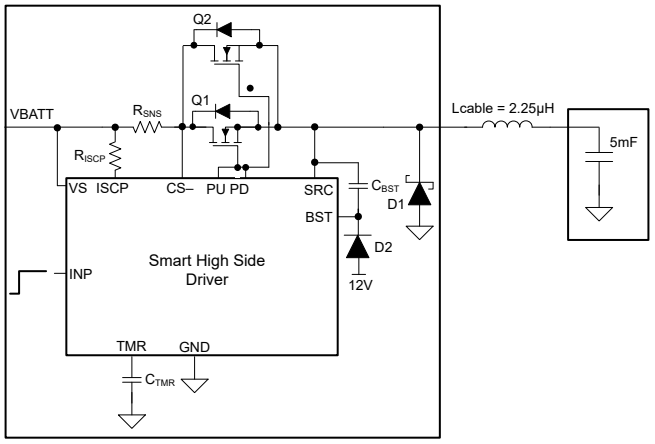

Figure 8. *Typical application schematic for driving a capacitive load.*

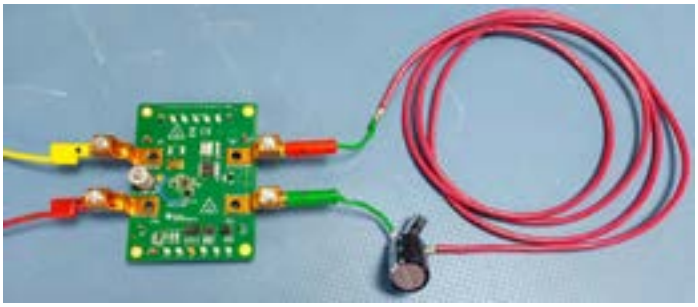

Figure 9. *Test setup using the TPS1211-Q1 evaluation module with a 1.5m cable harness.*

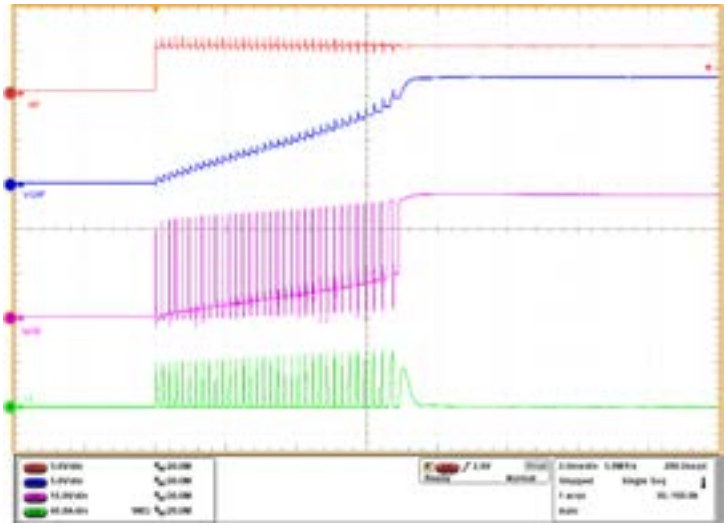

Figure 10. *Startup with a 5mF load capacitance using the TPS1211-Q1 in switching mode.*

Conclusion

Semiconductor-based smart fuse solutions are gaining popularity over traditional melting fuses in automotive power distribution given their significantly improved fuse time-current characteristics and resettability through software. These benefits enable a reduction in overall cable harness weight because the cables are thinner and shorter.

One of the system design challenges with semiconductor-based smart fuse solutions is whether the capacitor load charging can meet the system startup time requirements. TI's high-side switch controller devices offer various techniques to address the challenges of capacitive load driving.

References

1. Rogachev, Artem. 2014. "**Robust Hot Swap Design**." Texas Instruments application report, literature No. SLVA673A, April 2014.
2. **FET SOA Margin Calculator for dv/dt-Based Startup**

Related Websites

- **TPS1211-Q1**
- **TPS1200-Q1**

The art of passive matching a high-speed ADC analog-input front end

Rob Reeder
Application Engineer
High-Speed Converter Group

Luke Allen
Application Engineer
High-Speed Converter Group

Introduction

Understanding the mechanisms involved in designing high-speed analog-to-digital converter (ADC) front ends is sometimes like an art of its own. Simply placing a balun down and drawing two trace lines from the balun's secondary outputs to the ADC's inputs is not recommended for any high-speed analog receiver front end design. Baluns are notorious for being parasitic-sensitive on bandwidth, along with other nuisances. In this article, we'll show you how to get the most out of your passive analog-input design using a balun. The added benefit is that you don't need a costly balun nor a costly attenuation pad in order to achieve the bandwidth you want.

The art of choosing the right balun or transformer

Let's begin with the assumption that you don't need to DC-couple; that is, sample the DC frequency bin. Because a balun does not require an additional power supply, the advantages of using one include lower overall power consumption and smaller board space requirements. Additionally, with no extra power supply to contend with, a balun won't add noise to the overall radio-frequency (RF) signal chain that leads up to the ADC itself, which means that no degradation in the signal-to-noise ratio (SNR) or noise spectral density will occur.

Figure 1 shows two different baluns used in the same application with TI's 16-bit, dual-channel **ADC3669** ADC. Even though both baluns are rated for the same bandwidth, they will ultimately respond differently given the combination of the ADC's varying input impedance from the ADC's internal sample network, as well as the printed circuit board (PCB) trace parasitics itself. Notice that with no "match" applied with either balun, the bandwidth falls quite rapidly [1].

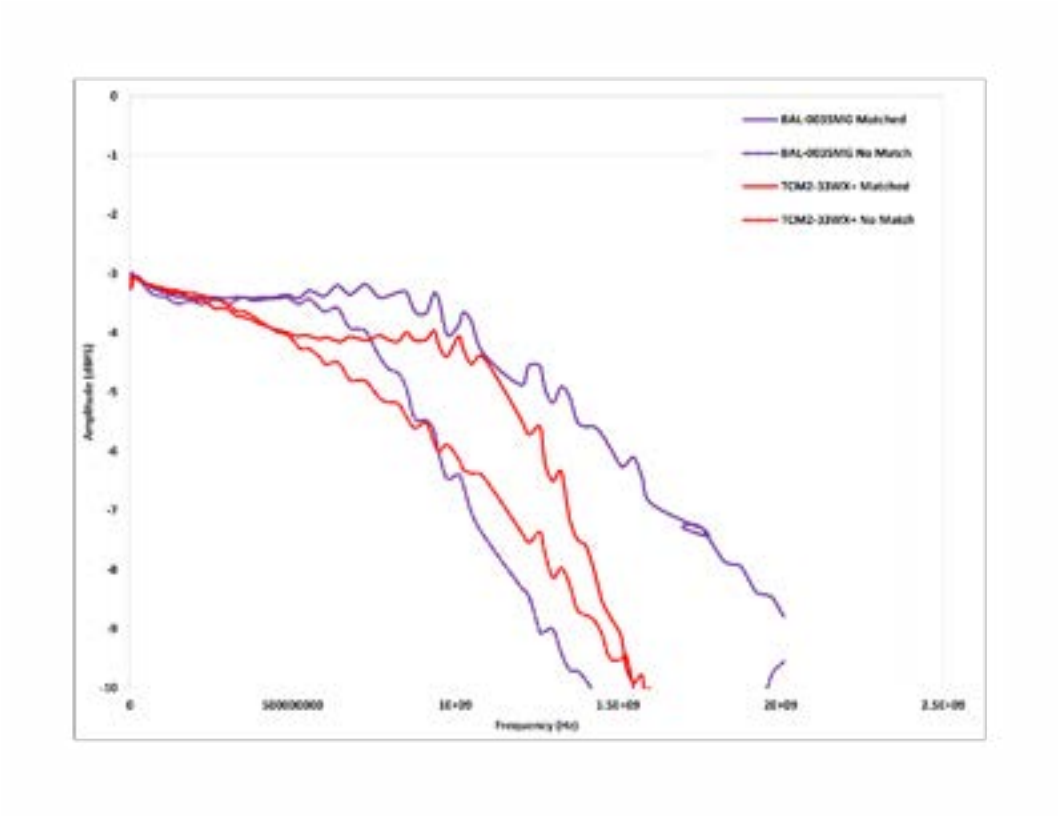

Figure 1. *ADC3669 and balun bandwidth comparison: match (solid lines) vs. no match (dashed lines).*

Take a close look at the balun's PCB footprint and layout recommendation in the data sheet. We recommend following these recommendations exactly, or else the balun will respond differently. The balun was characterized using this footprint both for data-sheet collection and measuring its S-parameters, and will only perform up to specifications under these circumstances.

To understand the balun's phase imbalance over your specific bandwidth, note that the poorer the balun's inherent phase imbalance, the worse even-order distortion (second harmonic distortion [HD2]) the ADC will manifest. If HD2 is important to your frequency planning application, we recommend picking a balun with good phase imbalance. There is really no good guidance on this, as each ADC can also have its own sensitivity to phase differences across its usable frequency range. Typically, choosing a balun with ≤5 degrees of phase imbalance over your application's operating bandwidth would be a good start. This amount of phase imbalance would add little to the aggregate even-order distortion already existing in your RF signal-chain lineup [2].

Figure 2 shows the difference between the same two matched baluns scenarios, and its impact on even-order distortion using the **ADC3669**. Notice that the third harmonic distortion (HD3) is relatively the same across frequency and has no significant differences.

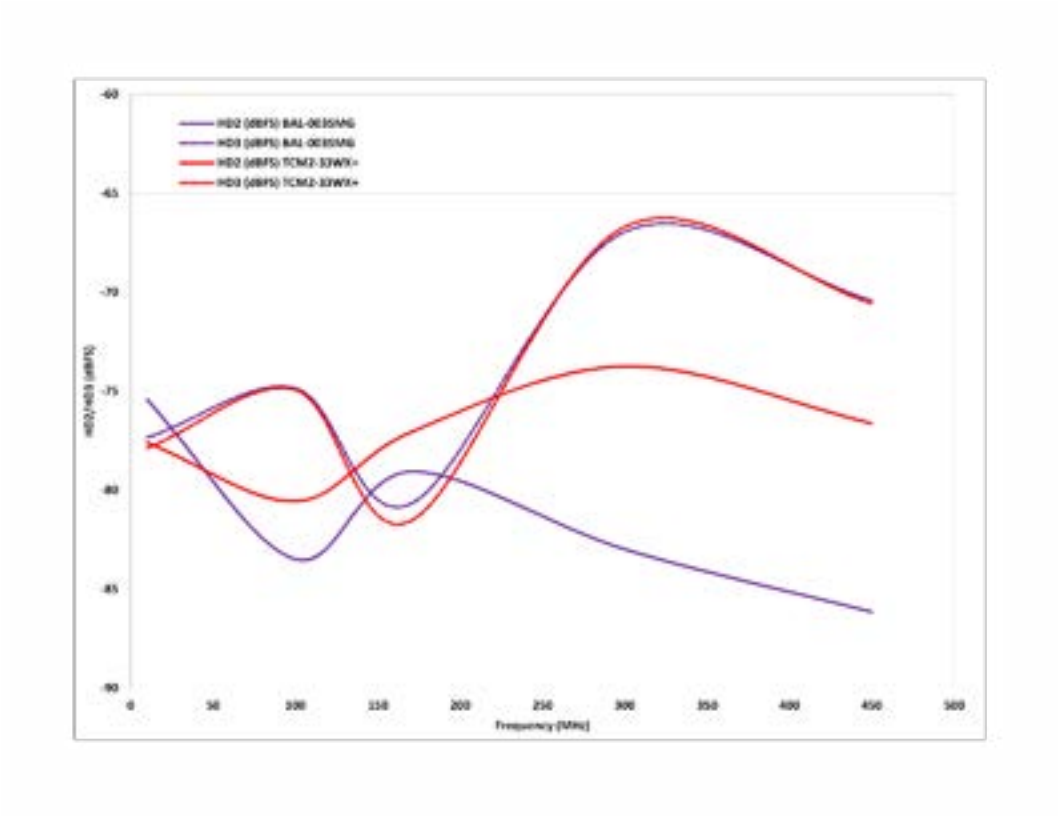

Figure 2. *ADC3669 HD2 and HD3 comparison between two baluns: high cost vs. lower cost.*

The art of choosing the right balun matching network

Over the years, there have been many attempts to simulate and perfect the balun match. After weeks to months of simulation and trying to understand some level of PCB parasitics, it's still possible that the match will not work out in your favor when fabricating the PCB design. We suggest starting the design process differently, using the topology shown in **Figure 3**.

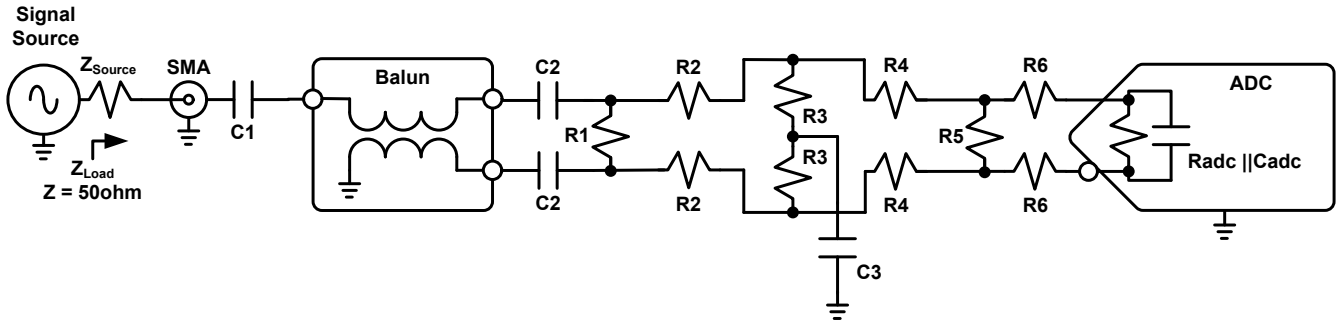

Figure 3. *Generalized passive network component placeholders.*

If you're wondering whether all of this effort and trade-offs are actually worth it, we suggest referring back to **Figure 1**.

Let's describe each component so that you know its need or function within the input matching network to the ADC:

- C1, C2. Typically 0.1µF, these components block DC from being fed into the balun or transformer. Some balun designs lead to ground, DC, or both, and may aggravate the balun's function, leading to poor performance.
- R1. This component enables back termination near the outputs of the balun after the DC blocking capacitors. If your trace lengths are long enough, you may need this component. Assuming that no perfect match across the band of interest is achievable, you may need to back terminate in order to handle any standing waves that accumulate as the imperfect match rolls back and forth across your frequency range.
- R2, R3, R4. These components enable you to employ various matching techniques and can take the form of several combinations in order to solve a balun and ADC matching conundrum. For the widest band matches, R2, R3 and R4 are generally configured as a matching pad, which helps dissolve the standing waves between the balun and ADC and provides a "stiff" 50Ω impedance that both the balun and the ADC need. Though these components are represented as resistors, they can take the form of capacitors or inductors as well.
- C3. This capacitor, typically 0.1µF, ties the center point of the R3s together and enables an AC current path. Adding C3 is also a good idea, because when over-ranging the ADC's input full scale, C3 allows this AC current to go somewhere. C3 could also be located at R5 instead.
- R5. This component allows back termination on the opposite side near the ADC's inputs, and is not always necessary. R5 provides the same function as R1, but from the opposite perspective in order to help resolve standing waves that may accumulate. Typically, R1 or R5 are required when trace connections are ≥300mils in length.
- R6. This is a kickback component, typically in the form of resistors, but in some cases inductors or low-Q ferrite beads that can help snub any residual charge kickback that comes back onto the analog input network from the internal sampling circuit in the ADC. These component placeholders are essential when using unbuffered ADCs.

Again, be wary if you just plan to run two traces from the output of the balun to the inputs of the ADC. Even if you collect S-parameters, simulate and prove the design to your colleagues, this methodology could prove to be costly unless you have previous experience with the balun and ADC combo.

Art using the ADC3669

Our example uses the 16-bit, dual-channel **ADC3669** ADC for a wideband front end match design of 1.5GHz of analog sampling bandwidth. The example also uses the **TCM2-33WX+** balun from Mini-Circuits, which has 3GHz of bandwidth and low insertion loss compared to higher-cost baluns that are easier to match with. This balun also has very good phase imbalance, <5degrees, when compared to other lower-cost baluns across the same frequency range.

Using the generalized circuit in **Figure 3**, the components needed are not purely resistive to define the match. In this case, we will use a resistor (R), internal parasitic capacitance (C) and inductor (L) (R2, R3 and R6) approach; see **Figure 4**.

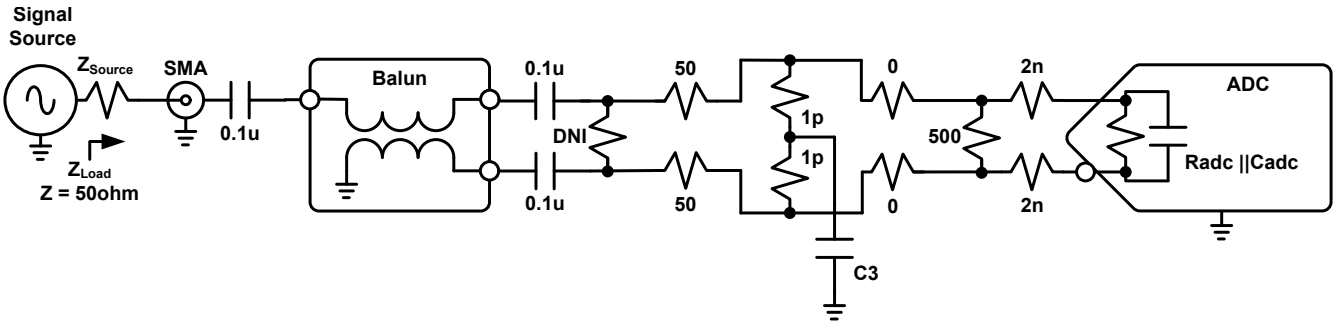

Figure 4. *Finalized passive network match.*

PCB parasitics will still be an issue, necessitating that you test a few different iterations on your board.

Get both sets of S-parameters (if available) for the balun and ADC and use your favorite simulation software. Use the matching network format given in **Figure 3** and one of these two approaches for R2, R3 and R4:

- The attenuation pad approach (approximately 8.6Ω, 140Ω and 8.6Ω for R2, R3 and R4, respectively) will give you a 3dB pad. To learn more about this approach, see the Electronic Products article, “Unraveling the Full-Scale Mysteries of Your RF Converter’s Analog Inputs.”
- The R, C and L approach for R2, R3 and R4, respectively, helps resonate away the ADC’s C using L as the last component. This approach will flatten out the bandwidth, allowing the balun to perform at its rated bandwidth. This approach does take a bit of iteration, however.

The goal here is to not use a lossy attenuation pad. Therefore, to give more context to the R, C and L approach, see **Figure 5**, **Figure 6** and **Figure 7** as varying the L, C and R, respectively, in the network (see **Figure 4**) and its role in defining the ultimate bandwidth and network match.

Figure 5 shows how changing the value of L around influences the bandwidth while keeping all other component values the same. Notice that as L increases in value the bandwidth is slowly reduced. This means that the L value is having an adverse reactive effect on the C of the ADC.

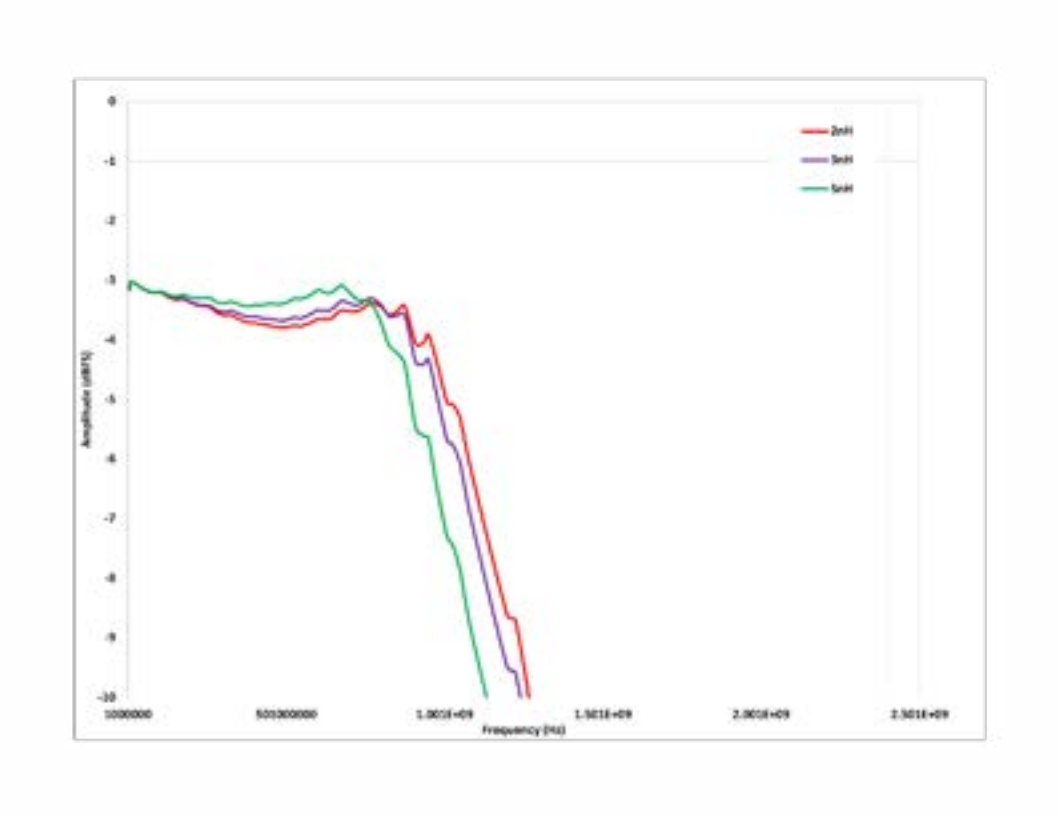

Figure 5. *Passband flatness response with various L values at R4.*

Figure 6 shows how moving the value of C around influences the bandwidth while keeping all other component values the same. Notice that as the value of C reduces, the bandwidth is slowly improving – at the cost of bandwidth flatness. This means that the C value is having a reactive effect on the balun's return loss over frequency. These capacitors help preserve the balun's bandwidth vs. frequency.

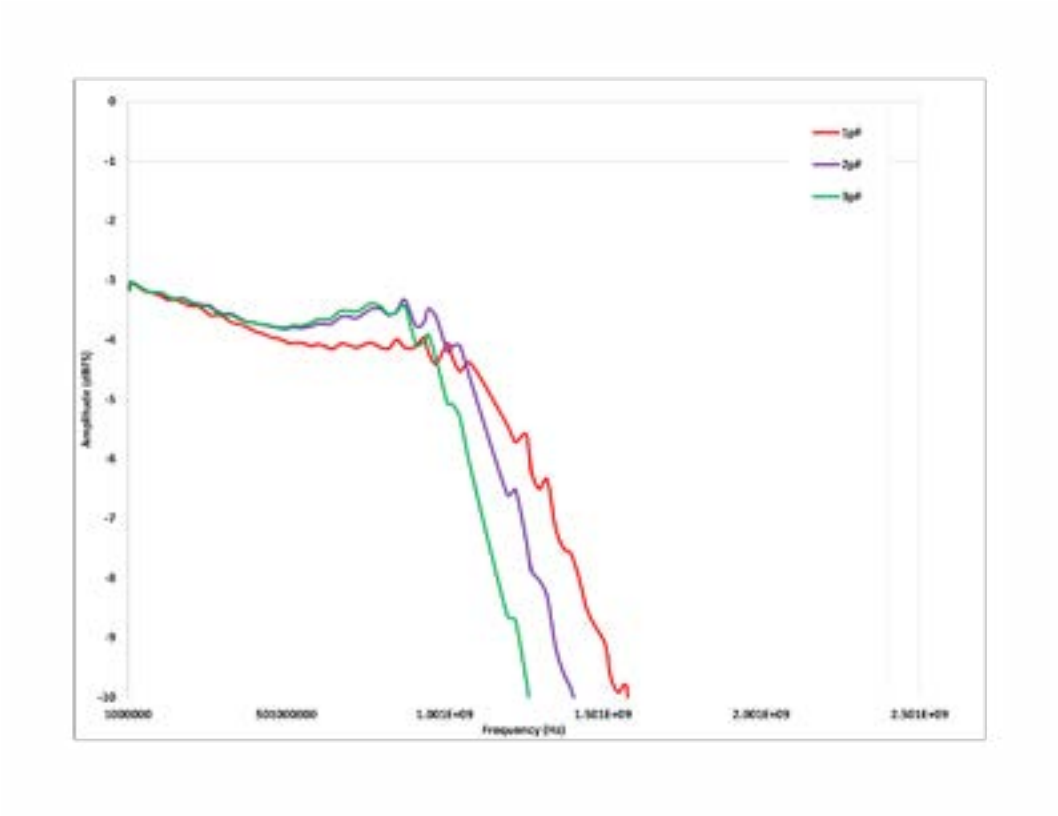

Figure 6. *Passband flatness response with various C values at R3.*

Figure 7 shows how moving the value of R around influences the bandwidth while keeping all other component values the same. Notice that as R increases in value, the bandwidth is slowly improving – at the cost of flatness or peaking in the bandwidth response. The effect of R's value is almost the same as the effect of L, therefore preserving the impedance requirements that both the balun and ADC should have in conjunction with each other.

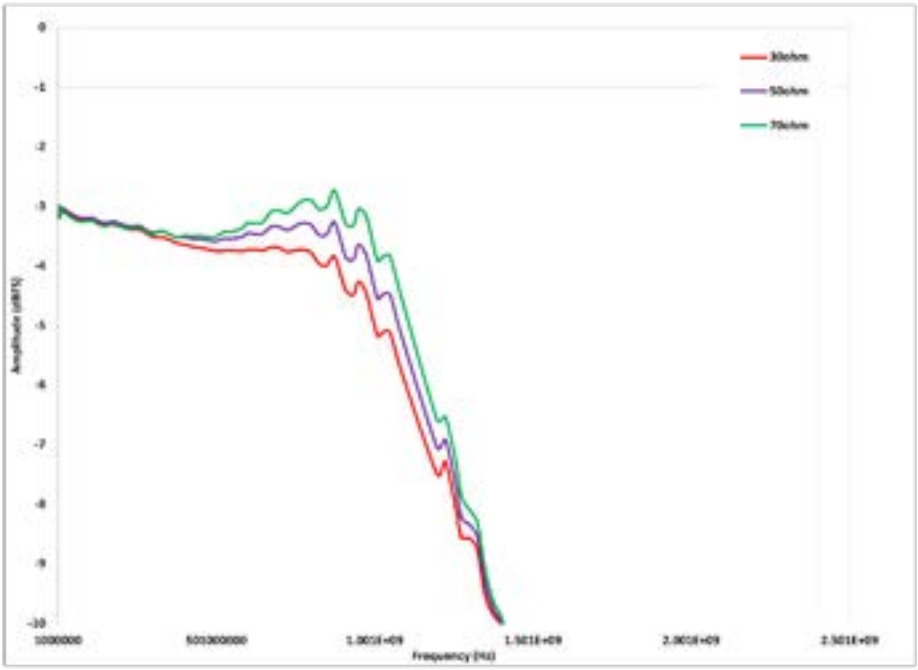

Figure 7. *Passband flatness response with various R values at R2.*

Simulating the R, C and L approach would give you a good starting point, using the “tune” feature in simulation software, and enables you to see the roles that each component plays in the network match. Settling on some good starting values can help define which direction to go when iterating and perfecting the match as needed for your application.

During the matching design effort, completing an AC performance sweep across the application bandwidth of the converter will give you insight as to how the performance is coming along dynamically, and ensure that nothing has gone wrong with the ADC.

Figure 8 illustrates the AC performance (SNR and spurious-free dynamic range [SFDR]) measured across the bandwidth of the **ADC3669**, using the method we’ve described to match the input network to 1.5GHz.

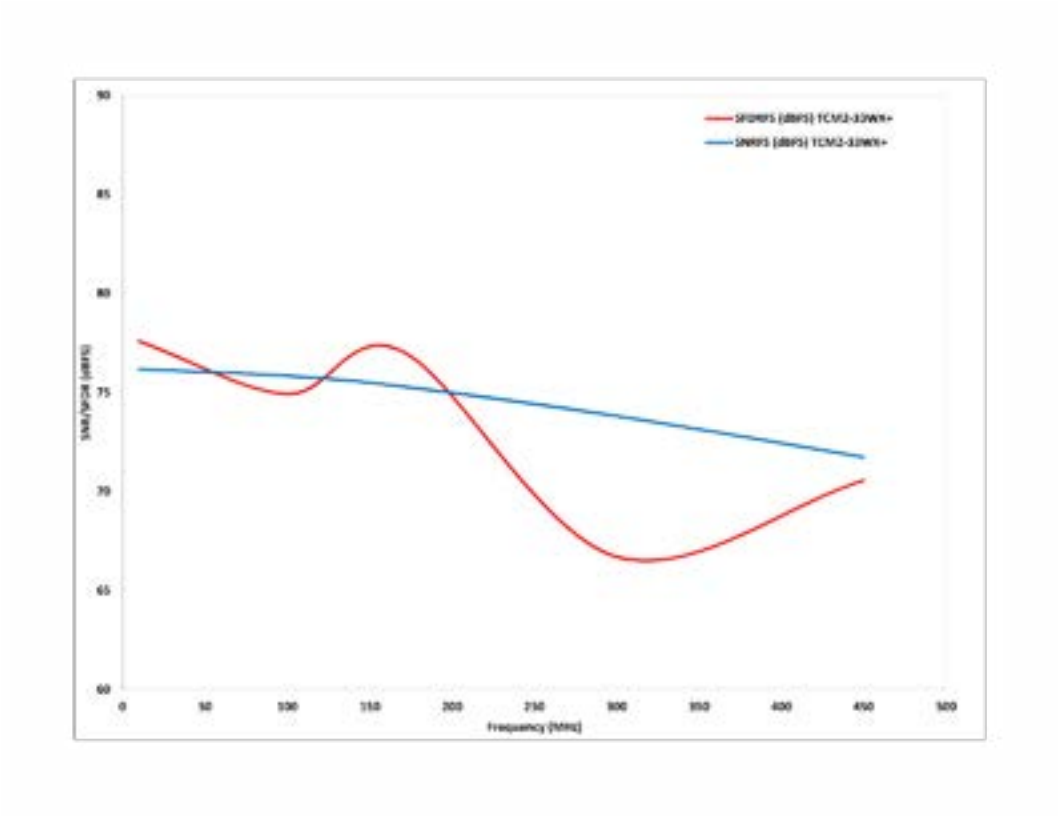

Figure 8. *Final matched network AC performance (SNR/SFDR) vs. frequency.*

Conclusion

Here are the basic steps when approaching a balun and ADC matching network design in the gigahertz region, in order to prevent your next matching effort from being bandwidth-hampered:

- Choose a balun or transformer that has some bandwidth overage for your particular application.
- If HD2 is important to your frequency application, choose a balun with ≤5 degrees of phase imbalance.
- A simplified input network can provide the initial placeholders required in most matching efforts when using a balun or amplifier and ADC.
- You may not need every component listed, but initially they can be beneficial, as it is not possible to capture all board layout and PCB parasitics in simulation.
- Understand the trade-offs that can affect your bandwidth performance. Some of these trade-offs can affect the linearity performance of the ADC.

References

1. Reeder, Rob. 2022. "**A Close Look at Active vs. Passive RF Converter Front Ends**." Planet Analog, Jan. 24, 2022.
2. Reeder, Rob. 2022. "**Evaluating high-speed RF converter front-end architectures**." Planet Analog, April 7, 2022

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265