How to use isolation to improve ESD, EFT and surge immunity in industrial systems

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Introduction

Industrial equipment is expected to operate reliably in harsh environments. The cables connecting equipment inputs and outputs can pick up voltage and current noise from a variety of disturbances. For example, cables near motors can pick up high-voltage and high-frequency electrical fast transients (EFTs). Lightning strikes (causing surges) can couple inductively to long running cables, or couple indirectly through power supplies. Connectors and exposed parts can be subject to electrostatic discharge (ESD) if they come in contact with a human operator during operation or maintenance. Industrial equipment must withstand these disturbances and continue to function normally.

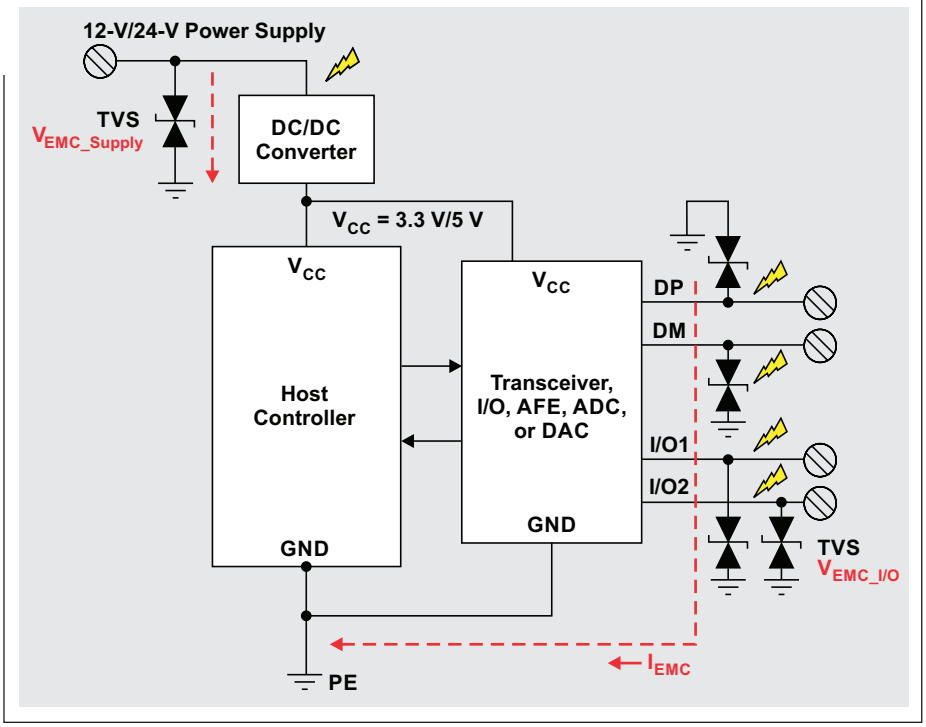
Achieving good electromagnetic compatibility (EMC) is different for isolated systems when compared to non-isolated systems. This article discusses how to use isolation to improve ESD, EFT and surge immunity. Improvements in performance and reduced system cost are possible through careful design.

Voltages and currents during EMC testing: Non-isolated systems

Reference 1 provides details of the voltage and current profiles of noise pulses and timing sequences associated with the International Electrotechnical Commission (IEC) for ESD, EFT and surge tests. Figure 1 shows a block diagram of a non-isolated system, and indicates the voltages and currents that are created due to an ESD, EFT or surge transient. In a non-isolated system, all circuitry, including any transient protection devices, connect to protective earth (PE). Modern transient voltage suppressors (TVSs) are the preferred protection components for high-speed data transmission because of their low capacitance, which enables them to be designed into every node of a multi-node network without requiring a reduction in data rate.

With response times of a few picoseconds and power ratings up to several kilowatts, TVS diodes present the most effective protection against ESD, burst EFT and surge transients. Transient protection devices conduct the

Figure 1. Voltage and currents during transient immunity tests in a non-isolated system



large currents induced during transient events to the PE. You must design transient protection such that the voltages on the supply and I/O pins are clamped below the maximum voltage ratings of the circuits connected to those terminals. For example, a TVS diode that clamps to 50 V for a 1-kV surge transient can protect transceivers and I/O circuits that can tolerate peak voltages up to 50 V. You may require additional components, such as ballasting resistors, to help protect the I/O circuitry if the clamping voltage of the TVS is much higher than the safe operating voltage of the transceiver circuits. Reference 1 discusses protection circuits for non-isolated RS-485 transceivers.

During a transient event on the transceiver and I/O pins, the transient protection devices clamp to a certain clamping voltage, V_C. This clamping causes a loss of regular signaling on the communication channel, drowned out by the energy of the transient pulse and potentially causing glitches or error pulses in the communication link. The error pulses are at least as wide as the transient-noise pulses (100 ns for ESD and EFT and 100 µs for surge) and repeat according to the test-repetition patterns. In order to meet Criterion A (no performance degradation during the application of noise transients), you must filter out these error pulses with resistor-capacitor filters, digital filters in the host controller, or through error detection and retransmission. However, these methods reduce the throughput of the communication channel, add cost and put an additional computational load on the host controller.

Voltages and currents during EMC testing: Isolated systems

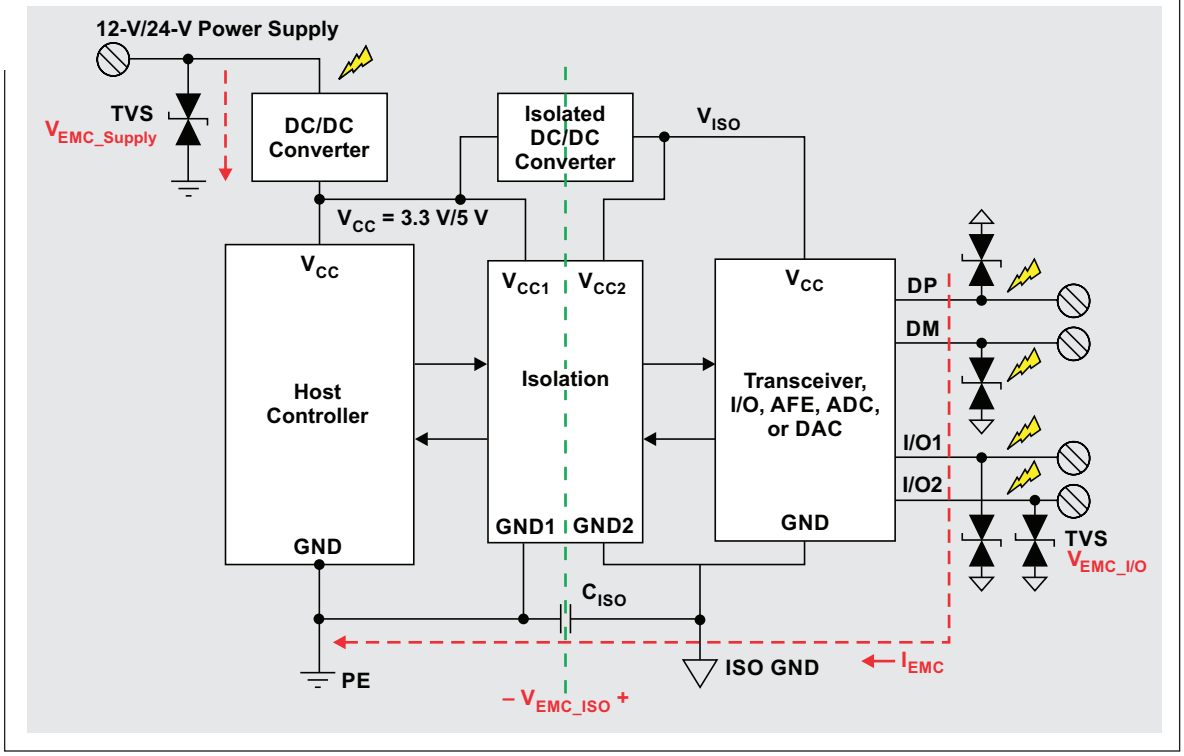
Figure 2 shows a block diagram of an isolated system, and indicates the voltages and currents that are created due to an ESD, EFT or surge event. In this example, the transceivers and other I/O ports are isolated from the host controller using a digital isolator. The host controller is referenced to PE. The interface side (or hot side) of the system, including transient protection devices, is referenced to a "floating" isolated ground (ISO GND). An isolated DC/DC converter generates the power supply for the hot side. Between the ISO GND and the PE is a parasitic capacitor, C_{ISO}. C_{ISO} is the sum of the isolation/barrier capacitances of all of the isolation elements used (isolators, optocouplers, transformers) and any capacitance introduced by the printed circuit board.

You can create electrical models of the different transient events using the voltage and current profiles defined in the standards, with the defined output impedances of the generators and clamping circuits. The block diagram in Figure 2 simulates the impact of transient events.

Voltage across the isolation barrier

During a transient event on the interface pins, the transient protection devices turn on with a relatively low voltage drop across them. This causes the entire open-circuit voltage of the transient pulse to appear across the isolation barrier. For example, an 8-kV ESD strike on the

Figure 2. Voltage and currents during transient immunity tests in an isolated system



interface pins will cause an 8-kV stress on the isolation barrier (between ISO GND and PE).

You can reduce the voltage stress across the isolation barrier by using additional safety certified capacitors (extra components) across the barrier, increasing the effective value of C_{ISO}. Short-duration ESD and EFT pulses are easier to filter than a surge.

Simulation results in Figure 3a show the filtering of an 8-kV ESD strike to less than 5 kV, with C_{ISO} equal to 100 pF. Figure 3b shows the attenuation of a 4-kV EFT pulse to less than 2 kV, with C_{ISO} = 1 nF.

Only a few signal-isolation technologies available in the market today (Texas Instruments reinforced isolators included) can handle 8-kV ESD and 4-kV EFT events across the barrier. The others would need an additional safety certified capacitor to reduce the barrier stress to acceptable levels. While the obvious disadvantage of an extra safety certified capacitor is an increase in system cost, there are other disadvantages as discussed in the next section.

Surge pulses are wider and thus more difficult to filter with a reasonable C_{ISO} value. At the same time, most isolation barriers are able to handle the 1-kV to 2-kV surge levels required for industrial systems, thus needing no additional filtering.

References 2 and 3 discuss the insulation specifications and transient voltage tolerance of TI reinforced isolators.

Current through transient protection devices

For the isolated system shown in Figure 2, the current loop for a transient event on the interface pin is completed through C_{ISO}. If you carefully design C_{ISO} to be low, it can present significant impedance to the transient event and drastically cut down the peak current through the transient protection devices. Slower transients like a surge see a higher impedance. As Figure 4 shows, with C_{ISO} = 10 pF, the peak current through the protection devices in an EFT event drops from 20 A in a non-isolated system to 1.8 A in an isolated system—an attenuation of 10x. The current

Figure 3. Simulation of voltage events across the isolation barrier

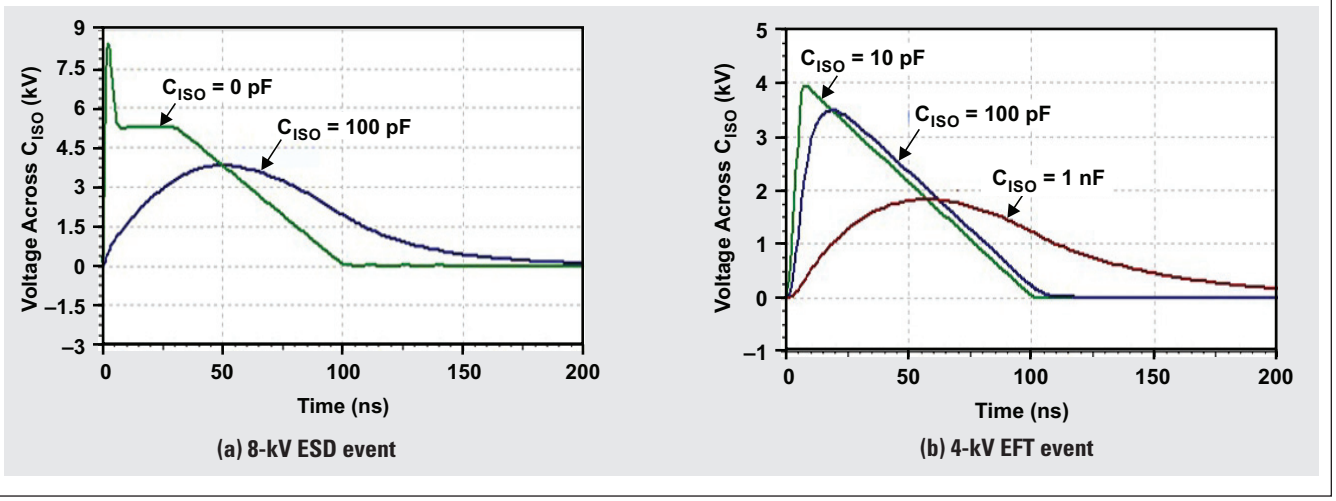
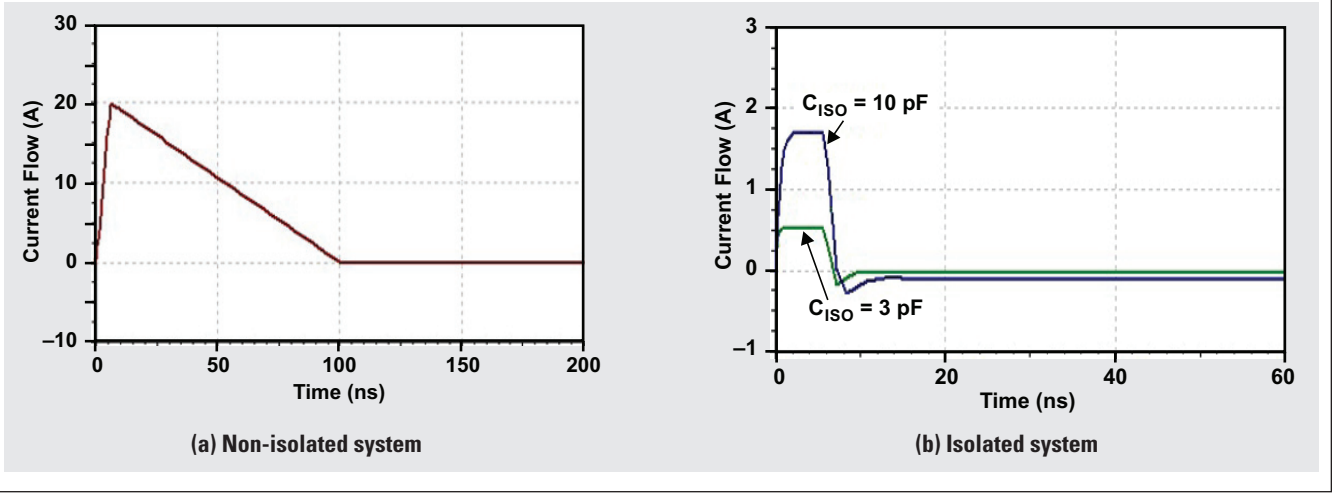


Figure 4. Simulation of current through protection devices during 1-kV EFT test



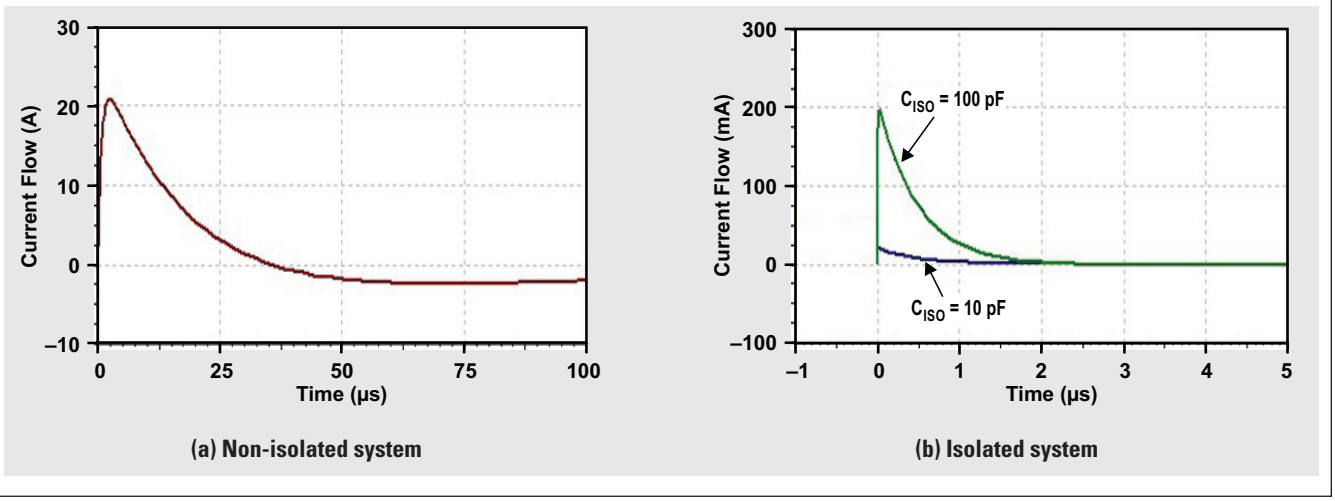
duration also reduces more than 10x, from 100 ns to less than 10 ns. Similarly, as Figure 5 shows, the peak current through the protection devices in a surge event drops more than 40x and the duration of the current is 100x smaller.

The reduction in amplitude and pulse width reduces the peak-current and peak-power requirements on external TVS protection, making them smaller and less costly. The peak power for surge events reduces from a few kilowatts to tens of a milliwatt, a very useful reduction. If C_{ISO} is low enough, and with reasonable on-chip transient protection on the transceivers, you can completely eliminate external transient protection.

Meeting Criterion A for EFT and surge

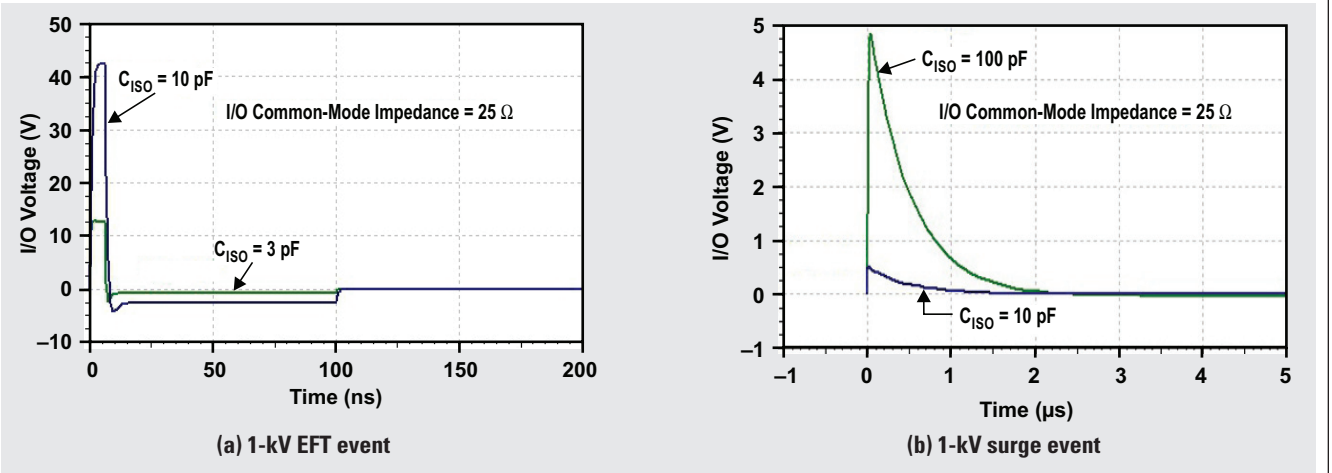
As discussed earlier, in a non-isolated system, the signal on the interface pins is drowned for the entire duration of the transient event: roughly 100 ns for an EFT event and 100 µs for a surge event. You must filter out the subsequent error pulses in the communication channel, resulting in extra cost, latency and reduction in data throughput. In an isolated system, since the current through transient protection devices lasts for a much smaller duration, the error pulses generated are narrower. As Figure 6 shows, the common-mode voltage excursions on a 25-Ω common-mode impedance transceiver or I/O can last for only 6 ns for an EFT event and 2 µs for a surge event. Such narrow error pulses are filtered more easily, and without much impact on throughput. The voltage excursions are contained to a few volts, which might enable the transceiver to function normally without any filtering at all. Thus, isolation can enable systems to meet Criterion A without trading off throughput or latency.

Figure 5. Simulation of current through protection devices during 1-kV surge test



(a) Non-isolated system (b) Isolated system

Figure 6. Simulation of voltage developed on an I/O with a 25-Ω common-mode impedance



(a) 1-kV EFT event (b) 1-kV surge event

Table 1. Reduction of peak current and duration of current pulse through isolation

Event	Non-Isolated System			Isolated System with C_{ISO} = 10 pF		
	Peak Current	Common-Mode Voltage Excursion[1]	Duration of Current-Pulse/Common-Mode Excursion	Peak Current	Common-Mode Voltage Excursion[1]	Duration of Current-Pulse/Common-Mode Excursion
EFT: 1 kV	20 A	V_C[2]	100 ns	1.8 A	44 V	6 ns
Surge: 1 kV	20 A	V_C[2]	100 µs	20 mA	0.5 V	2 µs

[1]Transceiver with 25-Ω common-mode impedance
[2]V_C is the clamping voltage of the external transient protection

Table 1 summarizes the reduction in current peaks and duration of peaks through isolation, reducing or eliminating the need for transient protection. For example, you can reduce the peak power during a surge event from 1.2 kW to 10 mW. The reduction in common-mode excursions during transient events also enables easier compliance with Criterion A.

Conclusion

The considerations for achieving good EMC performance in isolated systems and non-isolated systems differ. The open-circuit voltage applied during ESD, EFT and surge tests can appear as voltage stress across the isolation barrier. The isolators used in the system must be capable of handling these high-voltage fast transients.

The current loop for a transient event on the interface pins in an isolated system is completed through the total isolation barrier capacitance. Through careful design, keeping the value of the isolation-barrier capacitance low, you can present significant impedance to the transient event and drastically cut down the peak current passing through transient protection devices, thus eliminating the need for high-power transient protection devices and reducing system cost. Isolation also reduces the duration for which the protection devices clamp the I/O pins by an order of magnitude. This reduces the width of error pulses in the communication channel during EMC tests, and enables systems to meet Criterion A much more easily when compared to non-isolated systems.

References

1. Thomas Kugelstadt, “Protecting RS-485 Interfaces Against Lethal Electrical Transients,” Texas Instruments application note (SLLA292A), March 2011.
2. Anant Kamath and Kannan Soundarapandian, “High-voltage reinforced isolation: Definitions and test methodologies,” Texas Instruments white paper (SLYY063), November 2014.
3. Sarangan Valavan, “Understanding electromagnetic compliance tests in digital isolators,” Texas Instruments white paper (SLYY064), November 2014.

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