High-Performance Analog Products

Analog Applications Journal

Fourth Quarter, 2011

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products	
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Management	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP™ Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications	
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E™ Community Home Page e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

SSZZ022B

Contents

To view past issues of the
***Analog Applications Journal*, visit the Web site**
www.ti.com/aaj

Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Audio
- Amplifiers: Op Amps
- Low-Power RF
- General Interest

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

How delta-sigma ADCs work, Part 2

By Bonnie Baker
Signal Integrity Engineer

A strong addition to the process-control design environment is the delta-sigma (ΔΣ) analog-to-digital converter (ADC). This device's claim to fame is its high 24-bit resolution, which provides 2^{24} or about 16 million output codes. Granted, not all of the lower bits are noise-free, but it is not unusual for a ΔΣ ADC to have 20 noise-free bits, or about 1 million noise-free output codes. This is at least four times better than the performance of 16-bit converters.

Figure 1 shows a block diagram of a ΔΣ ADC. As explained in Part 1 of this article series (see Reference 1), the modulator of a ΔΣ converter shapes the data in such a way as to allow high resolution by reducing low-frequency noise. Part 1 also pointed out that the undesirable characteristics of the modulator output are high-frequency noise and a high-speed, 1-bit output rate. Once the signal resides in the digital domain, a low-pass digital-filter function can be used to attenuate the high-frequency noise, and a decimator-filter function can be used to slow down the output-data rate. This article, Part 2, will consider each function independently, although real-world designs intertwine them in the same silicon.

The digital-filter function

The digital-filter function implements a low-pass filter by first sampling the modulator stream of the 1-bit code. Figure 2 shows a first-order, low-pass averaging filter. An averaging filter is the most common filter technique used in ΔΣ converters. As can be seen, the digital filter in Figure 2 is a weighted averaging filter. Almost all ΔΣ ADCs incorporate a class of averaging filters called sinc filters, named for their frequency response. Many ΔΣ devices, especially audio devices, use other filters in conjunction with sinc filters as part of a process called two-stage decimation. Low-speed industrial ΔΣ ADCs usually use only the sinc filter.

Figure 1. Block diagram of ΔΣ ADC

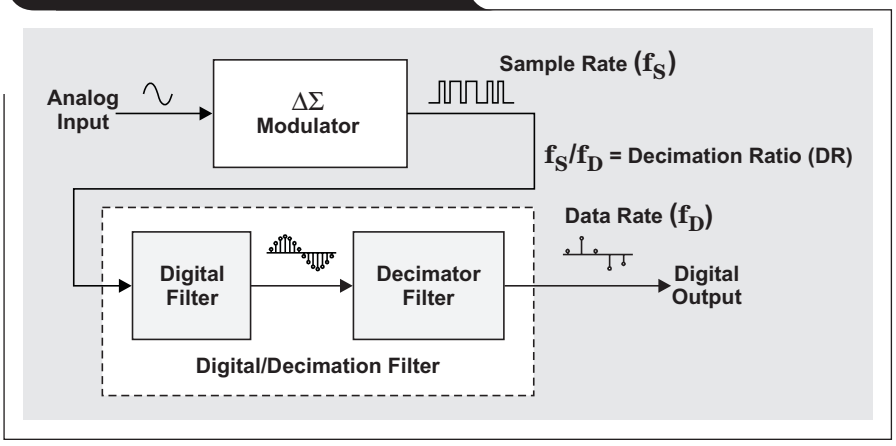
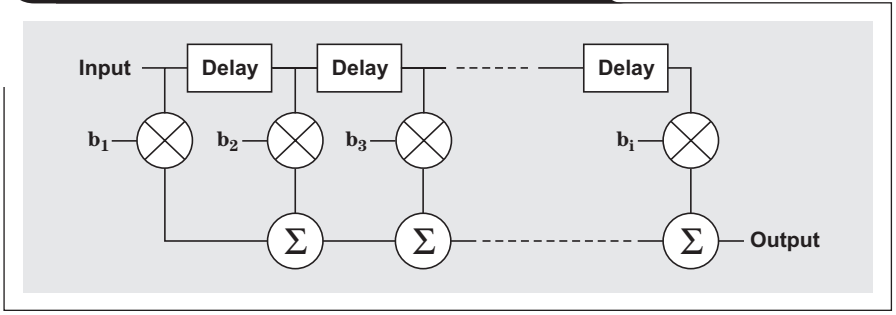
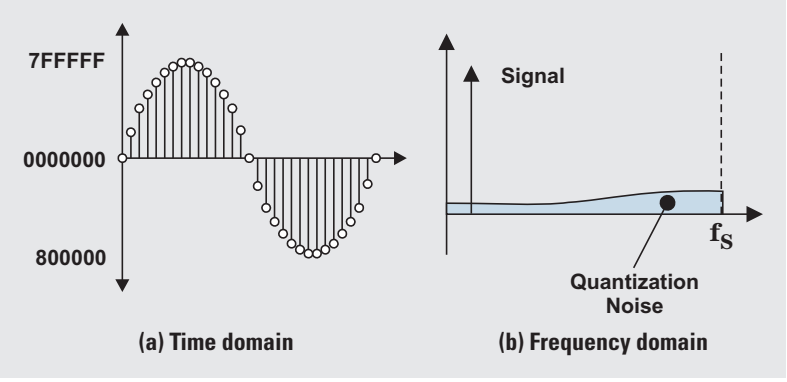


Figure 2. First-order, low-pass averaging filter



The output rate of a digital filter is the same as the sampling rate. Figure 3 shows a digital filter's outputs. In the time domain (Figure 3a), the digital filter is responsible for the high resolution of the ΔΣ converter. Notice that the 24-bit code train resembles the original signal. However, in the frequency domain (Figure 3b), the digital filter applies only a low-pass filter to the signal. In so doing, it attenuates the modulator's quantization noise; but it also reduces the frequency bandwidth, as any good low-pass filter will. With the quantization noise reduced, the signal re-emerges in the time domain.

Figure 3. Outputs of a digital filter



The signal is now a high-resolution, digital version of the input signal, but it is still too fast to be useful. The designer could have the converter deliver every one of the samples, but it would be pointless to do so because:

- This converter would require a very fast controller or processor.
- While it might appear that there is an abundance of high-quality samples at the high sampling rate of the modulator, most of them don't provide any useful information, since a low-pass filter has been applied. In other words, the extra samples are interpolations or intermediate results.

The decimator-filter function

The second function of the digital/decimation filter is the decimator. The word "decimate" was originally used by the Roman army to mean the killing of every tenth man of a group that was guilty of mutiny. In the case of the digital/decimation filter, the "decimation" of the digital filter's samples is much more dramatic. In the decimation circuit, the digital signal's output rate is reduced by throwing away or "killing" portions of the output data. The way to do this is to discard some of the samples.

This may seem a bit distressing. Previously, there was a beautiful sine wave that was well-defined with a large number of samples. Throwing away a large number of those samples leaves a skeleton of the original signal; but, remember, most of those samples are not "real." They can be thought of as the filter's work-in-process samples. In fact, according to the Nyquist theorem, the new "skeletal" version of the signal has exactly the same informational content as the previous waveform, but now it is at a manageable data rate. Decimating some of the samples has not caused any information to be lost.

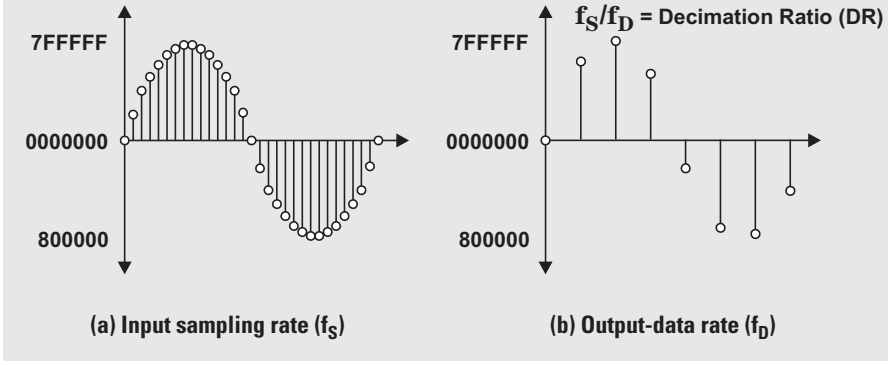
Figure 4 conceptually shows the decimation process. The digital filter's time-domain output in Figure 3a has been brought forward to Figure 4a. Figure 4b shows the decimator-filter function's output signal.

This completes the description of the digital-filter and decimator-filter functions in a ΔΣ converter.

Pulling the ΔΣ ADC together

Part 1 of this series showed the inner workings of the modulator in the time and frequency domains. It also showed how the modulator shaped noise into higher

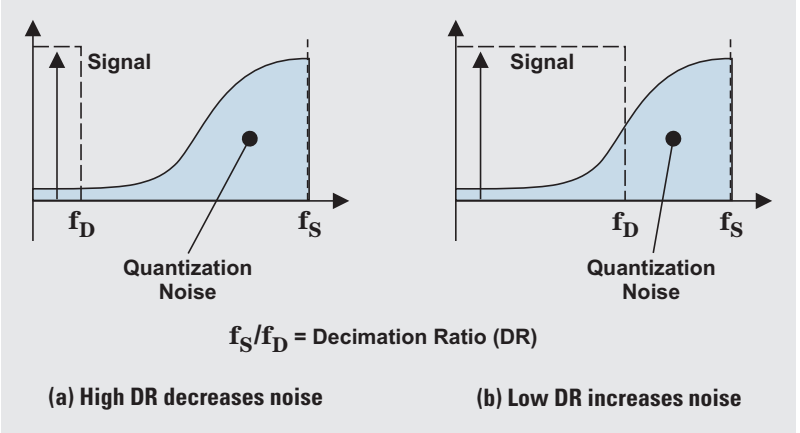
Figure 4. Digital/decimation filter's output from decimation process



frequencies because of an oversampling system with negative feedback. As previously stated in the present article, the digital/decimation filter reduces high-frequency noise and passes the input signal to the output of the converter at a reduced data rate. The combination of these two components provides a high-resolution ADC.

The meaningful variables in this system are the modulator's sampling rate ($\mathbf{f_S}$) and the digital/decimation filter's output-data rate ($\mathbf{f_D}$). The ratio between these two variables is defined as the decimation ratio (DR). The decimation ratio is equal to the number of modulator samples per data output. Decimation ratio values range anywhere from 4 in the Texas Instruments (TI) ADS1605 ADC to a maximum of 32,768 for TI's ADS1256 ADC.

Figure 5. Increased DR provides a lower-noise, slower output signal



Consider the output spectrum of the ΔΣ modulator in Figure 5. The modulator samples at a frequency of $\mathbf{f_S}$ and, in doing so, shapes the quantization noise into higher frequencies. Many ΔΣ converters permit the designer to program the data rate directly by adjusting the decimation ratio. Suppose the data rate is chosen to be some fraction of $\mathbf{f_S}$, as shown in Figure 5a. The frequencies from 0 to $\mathbf{f_D}$, which constitute the output, are in the signal band. Note the noise level in the signal band.

In Figure 5a, the effective number of bits (ENOB) is very high. Since the output-data rate ($\mathbf{f_D}$) is determined by the decimator-filter function, it depends on the decimation ratio (DR), where $\mathbf{DR = f_S/f_D}$. Figure 5b shows that the value for $\mathbf{f_D}$, which has moved to the right, is now higher. Unfortunately, there is also more noise. Most of the noise is in the higher frequencies, decreasing the signal-to-noise ratio and the ENOB.

There is a way to increase the sampling speed ($\mathbf{f_S}$) while keeping the ENOB the same, and that is to increase the master-clock rate. This will also increase $\mathbf{f_D}$ but will not decrease the decimation ratio. Unfortunately, increasing the master-clock rate will also increase power consumption. Additionally, most converters have a practical limit for $\mathbf{f_S}$ beyond which they will not function properly.

Conclusion

A ΔΣ ADC fundamentally includes a modulator and a digital/decimation filter. The modulator converts the analog signal directly into the digital domain by using a 1-bit ADC and oversampling. The modulator topology implements a noise-shaping function that drives the lower-frequency quantization noise into higher frequencies. The low-pass digital/decimation filter throws away the high-frequency noise that was shaped by the modulator stage and reduces the data-output rate of the device to a usable frequency.

There is a strong relationship between the output-data rate and the converter's resolution. If the sample rate is kept constant, lower data rates provide high effective resolution, or ENOB, at the output of the converter.

ΔΣ ADCs have other functions besides the basics in these two articles, acting as current sources, voltage sources, input buffers, etc. However, examining any ΔΣ ADC will always reveal a modulator and a digital/decimation filter. In choosing a ΔΣ ADC, it is best to start with the fundamentals and then see what else the device has to offer.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Bonnie Baker, "How delta-sigma ADCs work, Part 1," *Analog Applications Journal* (3Q 2011)	SLYT423
2. "16-bit, 5MSPS analog-to-digital converter," ADS1605/6 Datasheet	SBAS274
3. "Very low noise, 24-bit analog-to-digital converter," ADS1255/6 Datasheet	SBAS288

Related Web sites

dataconverter.ti.com
www.ti.com/product/ADS1256
www.ti.com/product/ADS1605

Solar charging solution provides narrow-voltage DC/DC system bus for multicell-battery applications

By Wang Li, *Battery Power Applications Engineer,*
and Michael Day, *Power Applications Manager*

Introduction

Solar-powered systems typically must operate from a very wide input-voltage range due to the large variations in a solar panel's output voltage. This wide operating range limits the system's ability to consume maximum power from the solar cell under all light conditions. The ideal solar charging application operates the solar cell at its maximum power point (MPP) while simultaneously limiting the input-voltage range of the system. This goal is achieved by integrating a narrow-voltage DC/DC (NVDC) battery-charging architecture with a solar-charger design. The narrow voltage range for the system power bus provides higher system efficiency, minimizing battery charging times and extending battery run times.[1] This article shows the NVDC charging architecture in a solar charging application and introduces a circuit that provides acceptable charger operation under several operating conditions, such as battery overtemperature, a discharged battery, a fully charged battery, and a system-current overload.

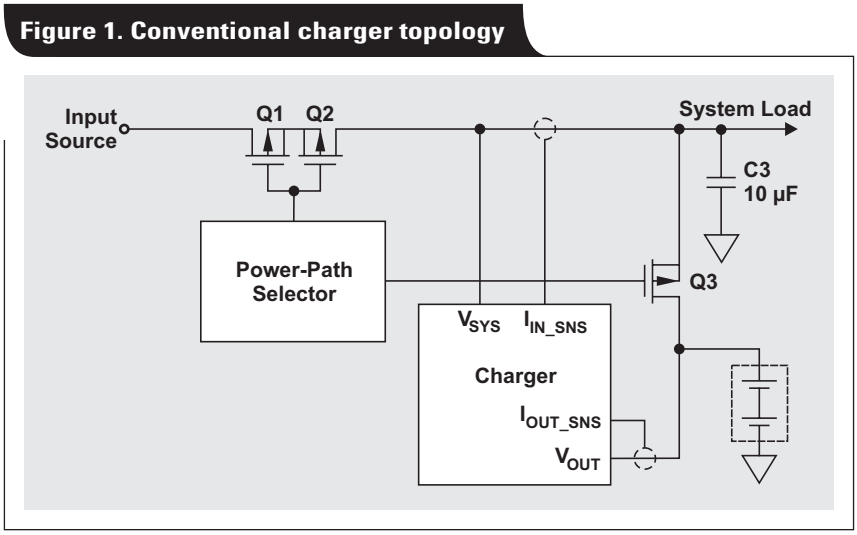
Conventional charger topology

Figure 1 shows a conventional charger topology used with high-power switching chargers. Notebook charging is a typical application for this topology. One drawback is the system's wide operating voltage range, which requires more expensive, less efficient power supplies to generate the power rails for the downstream circuitry.[1] The system voltage ranges from the highest AC adapter voltage (typically 22 V for a lightly loaded adapter) to the lowest battery voltage, which is 9 V for a 3S2P laptop battery pack. (3S2P is an abbreviation for three batteries in series with two of these series connections in parallel.) When the AC adapter is present, the power-path-selector MOSFETs (Q1 and Q2) turn on, and the battery MOSFET (Q3) turns off. The AC adapter voltage is applied to both the system voltage and the battery charger's input, delivering power to both circuits simultaneously. If the AC adapter voltage drops due to a brownout, an overcurrent condition, or unplugging the adapter, Q1 and Q2 turn off to prevent battery power from flowing backwards into the adapter. Q3 turns on and connects the battery-pack voltage directly to the system. In this way, the system is always supplied with power—either from the adapter or the battery.

Requirements of a solar-powered charger

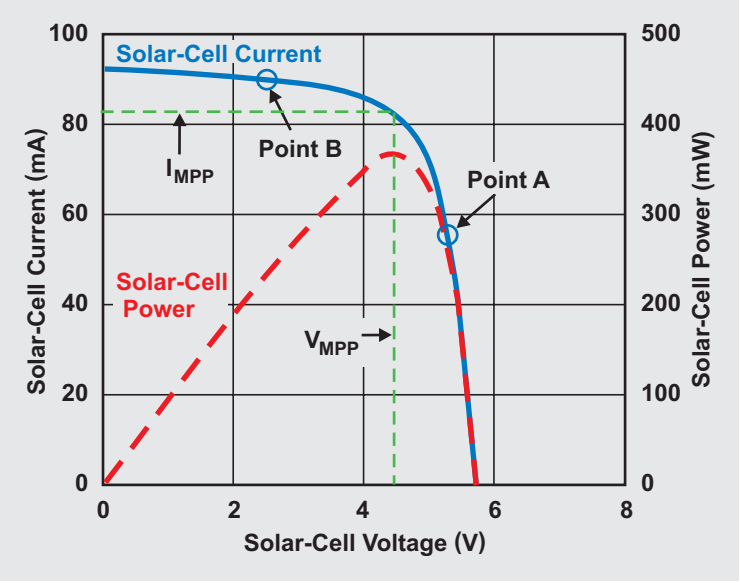
The battery-charger architecture in Figure 1 is acceptable for systems that use an AC adapter, but it is not ideal for solar charging applications because there is no way to limit the input current. To keep the solar cell always operating at its MPP, which will minimize battery charge time and the solar cell's size and cost, the charger needs a current-limiting mechanism. Unlike a conventional AC wall adapter,

Figure 1. Conventional charger topology



a solar cell should be operated with very tight control over its load current. Figure 2 shows the V-I characteristics of a typical solar cell under one light condition and helps explain this concept. The solid line represents the output current of the solar panel as its voltage varies, while the dashed line represents the output power. Because the panel's voltage drops as the current it delivers increases, an MPP is created at a specific voltage and current. A solar cell's MPP varies with different light conditions and temperatures. If very little charging and system current are required, the solar cell may operate at Point A in Figure 2, which is below its MPP. The solar cell delivers less than its maximum power, which is acceptable because the system is getting the power it needs. However, if the battery charge current or system power requirements increase, the charger pulls more current and the solar cell operates at Point B in Figure 2. At Point B, the solar cell's output current has increased, but the actual delivered power has gone down because of the drop in voltage. With reduced power from the solar cell, it takes longer to charge the battery. A well-designed solar-cell charger should contain circuitry that separates the solar cell from the system as well as circuitry that controls the solar cell's total current so the cell can be operated at its MPP. This combination of circuitry can fully utilize the solar cell's available power, resulting in a less expensive system because the designer does not have to oversize the solar cell to meet charging requirements.

Figure 2. Solar panel's V-I curve and output-power curve



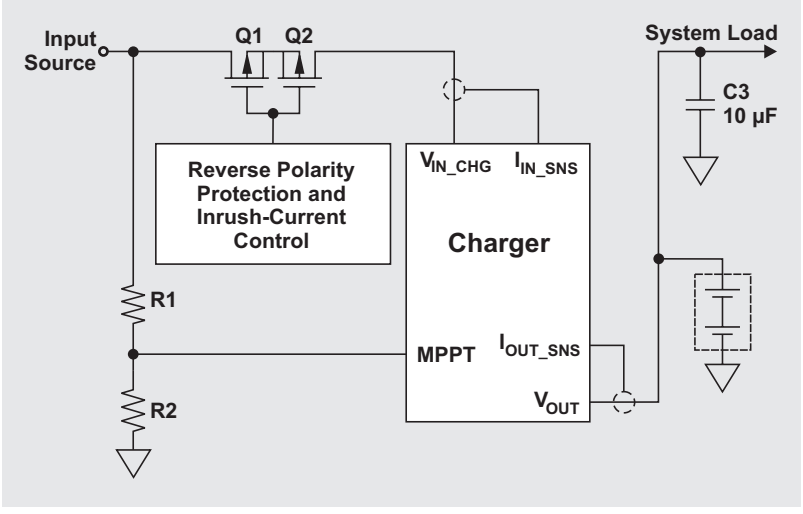
Basics of maximum-power-point tracking

Solar-cell chargers include special circuitry called maximum-power-point tracking (MPPT) circuitry that prevents the charger from consuming more than the solar cell's maximum power. This is typically implemented by setting the minimum operating voltage that corresponds with the solar cell's MPP. A design using the solar cell in Figure 2 allows the charger and system to draw any current from the solar cell as long as the solar cell's voltage remains above V_{MPP}. When the current increases to the point where the voltage drops to V_{MPP}, a special control loop in the charger takes over and regulates the total current from the solar cell to maintain the solar cell's voltage at V_{MPP}. At this operating point, the solar cell delivers its maximum power. Any power not required for the system load is used to charge the battery. This voltage-based MPPT circuitry is fairly accurate at providing maximum power, even with varying solar-cell illumination levels. Although reduced light lowers the solar cell's maximum power and current capability, the MPP is still achieved at approximately the same voltage.[2] Voltage-based MPPT circuitry typically consists of only two resistors external to the battery charger.[3] All other circuitry is integrated into the charger IC itself. A solar cell's V_{MPP} does vary significantly with temperature. If desired, additional circuitry can be added to track a solar cell's V_{MPP} change with temperature. Tracking MPP over temperature can reduce charging times by 40%.[4]

Adding NVDC charging architecture

Figure 3 shows how a narrow-voltage DC/DC (NVDC) charging architecture can separate the solar cell from the system. Rather than being connected to the solar cell via

Figure 3. NVDC architecture with MPPT circuitry



the power-path-selector FETs, the system is connected directly to the battery. The system voltage is now equal to the battery voltage, regardless of the input voltage of the adapter or solar cell. The narrow operating voltage allows the designer to optimize the system power supplies for size, cost, and efficiency.[1] It also eliminates the need for the battery FET. The NVDC architecture is useful for solar charging because it routes all current through the charger. This allows the MPPT circuitry to effectively control the total current from the solar cell and maintain operation at the maximum rated power.

Connecting the system directly to the battery as in Figure 3 has significant advantages, but it also has disadvantages under certain operating conditions that should be considered. These conditions are as follows:

1. When the battery voltage is lower than the battery's precharge voltage, the battery current must be limited to the precharge current, which may not be sufficient to operate the system.
2. When the battery temperature is outside the allowable range for charging, the charger must disable charging, which also disables the system's power.
3. When the battery is fully charged, it should be disconnected from the charging source to extend battery life, but the system should remain on.

All of these conditions can be addressed with the addition of FETs Q4 and Q5 to the NVDC architecture (see Figure 4). A gas gauge or a host controller monitors voltages, current, and battery temperature and uses these inputs to control the FETs, which connect or disconnect the battery to or from the charger depending on the operating conditions. The host can be as complicated as a microprocessor with analog-to-digital converters that continuously monitors operating conditions and adjusts charger performance based on the system's needs, or it can be simple, discrete circuitry that monitors only battery voltage and temperature.

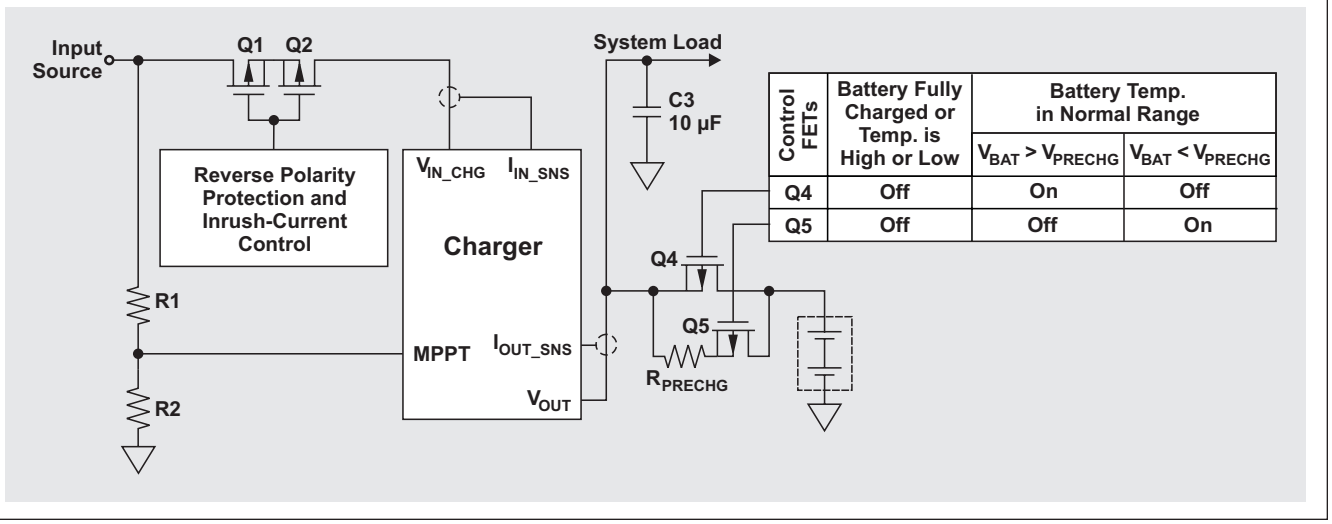
A deeply discharged battery requires preconditioning prior to being charged. Typical Lithium-Ion (Li-Ion) batteries require the charger to apply a precharge current that is 1/10 of the fast-charge current until the battery voltage rises above a specific voltage, typically 3 V/cell. When the host detects a battery voltage that is less than the specified precharge voltage ($V_{BAT} < V_{PRECHG}$), it turns Q5 on and provides a precharge current through R_{PRECHG}. The value of R_{PRECHG} is chosen to provide the maximum allowable precharge current when the battery voltage is fully discharged. In this operating mode, the system is effectively isolated from the battery voltage, which allows the charger to maintain the NVDC regulation voltage even with a discharged battery. When the battery voltage increases above the precharge voltage, the host turns Q5 off and Q4 on, effectively shorting the battery and the system together. The battery's charge current increases to the charger's maximum output current minus the current into the system. If the system current exceeds the charger's fast-charge current, the battery enters supplement mode where current flows out of the battery to the system.

If the host detects an over- or undertemperature fault condition, it turns off both Q4 and Q5. This stops the battery charging while still allowing the charger to power the system. The host can also turn Q4 and Q5 off when the battery reaches its full-charge voltage to increase battery life. Detailed information on the battery-disconnect circuitry can be found in Reference 5.

Conclusion

The NVDC charger architecture coupled with MPPT and the battery-disconnect circuitry provides several advantages over standard charging architectures. It intelligently connects and disconnects the battery from the system

Figure 4. NVDC architecture with battery-disconnect circuitry



Control FETs	Battery Fully Charged or Temp. is High or Low	Battery Temp. in Normal Range	
		$V_{BAT} > V_{PRECHG}$	$V_{BAT} < V_{PRECHG}$
Q4	Off	On	Off
Q5	Off	Off	On

under the appropriate operating conditions, allowing the designer to optimize the solar panel's output power for the system's needs. The charger also provides a narrow system operating voltage, which optimizes efficiency and extends battery life.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Xiaoguo Liang, Gnanavel Jayakanthan, and Meng Wang, "Design considerations for narrow Vdc based power delivery architecture in mobile computing systems," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, 2010, pp. 794–800 [Online]. Available: http://ieeexplore.ieee.org	—
2. Lokesh Ghulyani, "Simple MPPT-based lead acid charger using bq2031," Application Report	SLVA378
3. "Synchronous switch-mode battery charge controller for solar power with maximum power point tracking," bq24650 Datasheet	SLUSA75
4. Jared Casey, "Maximum power point tracking with the bq24650 charger," Application Report	SLUA586
5. Wang Li, "A discrete narrow voltage DC/DC (NVDC) charger solution for multi-cell batteries," Application Report	SLUA620

Related Web sites

power.ti.com
www.ti.com/product/bq2031
www.ti.com/product/bq24650

Solar lantern with dimming achieves 92% efficiency

By Chris Glaser
Applications Engineer

Solar lanterns are becoming increasingly popular, especially for decorative nighttime lighting or in areas with unreliable or nonexistent electrical service. These lanterns charge a battery during the day and then use that stored energy during the night to provide light on outdoor paths and sidewalks, or for indoor activities such as cooking or reading. Since the lanterns typically are powered by low-cost and robust multicell lead-acid batteries, a common problem encountered is how to efficiently convert this chemical energy to lumens (visible light output). To solve this, LEDs are frequently used because they produce many lumens per watt of energy consumed. A switching regulator is usually employed to efficiently convert the variable battery voltage to a regulated yet changeable (dimmable) current in the LED, which creates light. Efficiency must remain high over the battery voltage and dimming range in order to prolong battery life. A complete, cost-effective solution is needed to efficiently convert the 6, 9, 12, or 15 V of a common lead-acid battery pack to light with dimming capabilities.

Single LED versus an LED string

When designing a solar-lantern system, designers must choose whether to produce the desired amount of light with multiple smaller, lower-power LEDs or one larger, high-brightness LED. Typically, a single LED driver drives a string of smaller LEDs in a series configuration. The advantages of this approach are that the current in each LED is exactly the same and the LEDs can be positioned to illuminate a wider area than is possible with a single LED. However, even with equal currents, the LEDs cannot each emit exactly the same color of light unless they are tested and binned before assembly. This is more costly.

A single high-brightness LED emits light to a smaller area, but this can be overcome by a diffuser cover placed over the LED. When pick-and-place costs in assembly are considered, a single high-brightness LED is usually more cost-effective overall than several smaller LEDs. A single LED does not need to be binned, which also reduces costs. This article discusses use of the low-cost, single high-brightness LED. The LED current is set to 800 mA for a dimmable 2.8-W power output, which is typical for solar lanterns.

Easily dimmable

The light output of the solar lantern must be adjustable according to the needs of the user. For instance, more light might be required for reading than for cooking. Dimming the light output draws less energy from the battery and results in a longer battery run time.

Analog dimming and pulse-width-modulator (PWM) dimming are two methods that can be implemented to reduce the LED's light output. Analog dimming reduces the average current in the LED, while PWM dimming operates the LED at full current but varies the duty cycle at which this full current is applied. Thus, PWM dimming creates an average LED current equivalent to the full current multiplied by the duty cycle of the applied PWM signal. The PWM dimming frequency should be above the bandwidth detectable by the human eye so that the viewer does not notice any flicker. In general, analog dimming is more efficient, but PWM dimming eliminates the LED color shift that occurs when the LED is driven at different currents (as in analog dimming). So, the LED light color remains the same across the dimming range. Since both dimming methods have advantages and disadvantages, the ideal solar-lantern LED driver should accommodate both dimming methods. A PWM signal from a microcontroller, which typically is present in the solar-lantern system for battery management and other tasks, should be the single dimming interface with the LED driver for both methods. The Texas Instruments TPS62150 supports analog and PWM dimming from a PWM signal, as shown in Figures 1 and 2 (see next page). Detailed design equations are found in References 1 and 2.

The advantage of these circuits is their similarity. Only small schematic changes and a change to the PWM signal's frequency are needed to implement analog or PWM dimming in a given design. This means that the same LED driver circuit can be used for multiple solar-lantern designs. Simply populate the circuit with different components and load a slightly different code to the microcontroller, and the solar lantern is optimized for either highest efficiency or most constant light color through the use of either analog or PWM dimming.

Another major concern is the dimming linearity. Does the rate of change in the LED current (and thus the light output) across the dimming range correspond to the rate of change of the input signal (in this case, the duty cycle of the PWM signal)? If this is true for the given LED driver, then the code development is quite simple, as a 10% increase in duty cycle results in a 10% increase in light output. If this were not true, then additional testing and code would be needed to correlate a given change in the input signal to the desired change in light output. This

Figure 1. Circuit schematic for analog dimming

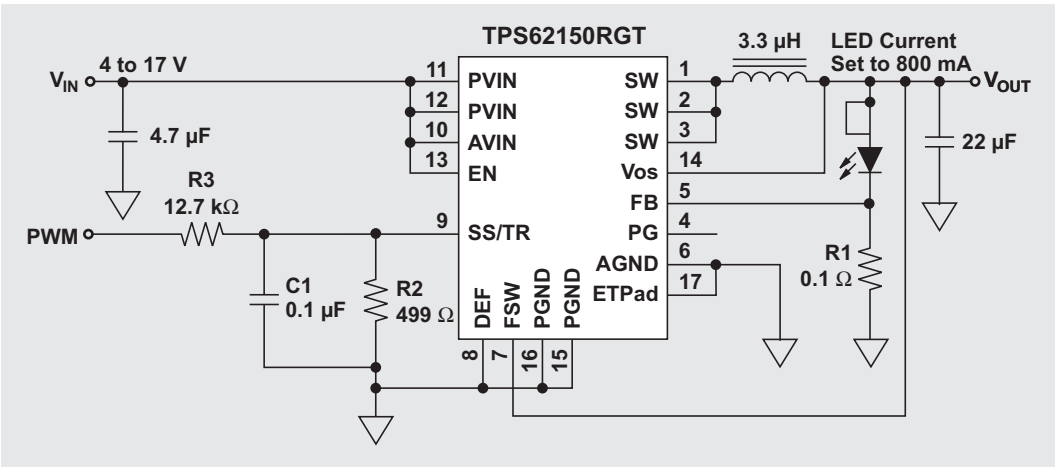
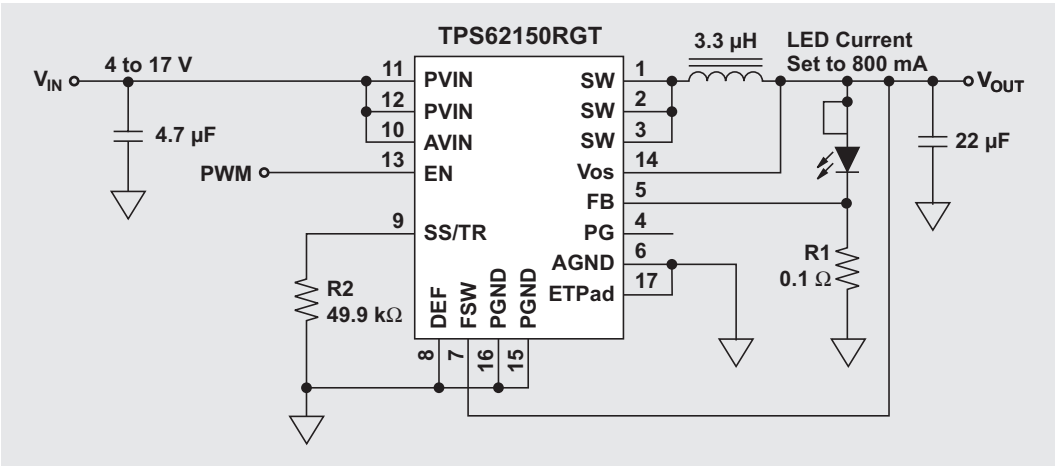


Figure 2. Circuit schematic for PWM dimming



correlation might also vary across the dimming range, resulting in further complications to the dimming algorithm. Fortunately, the circuits in Figures 1 and 2 support very high dimming linearity, as shown in Figures 3 and 4. Each circuit has a coefficient of determination (R^2 value) of 1, which indicates perfect linearity. (The R^2 value is a statistical measure of the variability in a data set, and a value of 1 indicates zero variability.) This results in a very simple code development for the dimming algorithm and provides a pleasant user experience in the smooth dimming behavior of the lantern.

However, for analog dimming, the linear equations modeling this linearity have a y-axis intercept of 94 mA. This shows another limitation of analog dimming—an inability to dim the LED at very low output currents. To solve this, PWM dimming is used, with a y-axis intercept of –7 mA. This allows very low LED currents to be achieved at very low PWM duty cycles.

Achieving high efficiency

Efficiency is critical in any battery-powered system, but especially in a solar lantern. Since it cannot be assumed that every day will have sunlight, the batteries have to last for more than one day at a time without a recharge. By an efficient conversion of stored chemical energy to light and a reduction of the light output through dimming, the LED driver increases the battery run time. In addition to supporting dimming, an efficient LED driver should (1) operate at a relatively low switching frequency to reduce the switching losses, (2) have a power-save mode to boost the efficiency at low light levels, and (3) have a cost-effective method to reduce the losses in the current-sensing resistor, R1 in Figure 1. The TPS62150 is a good choice because it has these three features and produces the efficiency

Figure 3. Analog dimming linearity

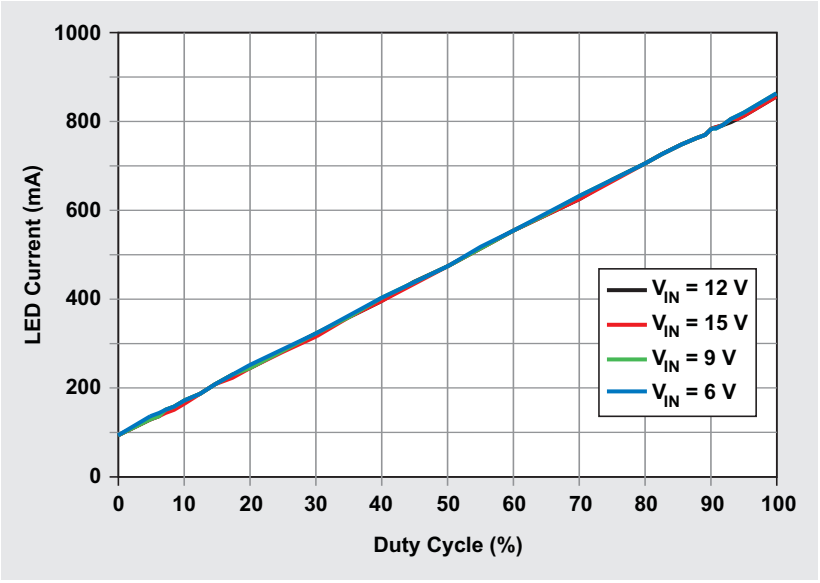
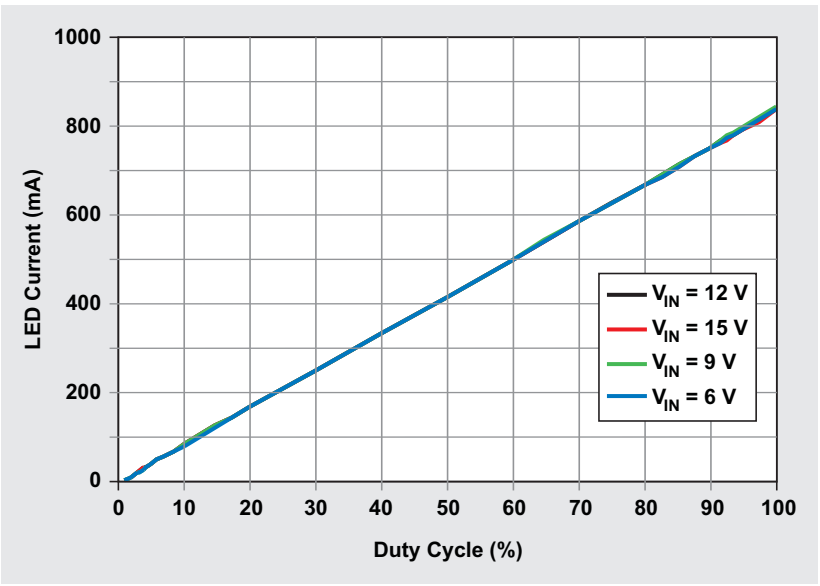


Figure 4. PWM dimming linearity

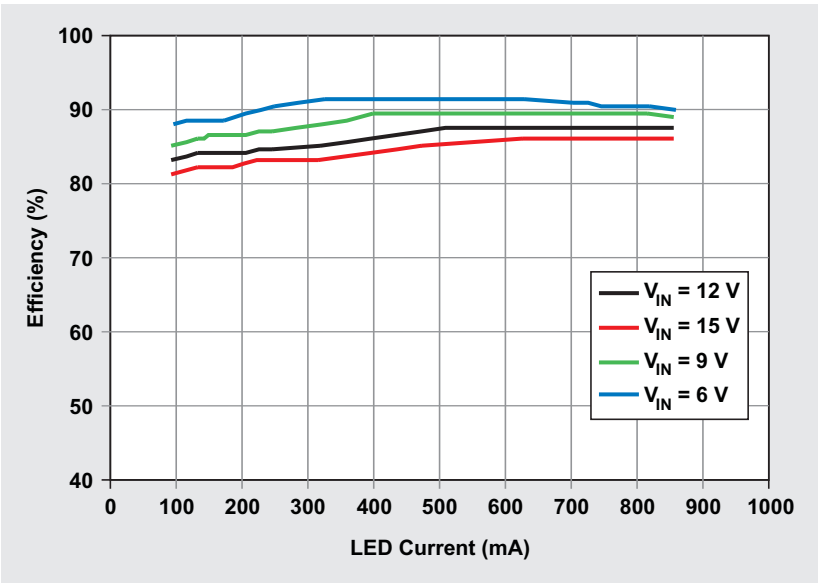


shown in Figures 5 and 6. Due to a higher voltage drop when the LED is driven at its full current, and due to reduced efficiency during the turn-on and turn-off of the IC, the efficiency of PWM dimming is lower than that of analog dimming.

Conclusion

This article has presented an efficient 2.8-W solar-lantern solution that drives a single high-brightness LED and provides either analog or PWM dimming from a PWM signal. Analog dimming achieves better efficiency over the entire dimming range, while PWM dimming allows very low LED currents (for very low light levels) at low PWM duty cycles and has the best efficiency at full output power. Both dimming circuits are extremely linear. This design is well-suited for solar lanterns powered from rechargeable lead-acid, nickel, or lithium batteries.

Figure 5. Analog dimming efficiency



References

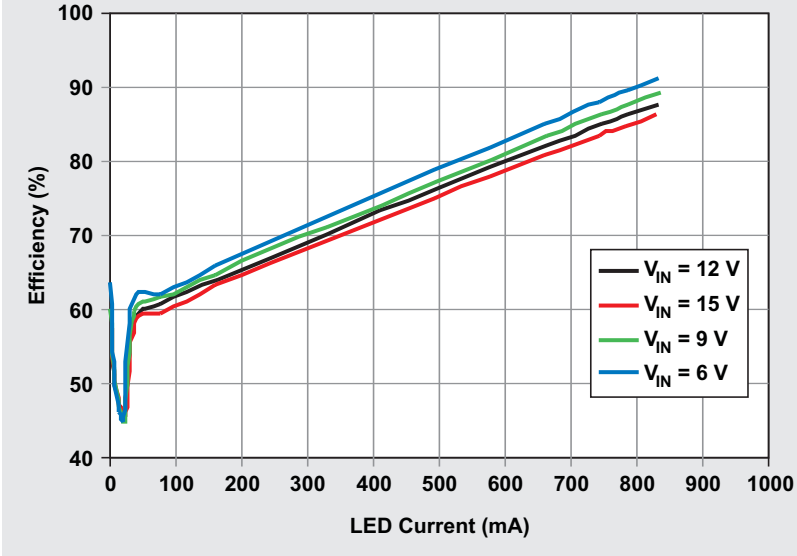
For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "Using the TPS62150 as step-down LED driver with dimming"	SLVA451
2. "Design tool for analog dimming using a PWM signal"	SLVC366
3. "3-17V 1A step-down converter in 3×3 QFN package," TPS62150/1/2/3 Datasheet	SLVSAL5

Related Web sites

power.ti.com
www.ti.com/product/TPS62150

Figure 6. PWM dimming efficiency



Extending the SPI bus for long-distance communication

By Thomas Kugelstadt
Senior Applications Engineer

The serial peripheral interface (SPI) bus is an unbalanced or single-ended serial interface designed for short-distance communication between integrated circuits. Typically, a master device exchanges data with one or multiple slave devices. The data exchange is full-duplex and requires synchronization to an interface clock signal. However, recent trends in the design of industrial data-acquisition systems have not taken this synchronization requirement into account, and distances between the microcontroller and the corresponding analog-to-digital and digital-to-analog converters (ADCs and DACs) can reach 100 m or more.

The impact of the added propagation delay on the data-to-clock synchronicity is often ignored, and interface designs that operate perfectly in the lab environment cease operation when implemented on the factory floor. There can be multiple reasons for the interface malfunction. This article tries to shed light on the major ones, including:

- Lack of synchronization due to large propagation delays of the signal path
- Reduced noise immunity due to long-distance, unbalanced signal paths
- Damaged transceivers due to large ground-potential differences (GPDs)
- Data transmission errors due to unterminated data lines
- Transceiver latch-up and network downtime due to large electrical transients

Synchronicity

An SPI primarily uses three interface lines:

- An interface clock initiated by the master device to ensure synchronous data transfers
- A data line for data sent from the master to a slave
- A data line for data sent from a slave to the master

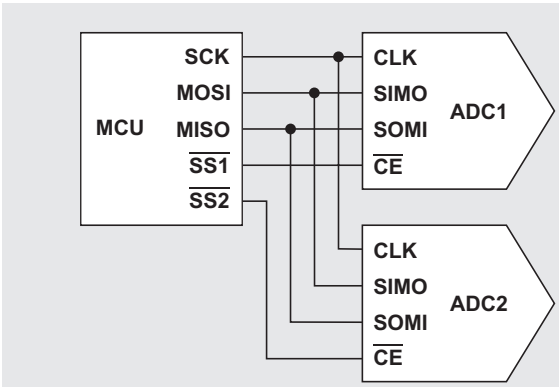
A fourth wire that carries what is known as the slave-select signal is not required for controlling interface flow but is needed for addressing a specific slave out of a range of slave devices. Figure 1a shows a simplified schematic of a microcontroller unit (MCU) operating as the master that controls two data converters representing the slaves.

With byte lengths ranging from 8 to 12 bits and multiples thereof, and data rates ranging from 1 to 20 Mbps, the standard SPI configuration allows for short propagation times and hence only short distances in order to maintain synchronicity between the interface clock and the data transmitted in both directions. Figure 1b shows the interface timing of the first three data bits when the SPI is configured to change data at the rising clock edge and to sample data at the falling clock edge.

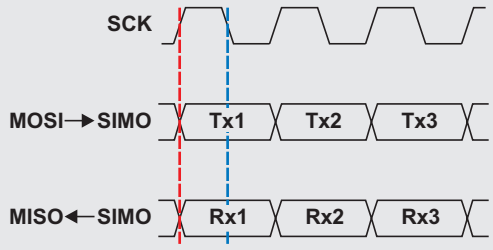
Over long distances, however, the transmission cable introduces significant propagation delay into the signal path. Assuming a typical signal velocity of 5 ns/m, a 100-m cable will cause a propagation delay of 500 ns. Because the data sent from the master to the slave experiences the same delay as the master-initiated interface clock, both will remain in sync across the entire data link. In the opposite direction, however, the slave sends data to the master only when the first clock edge reaches the slave. Furthermore, this data will experience a second delay on its way back to the master, so the slave data will be out of sync by twice the cable's propagation delay.

Of course, communicating across a 100-m cable won't be possible without appropriate line drivers and receivers. These components will further increase the propagation delay by about another 50 ns, for a total of 550 ns. The slave data will therefore lag behind the first clock edge by a total of 1100 ns, or 11 bits when a data rate of 10 Mbps is assumed.

Figure 1. Simplified schematic of an SPI



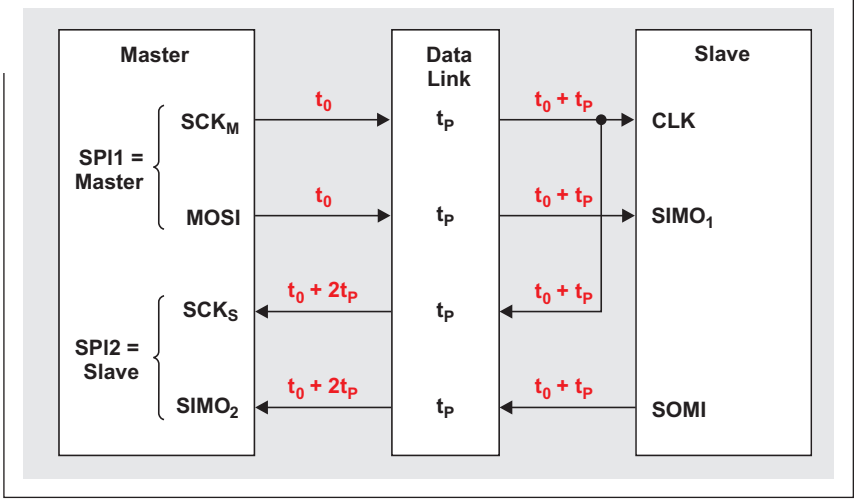
(a) MCU master controlling two slaves



(b) Timing of first three data bits

The only possible solution for restoring synchronicity between the slave data and the interface clock while maintaining a high data rate is to feed the clock signal from the slave back to the master. Figure 2 clarifies the benefit of clock feedback. Here t_0 represents the first rising clock edge, or the start of a data transmission, and t_P is the data-link propagation delay. After traversing the data link, both the master clock (SCK_M) and the master data (MOSI) remain in sync. Feeding back the master clock signal synchronizes the clock with the slave data so that both arrive equally delayed at the master. The only requirement is that the master provide two independent SPI ports, one configured as a master (SPI1) and the other configured as a slave (SPI2). Most modern microcontrollers possess two or more SPI ports, so this requirement poses no problem.

Figure 2. Clock-feedback path restores synchronicity



Nevertheless, implementing a long-distance, SPI-compatible interface in the real world is not a trivial task. Long-distance data links are always subject to external noise sources, ground-potential differences (GPDs), voltage and current surges due to inductive load switching, and often even reflections due to wrong or no termination. The flowing schematic in Figure 3 (see next page) tries to cover all of these aspects by showcasing the various transceiver and protection circuits that can counteract the derogating effects.

Increasing noise immunity

Unbalanced or single-ended drivers and receivers are inadequate for accomplishing a robust data link over long distances, as they are susceptible to common-mode noise. An excellent method to eliminate common-mode noise in a synchronous, full-duplex interface such as an SPI is the use of RS-422 differential driver and receiver circuits in combination with twisted-pair cable.

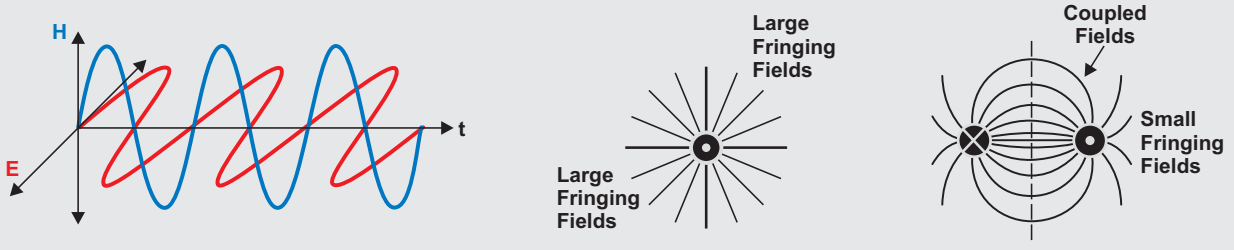
Because the conductors of twisted-pair cable are closely electrically coupled, external noise induced equally into both conductors appears as common-mode noise at the receiver input. Although differential receivers are sensitive to signal differences, they are immune to common-mode signals. The receiver therefore rejects common-mode noise, and signal integrity is maintained.

Another benefit of close electric coupling is that the currents in the two conductors create magnetic fields that cancel each other. The initial transversal electromagnetic (TEM) waves of the two conductors are therefore largely reduced to electric fields that cannot radiate into the environment (see Figure 4). Only the far smaller fringing fields outside the conductor loop can radiate, thus yielding much lower electromagnetic interference (EMI).

Eliminating ground loops and GPDs

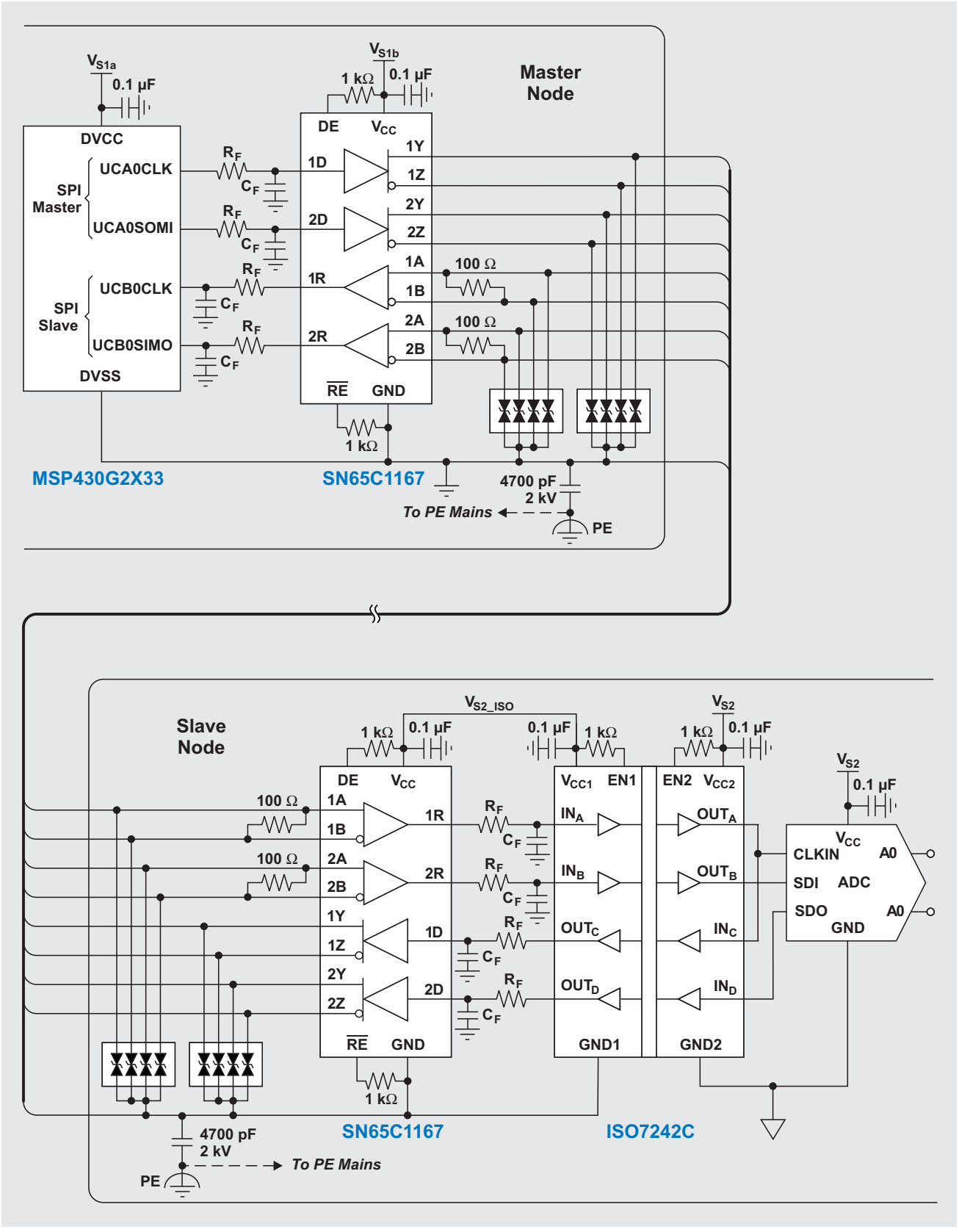
While the RS-485 and RS-422 standards specify that a data link without a ground wire can be operated with a GPD of up to ±7 V, it is advisable not to assume that these values

Figure 4. TEM-wave radiation effects



(a) Relationship of magnetic and electric fields (b) Single conductor (c) Closely coupled conductor pair

Figure 3. SPI extended via RS-422 data link



represent the maximum GPD. Much higher values are often encountered in industrial plants, sometimes reaching several hundreds and even thousands of volts. Because GPDs largely depend on factors outside the system designer's control, such as the electric installation and/or the number of electric motors and generators, the most secure way to prevent transceiver damage from large ground-potential variations is to galvanically isolate any remote network node from the bus. The circuit in Figure 3 demonstrates this by having only the remote transceiver connected to the bus, while the data-converter circuit is galvanically isolated.

Also, to provide the input and output signals of the remote transceiver with a stable ground reference, the transceiver's ground terminal as well as the digital isolator's ground terminal (GND1) are connected to the master ground potential via a separate ground conductor. This form of grounding is known as a single ground reference.

Avoiding antennas through line termination

The data link in Figure 3 is terminated with 100-Ω resistors, as suggested by the RS-422 standard, matching the characteristic impedance of the bus cable. A myth exists that bus cables of a few meters in length or data links operating at low data rates don't need termination. Don't believe it. Operating the bus without termination can turn the transmission line into a nasty receiver/transmitter antenna. The lack of termination resistors, which usually absorb the incident wave power sent by the driver, causes standing waves to occur; and the entire incident wave is reflected into the bus. The reflected waves mix with other incident waves, thus yielding standing waves for signal frequencies whose quarter wavelengths, or multiples thereof, equal the length of the data link.

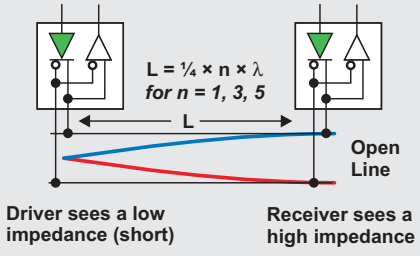
Depending on their location, the wave nodes (minima) and antinodes (maxima) can have varying effects on the bus transceivers (see Figure 5). A driver close to an antinode sees a high impedance and therefore transfers insufficient energy to the bus. A driver close to a node sees a very low impedance or a short. The resulting output current can exceed the driver's maximum drive capability and even trigger its current limit at around 250 mA. Receivers located at antinodes can be damaged by excessively large input signals that exceed the receiver's common-mode input range. Receivers close to nodes experience insufficient signal strength and are highly susceptible to noise and EMI. Any of the foregoing events will result in data errors from either the transmission or the reception of wrong data.

Protecting the network against damaging transients

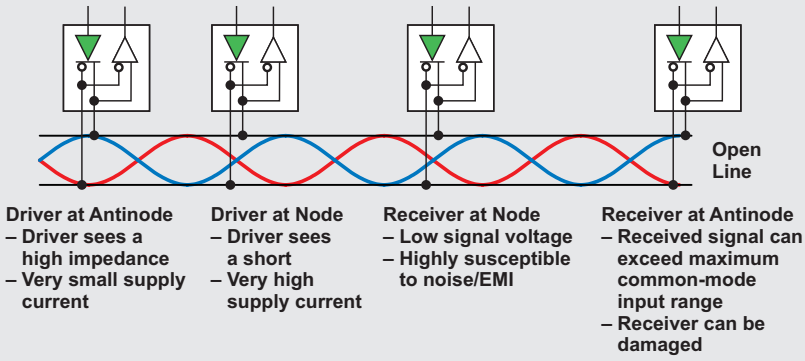
Electrical overstress transients caused by electrostatic discharge (ESD), switching of inductive loads, or lightning strikes will corrupt data transmission and damage bus transceivers unless effective measures are taken to diminish their impact. Modern transient-voltage suppressors, such as the ones in Figure 3, are the preferred protection components for high-speed data transmission due to their low capacitance, which allows them to be designed into every node of a multinode network without requiring a reduction in data rate.

Depending on the power rating of the transient-voltage suppressor chosen, the maximum clamp voltages can range from 25 to 35 V, which is higher than a standard transceiver's maximum bus voltage of 14 V. In this case, the internal protection circuit of the transceiver must

Figure 5. Effects of an unterminated bus



(a) Effects with a quarter-wave line length



(b) Effects of connecting drivers and receivers at nodes and antinodes

absorb the remaining clamp energy to protect the device from damage.

For ESD and burst transients, the clamp energy is rather low due to the short pulse duration and does not pose a problem to the internal ESD cells. Clamp energy from surge transients, however, can present a serious challenge due to the much longer pulse duration. For transceivers specified with low ESD immunity, series resistors might be necessary to reduce the remaining current flowing into the transceiver. Common resistor values range from 5 to 10 Ω. Note that these resistors must be surge-rated to provide high pulse robustness.

Although the transient-voltage suppressor's diodes divert large transient currents to ground, it must be ensured that these currents are further diverted to true earth potential without disturbing the ground reference of the remaining circuitry. Often this is accomplished by implementing a high-voltage capacitor that has one plate connected to ground and the other plate connected to a protective-earth (PE) island. This island is then connected via a short, low-inductance earthing wire to the PE terminal of the local mains supply.

In addition to the suppressor's action on the bus side, further protection against signal degradation is required on the transceiver's single-ended sides. This is accomplished with R-C low-pass filters, which filter transient remnants in the reception path and stop high-frequency noise from entering the transmission path.

Related Web sites

interface.ti.com
www.ti.com/product/ISO7242C
www.ti.com/product/SN65C1167

Analog linearization of resistance temperature detectors

By Bruce Trump
Staff Technologist

Resistance temperature detectors (RTDs) are commonly used in industrial and scientific temperature measurements. The most common types are pure platinum (Pt) formed into wire or evaporated in a thin film on a substrate. They rely on the fundamental temperature-dependent resistance properties of this noble metal. They are very stable and useful at temperatures ranging from cryogenic to over 800°C. A wide range of physical configurations, resistance ranges and accuracies is available.[1] The commonly used notation "Pt100" indicates a 100-Ω resistance at 0°C. The relationship between the RTD's resistance and temperature is described by the Callendar-Van Dusen equation,

$$R_{RTD} = R_0[1 + AT + BT^2 + C(T - 100)T^3],$$

whose values are defined as follows:

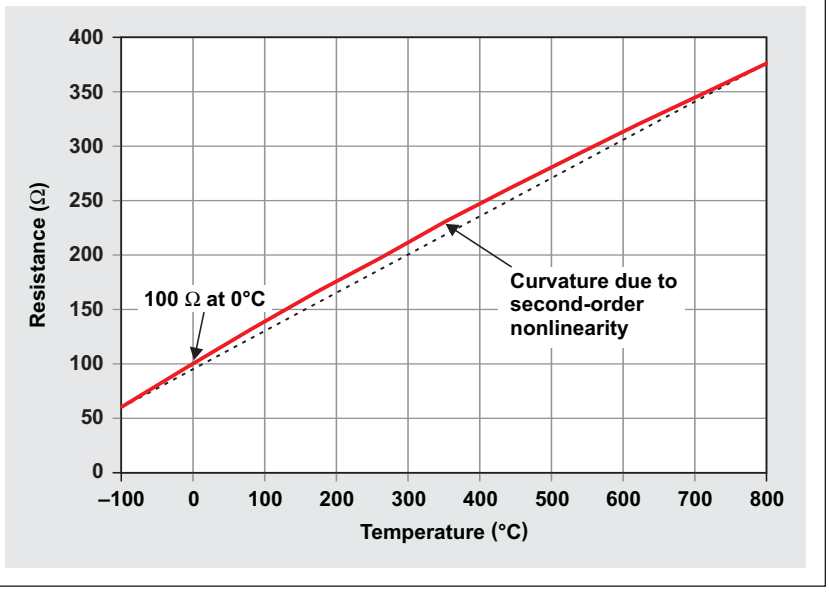
R_0 is a 100-Ω resistance at 0°C (Pt100)
$A = 3.9083 \times 10^{-3}$
$B = -5.775 \times 10^{-7}$
$C = 0$ for $T > 0$°C, or $C = -4.23225 \times 10^{-12}$ for $T < 0$°C.

The resistance of a Pt100 RTD increases with temperature at approximately 0.39%/°C. While they are far more linear than thermocouples, RTDs have a significant second-order nonlinearity of approximately 0.38% per 100°C measurement range (see Figure 1). This nonlinearity is often corrected digitally, but there are many applications for purely analog processing and linearization of the RTD.

This article explains an analog technique for linearization of the RTD. The same technique is also used with bridge sensors such as pressure and load cells. The principles can be applied to other ratiometric devices with primarily second-order nonlinearity; i.e., any sensor or system with an output that is proportional to an excitation voltage or current.

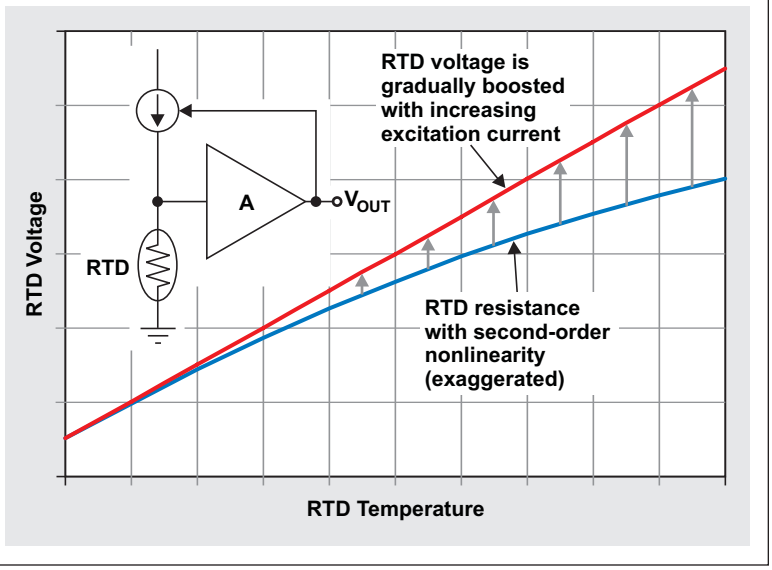
The exaggerated graph in Figure 2 shows that the temperature coefficient decreases with increasing temperature, producing an upward bow in the middle. Above 0°C, standardized data for the Pt100 has a purely second-order or parabolic function. Assuming calibration at two endpoint temperatures, this produces an error that is greatest at the midpoint temperature.

Figure 1. Resistance of Pt100 RTD versus temperature



When the RTD is excited with a current source, the resulting RTD voltage is directly proportional to the resistance, yielding the same nonlinearity. If, however, the excitation current is gradually increased as the RTD temperature

Figure 2. RTD voltage versus temperature



is increased, the nonlinearity can be greatly reduced. Figure 2 shows an increasing excitation current derived from the output of the amplified RTD voltage. This current is, in effect, a controlled amount of positive feedback. It yields an interesting "chicken-or-egg" dichotomy: The RTD voltage at the input of the amplifier is linearized when the output of the amplifier is linearized—and vice versa. The correct amount of positive feedback results in both.

When positive feedback is optimized, a much smaller s-shaped error remains with nearly equal negative and positive values, reaching maximums at ¼ and ¾ full scale (see Figure 3). This primarily third-order nonlinearity does not come from the RTD but is an artifact of the linearization technique. Its magnitude depends on the temperature range chosen for linearization. Figure 3 shows the initial nonlinearity error for a –100°C to +800°C temperature range—a 900°C span. The 3.7% RTD nonlinearity at midscale is reduced to approximately ±0.11%, a 33:1 improvement. The improvement is even greater for narrow temperature ranges, approaching 150:1 for a 200°C range.

The use of positive feedback might raise the concern of possible circuit instability. The magnitude of this feedback is small enough, however, to have negligible effect on the stability of commonly used circuits.

Figure 4 shows a practical implementation of an RTD. R1 provides the primary excitation current from V_{REF}, a stable voltage reference. R5 provides the temperature-varying component of excitation current from the output of A1. R2, R3, and R4 set the required amplifier gain and offset to produce the desired output-voltage range. The Texas Instruments (TI) OPA188* shown in this example is a new low-noise, chopper-stabilized operational amplifier that contributes negligible error to the circuit. Its very low and stable offset voltage makes it a possible upgrade to TI's OPA277 precision industrial amplifier.

The resistor values to achieve best correction can be calculated with iterative techniques. Many designers might optimize this type of circuit by using creative calculations or approximations. A closed-form solution is possible by solving the nodal equation that relates the RTD voltage, RTD resistance, V_{REF}, R1, R5, and V_{OUT}:

$$V_{RTD} = V_{REF} \times \frac{\frac{R_{RTD} \times R5}{R_{RTD} + R5}}{\frac{R_{RTD} \times R5}{R_{RTD} + R5} + R1} + V_{OUT} \times \frac{\frac{R_{RTD} \times R1}{R_{RTD} + R1}}{\frac{R_{RTD} \times R1}{R_{RTD} + R1} + R5}$$

Figure 3. Percentage of RTD error versus temperature

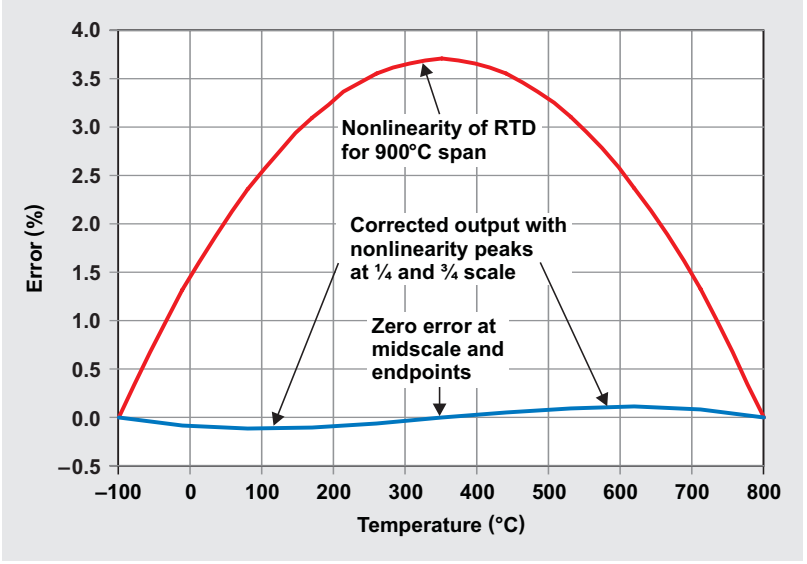
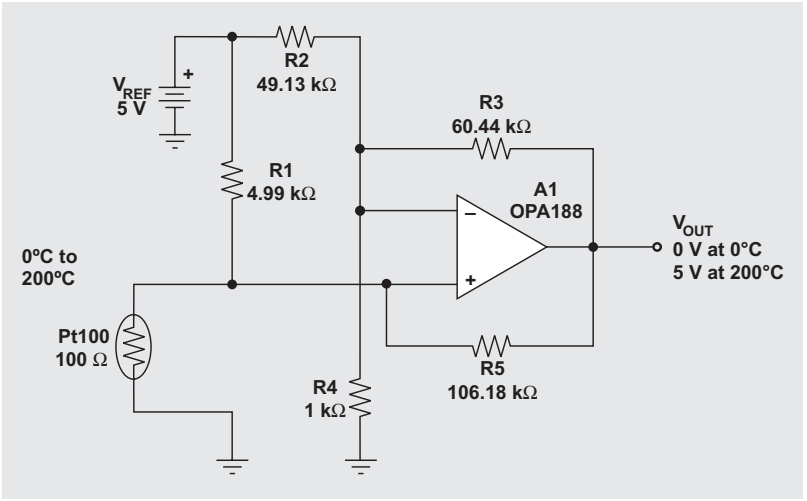


Figure 4. Typical RTD configuration with error compensation



*The OPA188 is expected to be available in early 2012. For general specifications, please refer to the dual version, OPA2188, at www.ti.com/product/OPA2188

Three conditions must be met to achieve zero error at the calibration endpoint temperatures and the midpoint temperature. Three separate variations of the preceding equation are written to describe the three zero-error conditions and are solved simultaneously for the only unknown variable, R5. The resistance of the RTD at the midpoint temperature is not halfway between the endpoint resistances. This midpoint condition holds the key to the solution for best linearity correction.

The math yields three results for R5; only one is a positive resistance. The expression for R5 is very long and impractical to present here. To download an Excel® worksheet that provides the calculations, go to http://www.ti.com/lit/zip/SLYT442 and click Open to view the WinZip® directory online (or click Save to download the WinZip file for offline use). Then open the file RTD_Linearization_v7.xls to view the calculation worksheet. This closed-form solution is intellectually satisfying and avoids possible problems with convergence, but the results are no better than those produced with iterative calculations. Practical implementations often require trimming of resistors for calibration because accurate, nonstandard values are often required. SPICE simulation can help determine actual performance with the nearest standard values. The WinZip file download listed above also includes two RTD simulation examples in TINA-TI™ SPICE files. One file implements an RTD linearization circuit based on an operational amplifier, and the other file is based on an instrumentation amplifier. Please see Reference 2 for more information on an RTD simulator for SPICE.

Figure 5 shows that uncorrected nonlinearity of the RTD increases as the calibrated temperature range is increased, reaching approximately 2% for a 500°C span. The variation in the RTD's excitation current to compensate for this nonlinearity is approximately four times the nonlinearity. Thus, for a 500°C measurement span, the excitation current increases by approximately 8% from low-scale temperature to full scale.

Low-resistance connections to the RTD are crucial in maintaining accuracy with this circuit. For this reason, high-resistance RTDs such as Pt1000 or Pt5000 may be most practical. With a four-wire (or Kelvin) connection to the RTD and an additional operational amplifier, errors induced by wire resistance can be eliminated.

An integrated instrumentation amplifier with a three-wire RTD connection can provide an alternative solution (see Figure 6). In the three-wire connection, two connections are used on the ground side of the RTD. Equal currents flowing in equal line resistances create a common-mode input voltage that is rejected by the instrumentation amplifier. Current flowing in the ground-wire connection also creates a common-mode voltage. Note that the currents in signal connections are not precisely equal. They differ due to the varying linearity correction current from R5. Nevertheless, this configuration removes most of the error that is due to line resistance.

Figure 5. Correlation of excitation current to RTD error

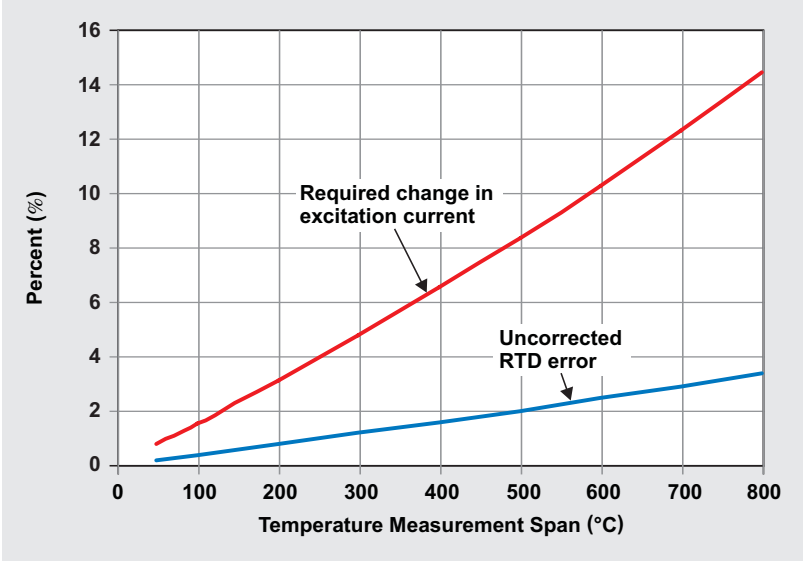


Figure 6. Amplifier with three-wire RTD connection

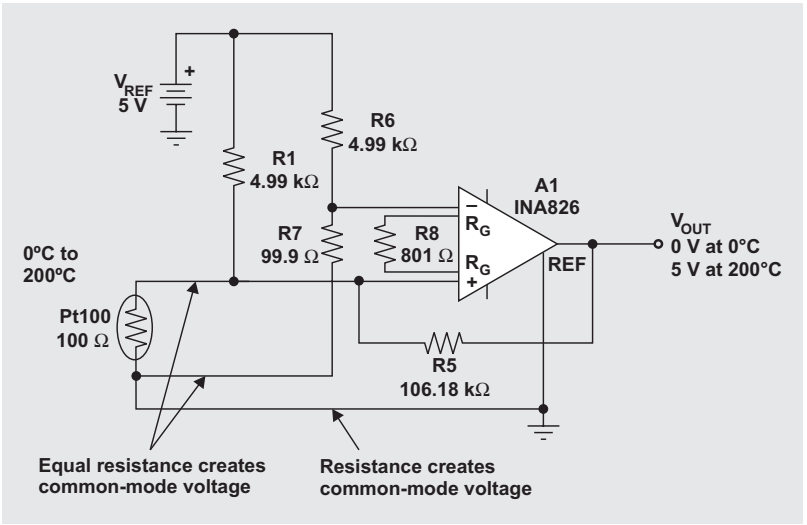


Table 1. Partial listing of TI's integrated circuits for RTDs and bridge sensors

PRODUCT	SENSOR TYPE	EXCITATION	OUTPUT	FEATURES
XTR105	RTD	Dual 1-mA current	4 to 20 mA	Resistor-programmed range and linearization
XTR106	Pressure bridge	Voltage	4 to 20 mA	Corrects positive or negative second-order nonlinearity
XTR108	RTD	Dual programmable current	4 to 20 mA or voltage	Programmable excitation current and linearization
XTR112	High-impedance RTD	Dual 100-µA current	4 to 20 mA	Excitation for Pt1000 RTD
XTR114	High-impedance RTD	Dual 250-µA current	4 to 20 mA	Excitation for Pt5000 RTD
PGA309	Pressure bridge	Programmable voltage	Voltage	Digitally controlled analog-signal path with linearization

Other sensor types

Bridge sensors such as strain gauges and load cells frequently require linearization with similar techniques. Voltage excitation is generally used for these applications, but the concept is the same. Excitation voltage is varied with amplifier output voltage. These sensors can have a downward bowing nonlinearity requiring that the excitation voltage decrease as pressure increases. Furthermore, nonlinearity may vary significantly from unit to unit, so individual calibration may be required.

Integrated solutions

TI uses variable excitation for linearization in several integrated circuits intended for RTDs and bridge sensors (see Table 1). Some circuits are designed specifically for remote sensors with two-wire, 4- to 20-mA current-loop output. XTR106 and PGA309 provide voltage excitation, which is preferred for many strain-gauge bridge-sensor applications. Though designed for specific sensor types, these devices have been successfully adapted to a variety of sensor applications, with and without variable excitation for linearization.

References

1. Resistance thermometer. *Wikipedia* [Online]. Available: http://en.wikipedia.org/wiki/Resistance_thermometer
2. Thomas Kuehl. (2007, May 28). Developing a precise Pt100 RTD simulator for SPICE. *EN-Genius Network: analogZONE: acquisitionZONE* [Online]. Available: http://www.analogzone.com/acqt_052807.pdf
3. Bruce C. Trump. (1994, March 3). Pressure gauge responds linearly to altitude. *EDN* [Online]. Available: http://www.edn.com/archives/1994/030394/05di5.htm

Related Web sites

www.ti.com/product/*partnumber*
Replace *partnumber* with INA826, OPA277, OPA2188, PGA309, XTR105, XTR106, XTR108, XTR112, or XTR114

Support files with Excel spreadsheet and TINA-TI™ simulation examples:
www.ti.com/lit/zip/SLYT442

Index of Articles

Power Management *(Continued)*

TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page
support.ti.com

TI E2E™ Community Home Page
e2e.ti.com

Product Information Centers

Americas Phone +1(972) 644-5580

Brazil Phone 0800-891-2616

Mexico Phone 0800-670-7544

Fax +1(972) 927-6377

Internet/Email support.ti.com/sc/pic/americas.htm

Europe, Middle East, and Africa

Phone

European Free Call	00800-ASK-TEXAS (00800 275 83927)
International	+49 (0) 8161 80 2121
Russian Support	+7 (4) 95 98 10 701

Note: The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

Fax	+(49) (0) 8161 80 2045
Internet	support.ti.com/sc/pic/euro.htm
Direct Email	asktexas@ti.com

Japan

Phone	Domestic	0120-92-3326
Fax	International	+81-3-3344-5317
	Domestic	0120-81-0036
Internet/Email	International	support.ti.com/sc/pic/japan.htm
	Domestic	www.tij.co.jp/pic

Asia

Phone

International	+91-80-41381665
Domestic	Toll-Free Number

Note: Toll-free numbers do not support mobile and IP phones.

Australia	1-800-999-084
China	800-820-8682
Hong Kong	800-96-5941
India	1-800-425-7888
Indonesia	001-803-8861-1006
Korea	080-551-2804
Malaysia	1-800-80-3973
New Zealand	0800-446-934
Philippines	1-800-765-7404
Singapore	800-886-1028
Taiwan	0800-006800
Thailand	001-800-886-0010

Fax	+8621-23073686
Email	tiasia@ti.com or ti-china@ti.com
Internet	support.ti.com/sc/pic/asia.htm

A122010

SLYT437