Message priority inversion on a CAN bus

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New Product Definition

This article examines the problems encountered during data transmission when multiple dominant bits are simultaneously placed on a bus by more than one node during arbitration or an ACK bit. CAN buses are often constructed with many nodes placed physically close together. When these "clumps" of nodes are spaced a long distance from other nodes on the bus, random data errors can occur. A "message priority inversion" error causes a high-priority message to receive low-priority placement after arbitration. Uneven node spacing can also affect the ACK procedure in a CAN message. If a message is not properly acknowledged because of interruptions from reflected waves, an error is generated with each occurrence until the controller reaches an error limit that is internally set by the CAN protocol. The controller places itself in a bus-off state when this internal limit is reached so that a single node cannot block all communication on the bus. These errors are not easily uncovered by a system designer.

Minimum distance between nodes on a CAN bus

The ISO 11898-2:2003 CAN bus is a distributed-parameter circuit whose electrical characteristics are primarily defined by the distributed inductance and capacitance* along the physical media. The media are defined as the interconnecting cable or the conducting paths, connectors, terminators, and CAN transceivers added along the bus.

The following analysis examines a trade-off between the amount of node capacitance that can be added and the amount of node spacing that can be used on a bus without compromising signal integrity. For a good approximation, the characteristic transmission-line impedance looking into an arbitrary end point in an unloaded CAN bus is defined by $Z = \sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. When capacitance is added to the bus in the form of devices and their interconnection, the bus impedance is lowered to Z′. When bus impedance is lowered, an impedance mismatch occurs between unloaded and loaded sections of the bus.

The worst case occurs during an arbitration or an ACK bit when multiple dominant bits are simultaneously sent from two or more nodes. In the equivalent bus circuit shown in Figure 1, when S1 switches at time zero from a dominant state to a recessive state, the differential output voltage, V_S, of the CAN driver moves from a dominant state to a steady-state, 0-V, recessive differential signal on the bus. When this signal wave propagates down the line and arrives at the loaded section of the bus, the mismatch in impedance reflects the voltage back towards the source.

*All capacitances are differential in this article. The differential is approximately one-half of the single-ended capacitance.

Figure 1. Imbalanced CAN-bus equivalent circuit

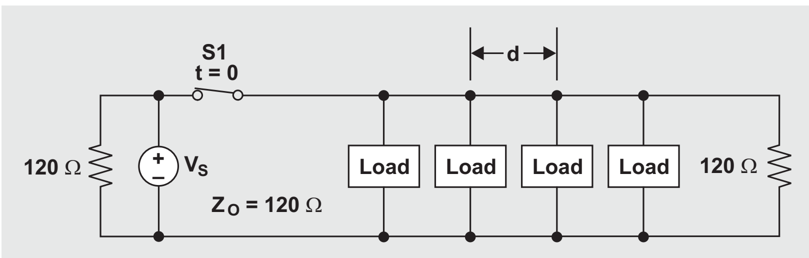
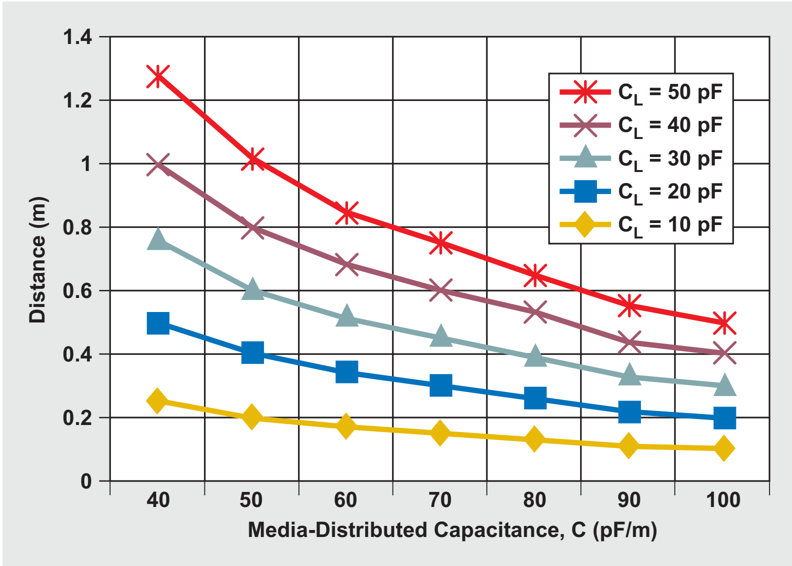


Figure 2. Minimum distance required between CAN nodes



The minimum safe distance between nodes, d, is a function of the device lumped-load capacitance, C_L, and the cable's distributed capacitance per unit length, C, where $d > C_L/0.98\ C$ meters (if C is in pF/m) or feet (if C is in pF/ft). Figure 2 displays this relationship graphically. For a complete development of this equation, please see Reference 1.

Load capacitance includes contributions from a CAN transceiver's bus pins, connector contacts, printed-circuit-board traces, protection devices, and any other physical connections as long as the distance from the bus to the transceiver is kept electrically short.

3.3-V CAN transceivers such as the Texas Instruments SN65HVD233 have about 16 pF of differential capacitance. Board traces add about 0.5 to 0.8 pF/cm, depending upon their construction. The capacitance of connectors and suppression devices can vary widely, and media-distributed capacitance ranges from about 35 pF/m for low-capacitance, shielded, twisted-pair cable to 70 pF/m for backplanes.

As a demonstration of how multiple dominant bits on the same bus affect data-transfer waveforms, ten SN65HVD233 CAN transceivers were connected to a bus with 12.7 cm of 120-Ω twisted-pair cable between each node (see Figure 3). The last node of the group was terminated with a 120-Ω termination resistor, and the first node was connected through an additional 200 m of Belden 3105A twisted-pair cable to another node and terminated.

Figure 3. Example of a capacitive load

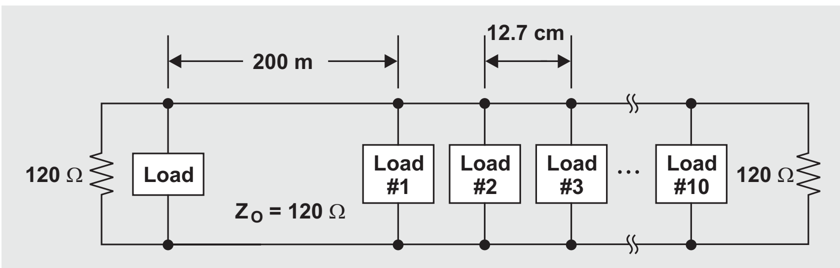


Figure 4 shows the receiving waveform of the 250-kbps data being transmitted onto the bus from the single-node load to the capacitive clump of nodes across the 200-m cable. Figure 5 shows the same waveform when more than one node sends a dominant bit onto the bus during an arbitration. Note the change in magnitude of the waveform. The propagation delay of 5 ns/m for 200 m is 1000 ns, or 1 µs, and is clearly evident. The negatively charged waveform is reflected back and attenuates the back of the waveform at the receiving clump of nodes. Figure 6 presents a higher resolution of this reflection.

Figure 6 is a good example of the possible arbitration bit-error problem, since the waveform voltage that is due to the negative reflection reduces the differential voltage of the signal to below the 900-mV dominant-bit threshold. Note that this is a single point-to-point bus connection and that any variation such as adding a drop-line to this configuration would serve only to exacerbate the problem. Also, if the signaling rate were increased to 500 kbps, this reflection would last for 50% of the waveform's 2-µs duration.

The lumped-load capacitance, C_L, of each CAN transceiver, board trace, and Berg connector amounts to approximately 20 pF per node in this example; and the distributed capacitance per unit length, C, is about 40 pF/m. The node-spacing calculation results presented in Figure 2 (C_L = 20 pF and C = 40 pF/m) indicate that 0.5 m of cable between each of the clumped nodes in place of the 12.7-cm cable will correct the problem (see Figure 7). Clearly, the calculations prove to be correct. The reflected wave has almost completely disappeared, and the added twisted-pair cable is a small price to pay for a reliable solution.

Figure 4. Normal data traffic on a CAN bus

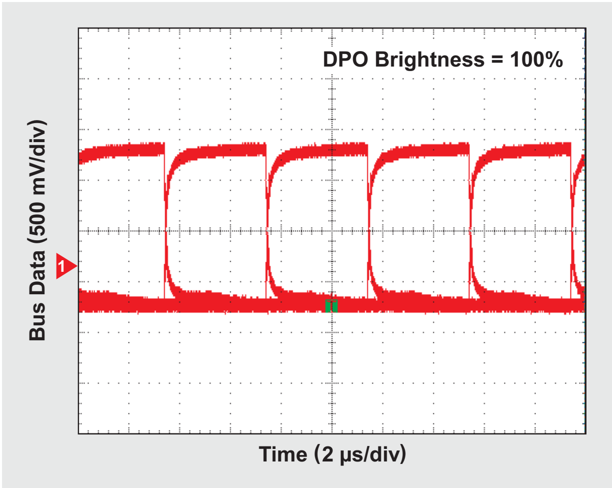


Figure 5. Distortion from multiple dominant bits on the same bus during arbitration

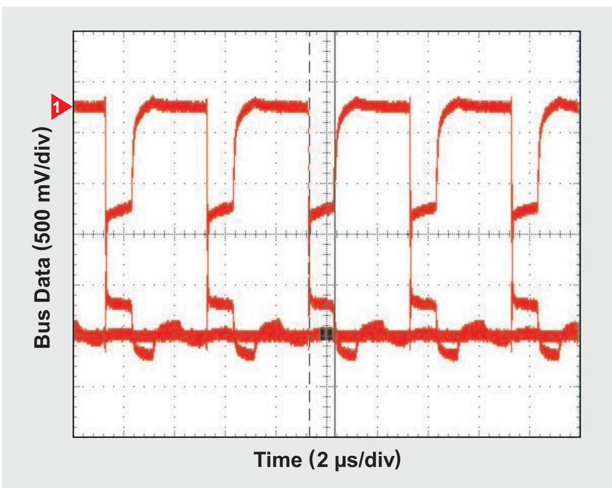


Figure 6. Reflected-wave distortion by multiple dominant bits

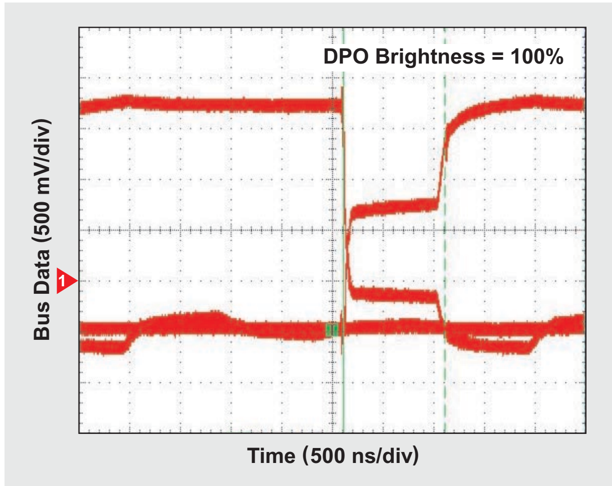
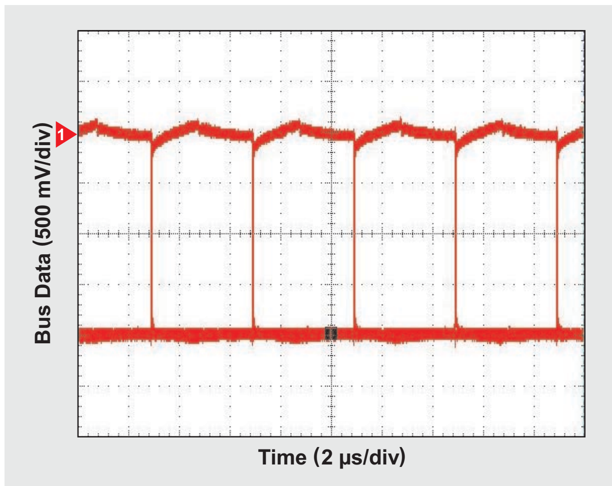


Figure 7. Addition of 0.5 m to bus length



Conclusion

A CAN bus that has not been optimized to minimize reflected energy at each node can cause a host of network problems. Even when data transfer seems to be working normally, dominant-bit collisions that occur randomly during arbitration or by design during an ACK bit may create sufficient signal reflections to cause priority inversion and delays from acknowledgment errors. Of course, more pronounced reflections can cause excessive bus delays due to bit-stuffing errors and normal data errors. These reflections can usually be controlled by optimizing the spacing between nodes according to established data-transmission practices.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Steve Corrigan, "Controller Area Network Physical Layer Requirements," Application Report	slla270

Related Web sites

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