High-Speed Communications Solutions

TSW3003: RF Transmit Signal Chain Demonstration Kit

Texas Instruments (TI) introduces a new tool in the TSW Solutions Family: the TSW3003, a demonstration kit to help design and optimize your RF transmit signal chain. This new tool demonstrates an In-phase and Quadrature (IQ) modulation transmit system with impressive RF performance numbers and the versatility to be adapted to various RF applications. The TSW3003 demo kit includes the DAC5687, a 16-bit, 500 MSPS DAC; a CDCM7005 clock device to satisfy clocking requirements for the accompanying devices; a passive interface to the TRF3703, a direct-launch IQ modulator; and the TRF3761, an integer N PLL with an integrated VCO to drive the local oscillator (LO) of the TRF3703.

The TSW3003 is designed for wireless base station transceivers, fixed wireless transmitters and digital predistortion applications using full IQ compensation, selectable interpolation, flexible input options and multiple outputs. This new tool implements all the necessary circuits from the DAC input to the output of the RF IQ modulation.

When the DAC5687 is interfaced with an IQ modulator, for which it is well suited, it has DC offset control and gain/phase control. The DC offset control provides tuning control for carrier suppression, and gain/phase control allows tuning control for sideband rejection. This interface also allows the DAC to provide a passive interface that maximizes power to the modulator and provides a superior adjacent-channel power ratio (ACPR). Other features of the DAC include its use of interpolation capability and a numerically controlled oscillator (NCO) to output intermediate frequencies (IFs) to the modulator. In addition, the IQ compensation feature in the DAC5687 allows optimization of phase, gain and DC offset to maximize sideband rejection and minimize LO feedthrough for an analog quadrature modulator.

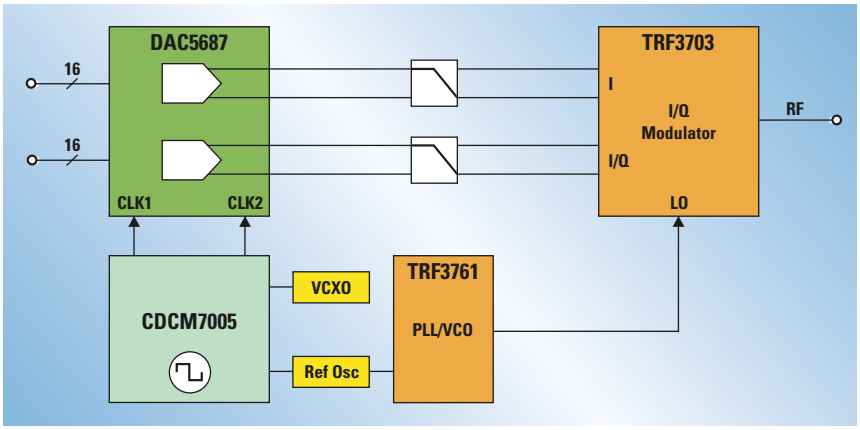
Applications

- Wireless base stations
- Communication test equipment
- Digital predistortion
- RF transmitter signal evaluation

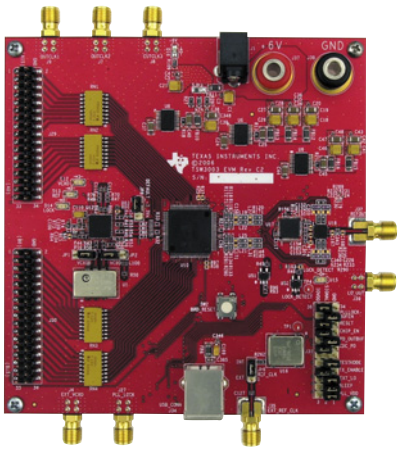
Key Features

- Over 76 dB of ACPR for one WCDMA carrier at 2.14 GHz
- Full IQ compensation including DC offset, gain and phase control for excellent LO and sideband suppression
- 500 MSPS, 16-bit-resolution DAC
- Complex mixer with 32-bit NCO, and coarse mixer at Fs/4 and Fs/2
- RF carriers tunable from 374 MHz to 2385 MHz with an integer N PLL and integrated VCO
- RF output power at 1 dB compression point of +9 dBm, OIP3 of 23 dBm
- Three independent clock outputs selectable by /2^n, LVPECL/LVCMOS interface
- Requires single 6 VDC wall supply included, power management onboard
- Easy-to-use graphical user interface simplifies system setup
- USB interface

TSW3003 Demonstration Kit Block Diagram



TSW3003



The CDCM7005 is a high-performance, low-jitter clock solution that synchronizes an onboard voltage-controlled crystal oscillator (VCXO) to a reference clock. Once the proper reference frequency and programming are applied, the CDCM7005 supplies two clock sources to the DAC and an additional three outputs for external equipment.

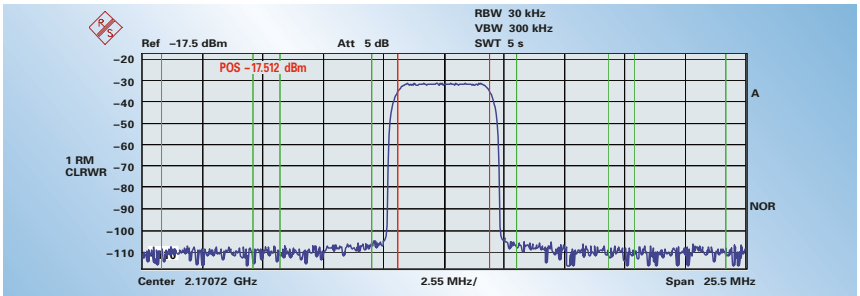
The TRF3703 is a low-noise direct IQ modulator that eliminates the need for an IF stage, improving efficiency and cost. It provides excellent carrier and sideband suppression and also offers high output power with an ultra-low noise floor. Typically the TRF3703 is capable of modulating one WCDMA carrier with 76 dBc ACPR at 2.14 GHz.

The TRF3761 is a LO synthesizer comprising an integer N PLL with integrated VCO. The TRF3761 provides the LO for the TRF3703 quadrature modulator.

The TRF3703 combined with the TRF3761 in the TSW3003 provides lower cost by utilizing an IF system with a single upconversion. In addition, the RF family's controls for carrier suppression and sideband rejection reduce filter requirements in the system. The CDCM7005 supplies a suitable clocking solution for the entire transceiver so that less clock circuitry is required.

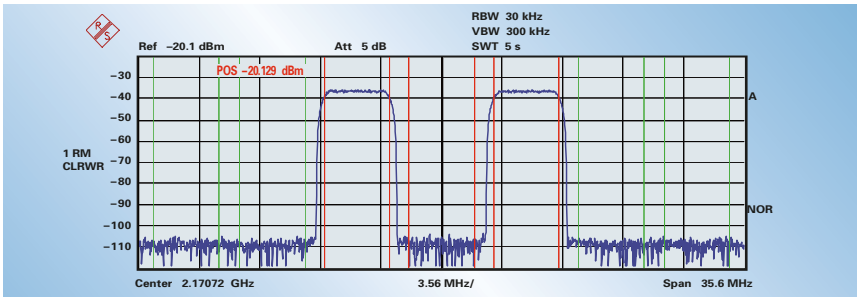
The TSW3003 supports a high-performance signal chain. This demo kit comes complete with a high-performance and versatile DAC, an onboard clock generator and an IQ modulator. This complete RF transmit system offers designers a low-risk, cost-effective alternative to designing a system from scratch. This system can be used to help shorten design cycles by helping with initial proof of concept and can be used as a reference for a reduced BOM RF transmit design.

TSW3003 Single-Carrier Test Mode 1 WCDMA
Typical Performance with IF = 30.72 MHz, LO = 2.14 GHz



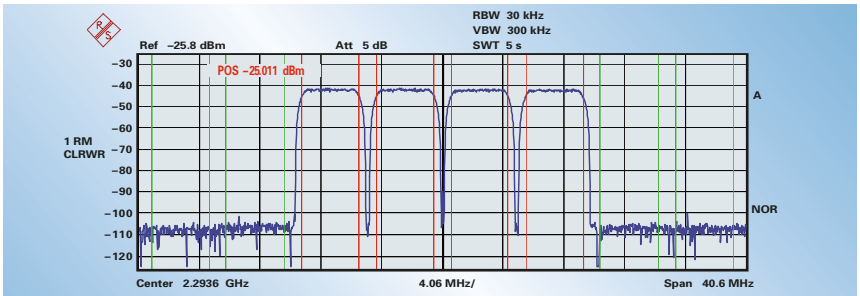
Tx Channel	Bandwidth	3.84 MHz	**WCDMA 3GPP FWD**	Power	–11.85 dBm
Adjacent Channel	Bandwidth	3.84 MHz		Lower	–76.67 dB
	Spacing	5 MHz		Upper	–76.59 dB
Alternate Channel	Bandwidth	3.84 MHz		Lower	–77.96 dB
	Spacing	10 MHz		Upper	–77.75 dB

TSW3003 Missing Middle Carrier Test Mode 1 WCDMA
Typical Performance with IF = 30.72 MHz, LO = 2.14 GHz



Standard: WCDMA 3GPP FWD			**Adjacent Channel**	Lower	–72.90 dB
Tx Channels	Ch1 (Ref)	–16.46 dBm		Upper	–72.69 dB
	Ch2	–88.87 dBm	**Alternate Channel**	Lower	–72.51 dB
	Ch3	–16.56 dBm		Upper	–72.55 dB
	Total	–13.50 dBm			

TSW3003 4-Carrier Test Mode 1 WCDMA
Typical Performance with IF = 153.6 MHz, LO = 2.14 GHz



Standard: WCDMA 3GPP FWD			**Adjacent Channel**	Lower	–64.03 dB
Tx Channels	Ch1 (Ref)	–22.39 dBm		Upper	–64.65 dB
	Ch2	–22.48 dBm	**Alternate Channel**	Lower	–65.48 dB
	Ch3	–22.63 dBm		Upper	–64.78 dB
	Ch4	–22.72 dBm			
	Total	–16.53 dBm			