Texas Instruments

HIGH VOLTAGE SEMINAR

GANGYAO WANG
ISOLATED GATE DRIVERS

GETTING STARTED WITH PROGRAMMING FUNCTIONAL SAFETY COMPLIANT GATE DRIVERS FOR EV/HEV TRACTION INVERTERS

Agenda

- Overview
- Getting started with the programming:
  - Modes of operation
  - SPI introduction
  - SPI commands
  - Daisy chain mode and address mode SPI
  - Writing a register
  - Reading a register
  - Frame timings for daisy chain and address mode SPI
  - General device setup
  - Enabling the driver
  - SPI communication in ACTIVE mode
  - Exiting ACTIVE mode
  - ADC sampling mode, setup and reading results
- EVM Demo

UCC5870-Q1 overview

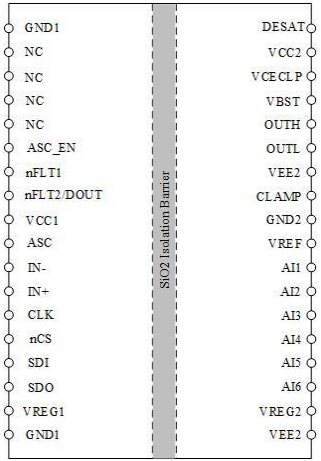
±15A ISO26262-compliant IGBT/SiC single-channel isolated driver

Features

- **Split driver outputs provide 15-A source and 15-A sink currents**
- **Real-time SPI programmable drive strength**
- **SafeTI™ ISO-26262 compliant:**
  - Power transistor protections (DESAT/SC/OC)
  - Integrated diagnostics
  - Supply monitors (VCC1/VCC2/VEE2/VREF)
  - Built-in self-test (BIST)
- **SPI-Enabled Configurations:**
  - TI Address-based SPI configuration (also daisy chain and standard)
  - DESAT based short circuit protection
  - Shunt resistor based over-current protection
  - Thermal diode/NTC based over-temperature protection
  - Programmable soft turn off (STO) and two-level turn off (2LTO) during power transistor faults
- **High accuracy, integrated 6-channel ADC**
- **Primary and Secondary side active short circuit (ASC) support**
- **Integrated, configurable dead-time**
- **Programmable internal or external Miller Clamp**
- **Advanced high voltage clamping control (V_{CE} Clamp)**

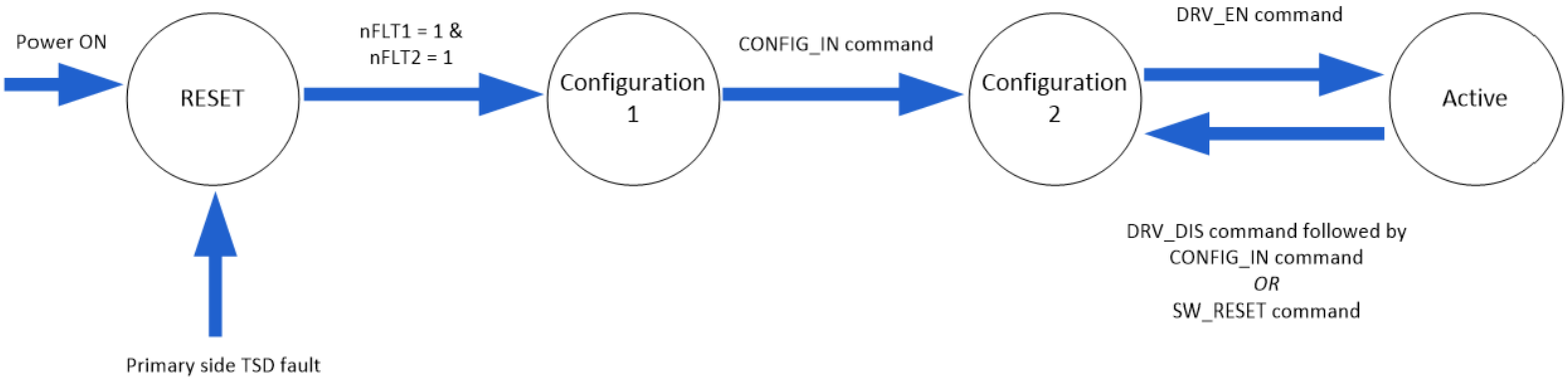
Benefits

- One-stop-shop gate driver for every HEV/EV traction inverter system
- Eliminate external circuits for driving high power modules; save PCB area space and cost
- Highly flexible through SPI-programmable configurations
- SafeTI™ Functional Safety support & documentation



BODY SIZE (NOM)
12.8 mm × 7.5 mm

Modes of operation



RESET:

- Internal regulators powering up
- BIST is running
- nFLTx are held low until the regulators are ready and BIST completes without failures

Configuration 1:

- SPI address programming is enabled
- nFLTx remain high unless indicating a fault

Configuration 2:

- DRV_EN_RCVD = 0
- Gate driver output is disabled (low)
- SW_RESET command sets configration registers to defualt values except for SPI address

Active:

- DRV_EN_RCVD = 1
- Gate driver output is enabled

Figure 7-37. Operation mode diagram during normal operation

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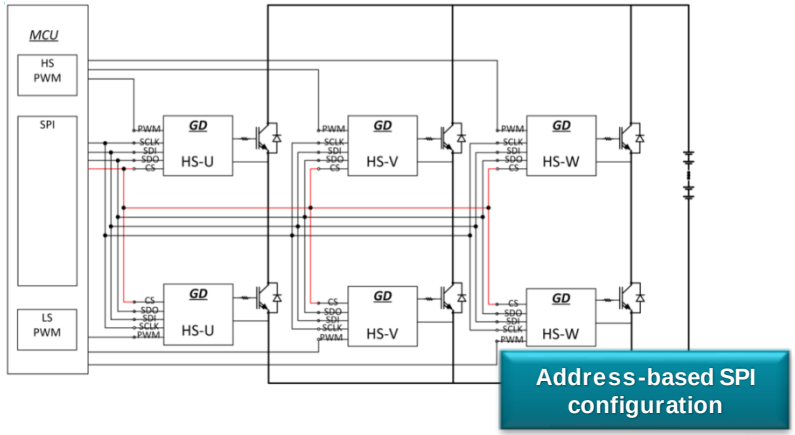
SPI introduction: flexibility, system programmability

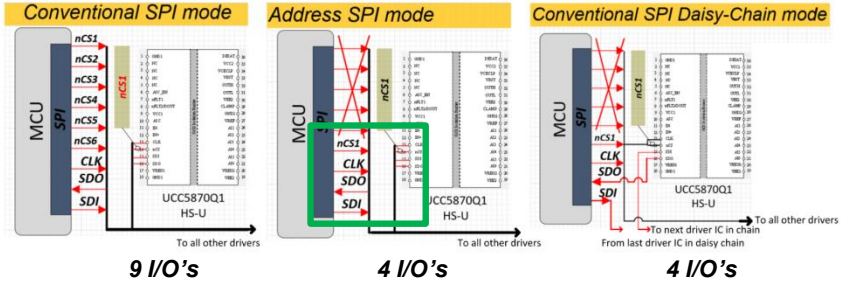
System Benefits



Address-based SPI configuration

- ✓ **System flexibility:** Option between **3 communication modes** (address-based, daisy-chain, regular SPI)
- ✓ **Ease of system programmability**: Simplify design time and engineering effort
- ✓ **Address-based SPI:** Only requires **4 I/O pins** and provides **6x shorter response time** compared to daisy chain configuration

Measurements & Specifications



Flexibility in SPI connections and I/O's
TI's address-mode allows less I/O's per system at shorter response time while maintaining high data throughput

Driver features configurable with SPI:	
▪ Thresholds and deglitches	▪ Drive Strength
▪ ADC sampling and mode	▪ Active Short Circuit (ASC)
▪ Faults and warnings	▪ DESAT OR Shunt/Sense FET Current Sense

SPI commands

Table 7-3. SPI message commands

		16-BIT DATA FRAME															
		BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Command Name	Command Description	CHIP_ADDR				CMD + DATA											
DRV_EN	Driver output enable	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	0	0	0	0	0	1	0	0	1
DRV_DIS	Driver output disable	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	0	0	0	0	0	1	0	1	0
RD_DATA	Read data from register address RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	1	0	0	0	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
CFG_IN	Enter configuration state	CA[3]	CA[2]	CA[1]	CA[0]	0	0	1	0	0	0	1	0	0	0	1	0
NOP	No operation	CA[3]	CA[2]	CA[1]	CA[0]	0	1	0	1	0	1	0	0	0	0	1	0
SW_RESET	Software RESET (Reinitialize the configurable registers)	CA[3]	CA[2]	CA[1]	CA[0]	0	1	1	1	0	0	0	0	1	0	0	0
WRH	Write D[15:8] to register RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	0	1	0	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
WRL	Write D[7:0] to register RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	0	1	1	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
WR_RA	Write register address RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	1	0	0	0	0	0	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
WR_CA(1)	Write chip address CA[3:0]	1	1	1	1	1	1	0	1	1	0	1	0	CA[3]	CA[2]	CA[1]	CA[0]

(1) IN+ must be high to program CHIP address

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Daisy chain mode

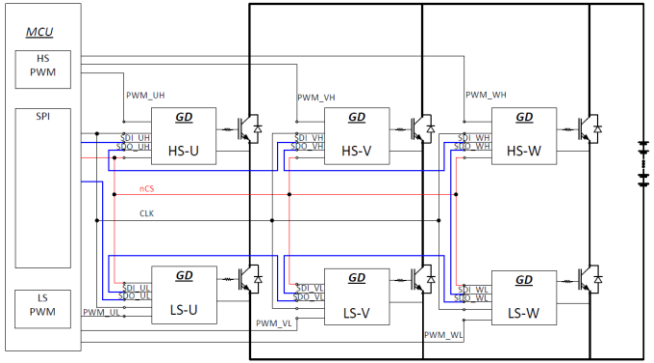
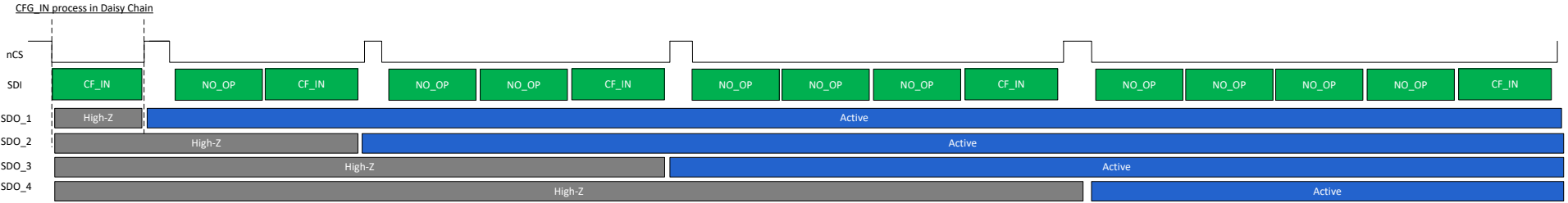


Figure 7-40. System configuration of daisy chain SPI configuration

- Use 0x0 as the address for every command
- No addressing needed, proceed directly to Configuration 2 state
- The devices must receive the CFG_IN command one by one in order to enable the daisy chain mode and the SDO pass-through



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Address mode

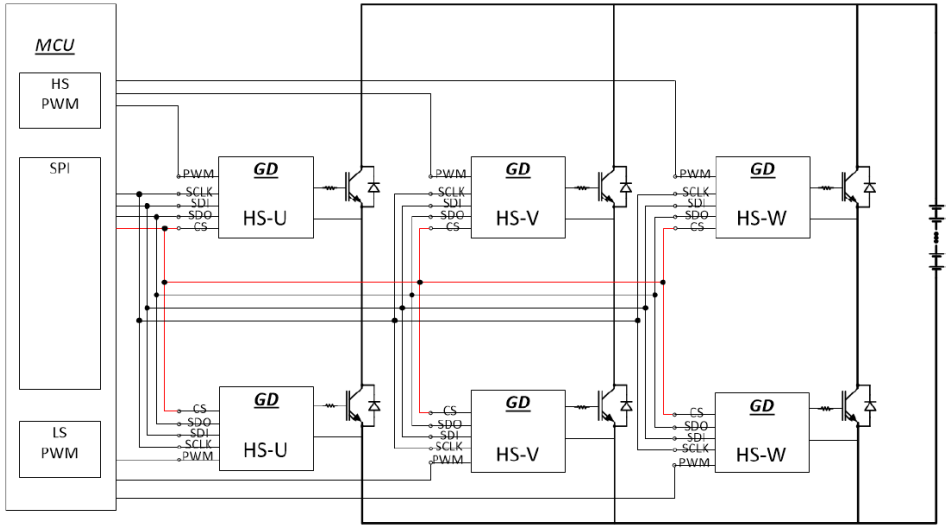


Figure 7-42. System configuration for Address-based SPI Communication Scheme

- Addressing Process:
  - Addressing occurs in Configuration 1 state. Do not enter Configuration 2. Once out of Configuration 2, a power cycle is needed to re-enter Configuration 1.
  - Pull the IN+ input high for ONLY the device to be programmed
  - Write the WR_CA command (below), where CA[3:0] is the address for the device (0x1 - 0xE)
  - Once all devices are addressed, send a broadcast CFG_IN command
- 0xF is a broadcast command. All devices will respond to this address
- Do NOT use 0x0 address. This is reserved for Daisy Chain and Standard operation.
- Each device must have a unique address
- Never do a read register command with 0xF address

WR_CA(1)	Write chip address CA[3:0]	1	1	1	1	1	1	0	1	1	0	1	0	CA[3]	CA[2]	CA[1]	CA[0]

(1) IN+ must be high to program CHIP address

Writing a register

WRH	Write D[15:8] to register RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	0	1	0	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
WRL	Write D[7:0] to register RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	0	1	1	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
WR_RA	Write register address RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	1	1	0	0	0	0	0	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]

- All writes must be performed in Configuration 2 state except for a few exceptions. See later slides (14,15) for exceptions.
- Writing registers can be done with the broadcast address to write all of the devices to the same value, or individually addressed (Address=0xF).
- Steps to write a register:
  - 1. Send WR_RA to set the register to be written. RA[4:0] is the register address to be written.
  - 2. Send WRL command to write the lower byte (bits [8:0]) of the register programmed in step 1. D[7:0] is the data to be written.
  - 3. Send WRH command to write the higher byte (bits [15:9]) of the register programmed in step 1. D[15:9] is the data to be written.
- WRH and WRL can be done in any order, but WR_RA always comes first.
- It is not necessary to do both WRH and WRL commands if only the high byte or low byte is changing.

Reading a register

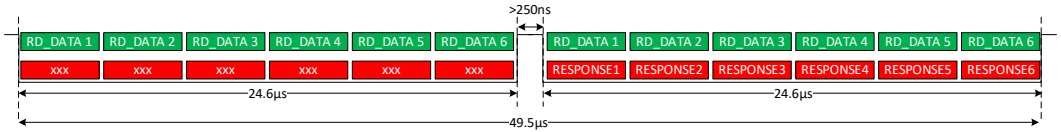
RD_DATA	Read data from register address RA[4:0]	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	1	0	0	0	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
NOP	No operation	CA[3]	CA[2]	CA[1]	CA[0]	0	1	0	1	0	1	0	0	0	0	1	0

- Reading registers can be done in Configuration 2 or ACTIVE modes.
- Reading registers must be done to individually addressed devices. Do **NOT** use the broadcast command
- Procedure to read a register:
  - Use the RD_DATA command where RA[4:0] is the address of the register to be read
  - Data is returned on the next SPI transaction.
  - Use a NOP command to clock the data read out if there is no further command in the stack

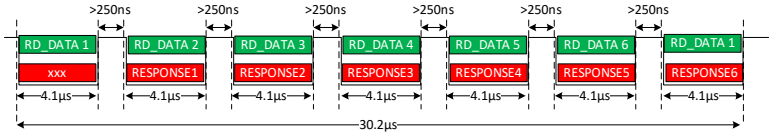
Frame timings: daisy chain and address mode SPI

Reading a single 16-bit register on all 6 devices

Daisy Chain



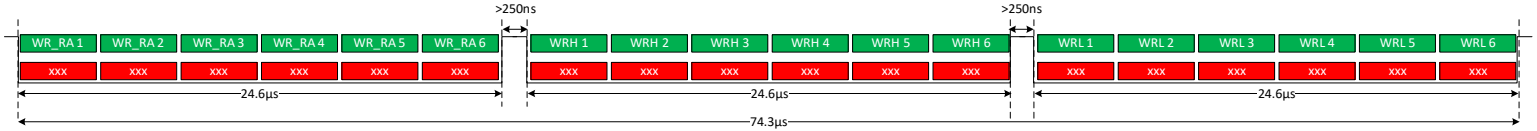
Address Mode



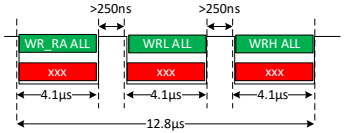
Addressing mode reduces read times by almost 40% while also allowing random access

Writing a single 16-bit register on all 6 devices

Daisy Chain



Address Mode



Addressing mode reduces startup programming time by more than 80%

	Daisy Chain (µs)	Address (µs)
Read all STATUS registers	149.1	134.9
Read all configuration registers	347.9	343.7
Write all configuration registers	965.9	166.4

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General device setup

- *_FAULT_P bits are used to mask faults. When the FAULT_P bit is set to mask the fault, the STATUS bit will still be set during the fault, however, the fault will be ignored (regardless of the FS_STATE) and the nFLTx pins will not trigger.
- FS_STATE_* bits are used to set the reaction to a fault. Generally, this should be set to “Pulled Low” (turn off the power switch), or “No Action” (motor controller to handle the turn off). The notable exception is for “High Impedance” for GM faults. This can prevent damage to the gate driver in the case of a shorted power transistor gate.
  - There are “Pulled High” options for some of the faults, I don’t know why. This was a thing from the original product definer that has never been justified to me, but we left it in.
- *_EN or *_DIS bits enable/disable the function. When a function is disabled, no faults are indicated.
- Writing to any “RESERVED” bit results in a CRC fault
- Writing the SPI_TEST register results in a CRC fault.

Enabling the driver

- Once all of the registers are programmed, send the DRV_EN command.
- This can be sent individually, or with the broadcast command.
- Once the DRV_EN command is sent, the CRC for the configuration registers is calculated and stored. Any bit flips to the configuration registers will result in a CRC fault.
- Most of the write commands to registers are disabled with a few exceptions noted on the next slide.

DRV_EN	Driver output enable	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	0	0	0	0	0	1	0	0	1

SPI communication in ACTIVE mode

- While in ACTIVE mode, all registers are read only with the exception of CONTROL2[CLR_FLT], CFG8[IOUT_SEL], and CFG8[CRC_DIS].
- To change the gate drive strength on the fly, use the following steps:
  - Write the CRC_DIS bit to a ‘1’
  - Write the IOUT_SEL bits to select the required strength
  - Write the CRC_DIS bit to a ‘0’
  - Writing to the IOUT_SEL bit without first writing the CRC_DIS bit results in a CRC fault
- The CONTROL1 and CONTROL2 registers are also used to perform diagnostics for some of the functions. To use these registers in ACTIVE mode, the CRC_DIS bit must be written to a ‘1’ similar to the previous example.
  - In general, these diagnostics are only used during a “Key On” cycle, so write the CRC_DIS bit once, go through all of the diagnostics, then write the CRC_DIS bit back to ‘0’ and proceed with normal operation.

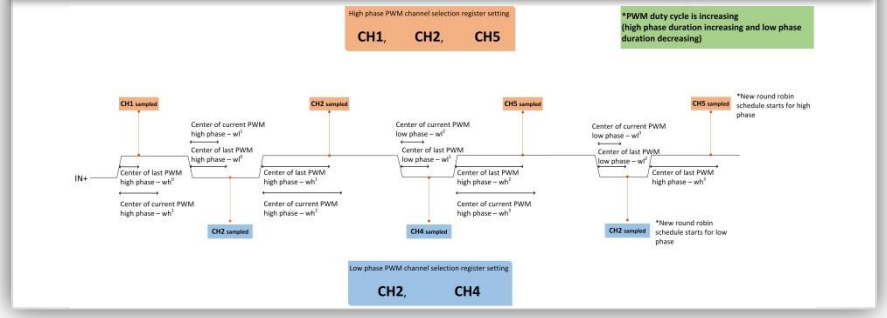
Exiting ACTIVE mode

- ACTIVE mode is exited in one of two ways.
  - Write DRV_DIS to turn off the driver and leave the registers intact
  - Write SW_RESET to turn off the driver and reset all of the registers to the default state. Note that this does NOT change the address
  - After sending one of these commands to turn off the driver, the CFG_IN command must be sent to put the driver back in Configuration 2 state and enable the normal read/write access.

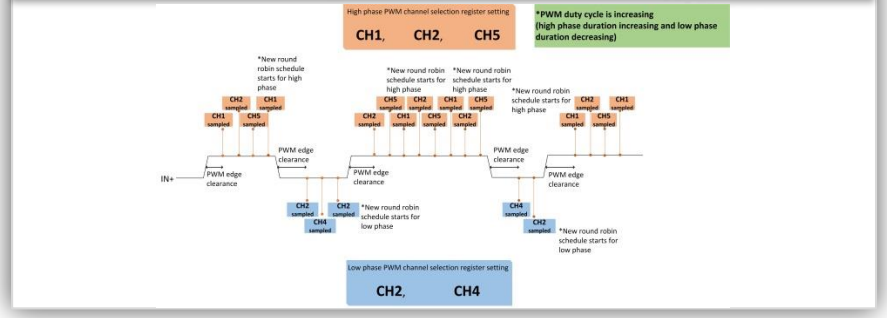
DRV_DIS	Driver output disable	CA[3]	CA[2]	CA[1]	CA[0]	0	0	0	0	0	0	0	0	1	0	1	0
SW_RESET	Software RESET (Reinitialize the configurable registers)	CA[3]	CA[2]	CA[1]	CA[0]	0	1	1	1	0	0	0	0	1	0	0	0

ADC sampling modes

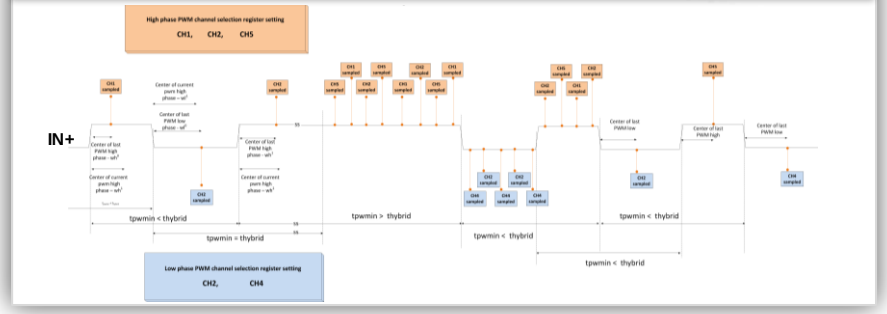
Center Sampling Mode



Edge Sampling Mode



Hybrid Mode



Configuring ADC Modes

- Three modes available to ensure least amount of switching noise
- **Center sampling mode:** samples in middle of switching cycle
- **Edge sampling mode:** samples at start or end of each switching cycle
- **Hybrid sampling mode:** samples mode samples in the center until a cycle is significantly longer then the one before it

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ADC setup

- Setup which channel is to be read and the part of the PWM cycle during which it is to be read.
- Enable the ADC with the ADC_EN bit
- Select the sample mode with the ADC_SAMP_MODE bits
- Set the delay (edge and hybrid modes only) with the ADC_SAMP_DLY bits. These bits are a “don’t care” when using center mode.
- Use the VREF_SEL bit to select between an external 4V reference and the internal reference for the ADC.

Figure 7-74. ADCCFG Register

15	14	13	12	11	10	9	8
RESERVED	ADC_ON_CH_SEL_7	ADC_ON_CH_SEL_6	ADC_ON_CH_SEL_5	ADC_ON_CH_SEL_4	ADC_ON_CH_SEL_3	ADC_ON_CH_SEL_2	ADC_ON_CH_SEL_1
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
RESERVED	ADC_OFF_CH_SEL_7	ADC_OFF_CH_SEL_6	ADC_OFF_CH_SEL_5	ADC_OFF_CH_SEL_4	ADC_OFF_CH_SEL_3	ADC_OFF_CH_SEL_2	ADC_OFF_CH_SEL_1
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R-0x0

Figure 7-51. CFG7 Register

15	14	13	12	11	10	9	8
UVLO2TH		OVLO2TH		UVLO3TH		OVLO3TH	
R/W-0x2		R/W-0x2		R/W-0x2		R/W-0x2	
7	6	5	4	3	2	1	0
ADC_EN	ADC_SAMP_MODE		ADC_SAMP_DLY		ADC_FAULT_P	FS_STATE_ADC_FAULT	
R/W-0x1	R/W-0x0		R/W-0x2		R/W-0x0	R/W-0x0	

ADC reading results

- The ADC results are stored in the ADCDATA* registers.
- The TIME_STAMP updates with every transition on IN+
  - If the TIME_STAMP has not changed since the last read, the data has not been updated, unless it happens to be exactly 63 PWM cycles since the last read.
- Equations to calculate the value of the data when using internal V_{REF}:
  - For AI pin voltage: $V_{AI}=V_{ADC}$(in decimal)*3.519mV;
  - For die temperature: T_{DIE}=DATA_DTEMP(in decimal)*0.7015°C-198.36°C;

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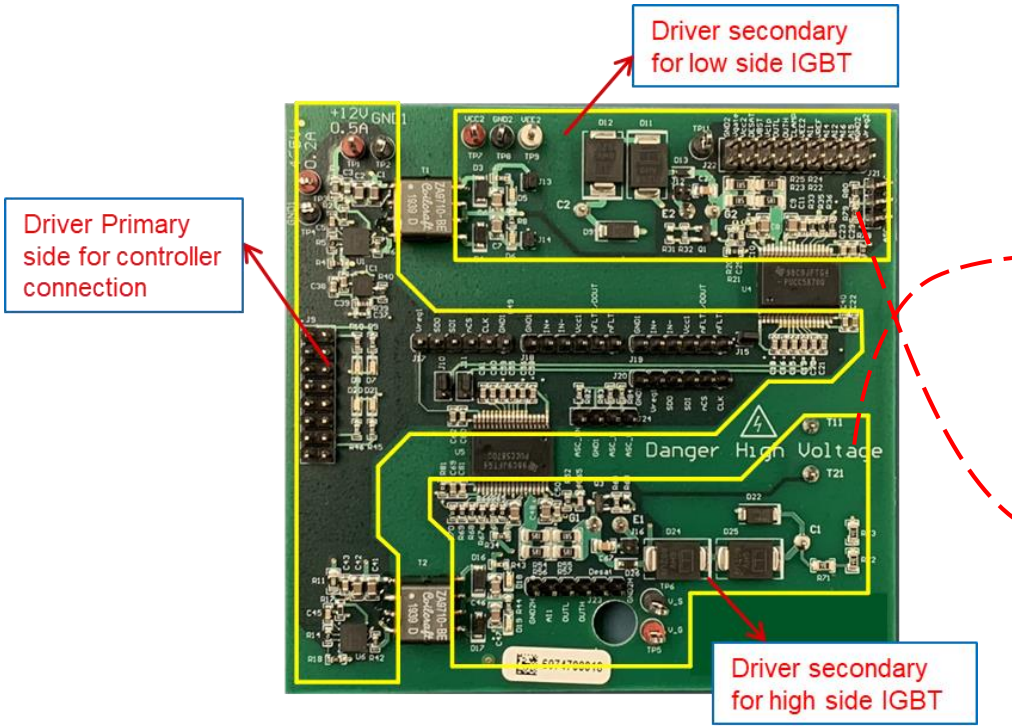
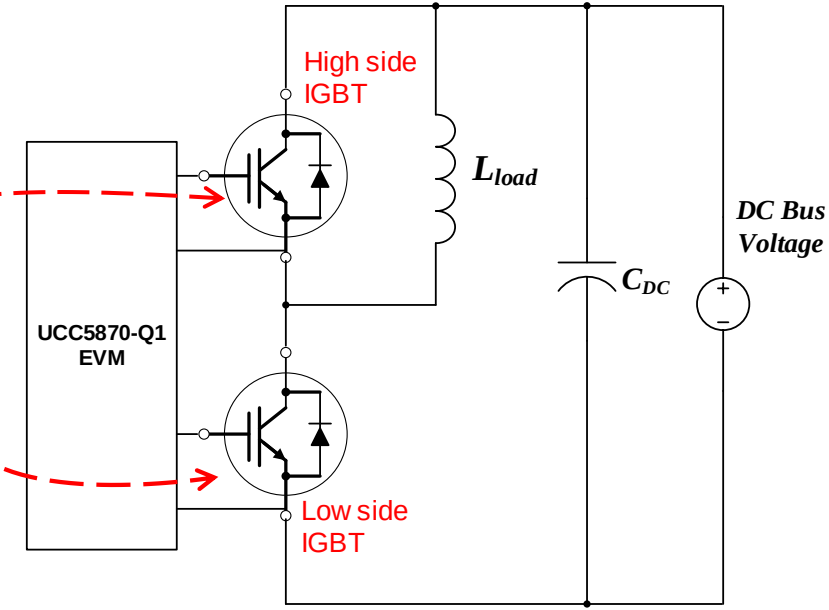
EVM demo: half-bridge board

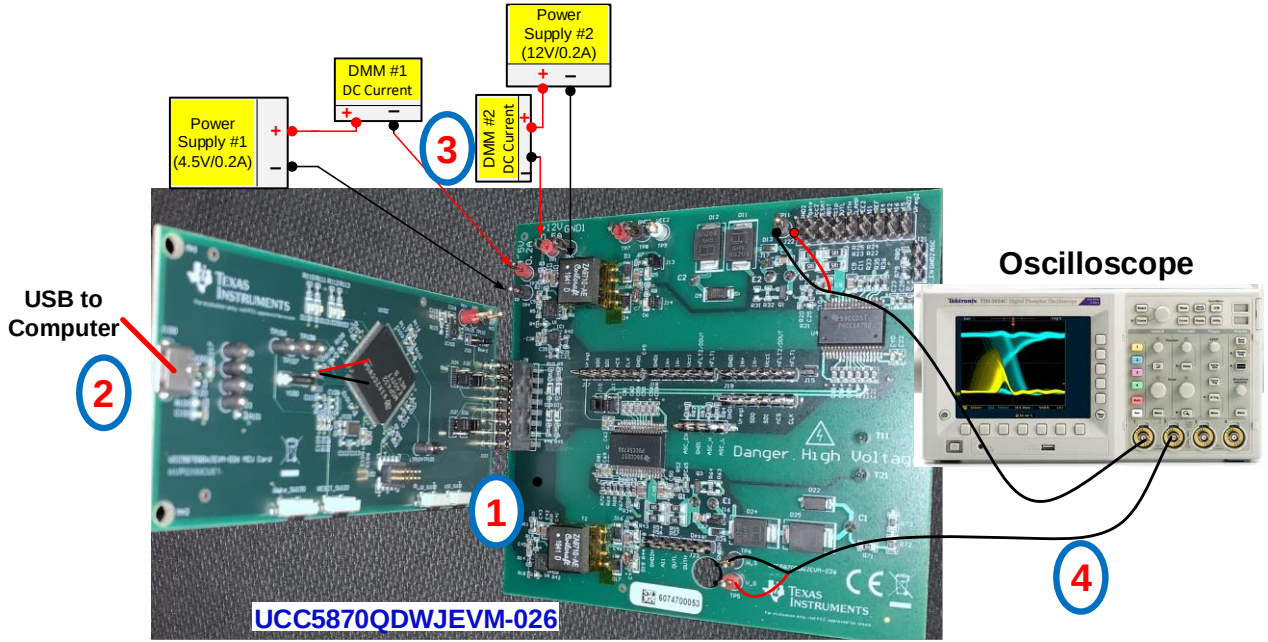




Double Pulse Test Circuit for a Bridge Leg of FS820R08A6P2B IGBT module

EVM link: https://www.ti.com/tool/UCC5870QDWJEVM-026
EVM quickstart demo: https://training.ti.com/ucc5870-q1-evm-quick-start-demo

EVM demo: test system setup

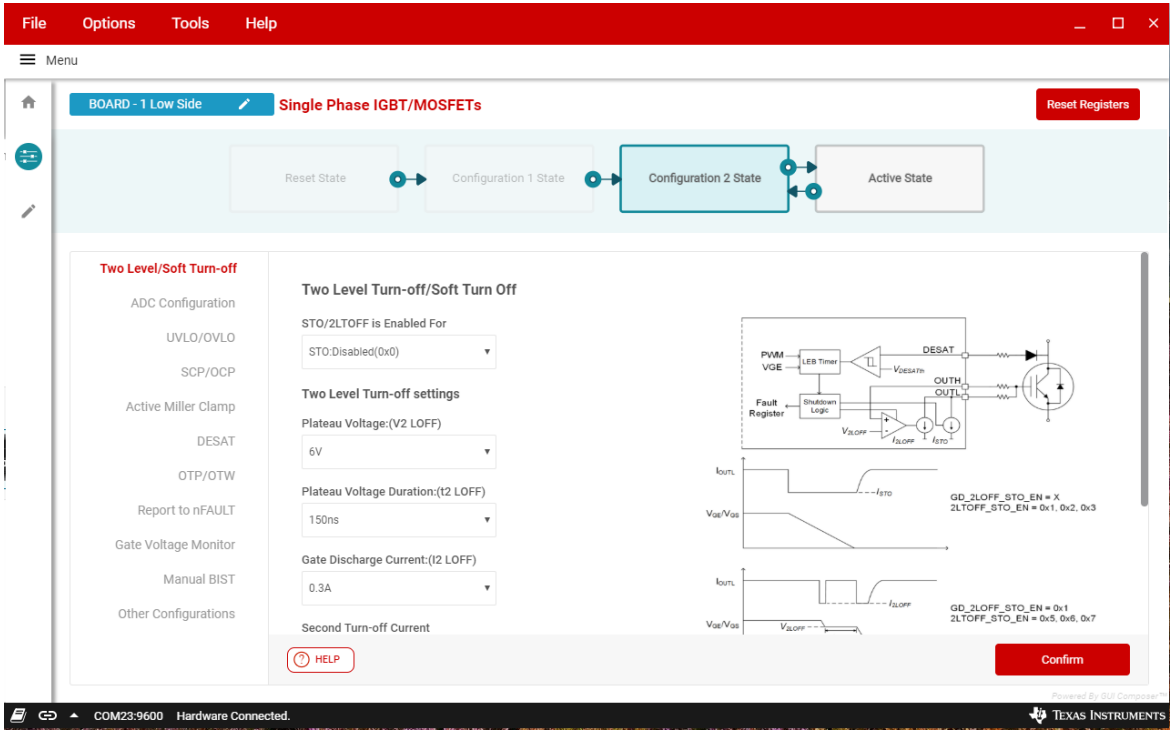


1. Plug in the MCU board, *make sure the side with components is facing the EVM board*
2. Connect the MCU board to computer with the USB cable
3. Connect 12V and 4.5V or 5V power supplies
4. Connect oscilloscope probes, for example, to measure both high side and low side driver Vout

Test system setup for low power test (without connecting IGBT)

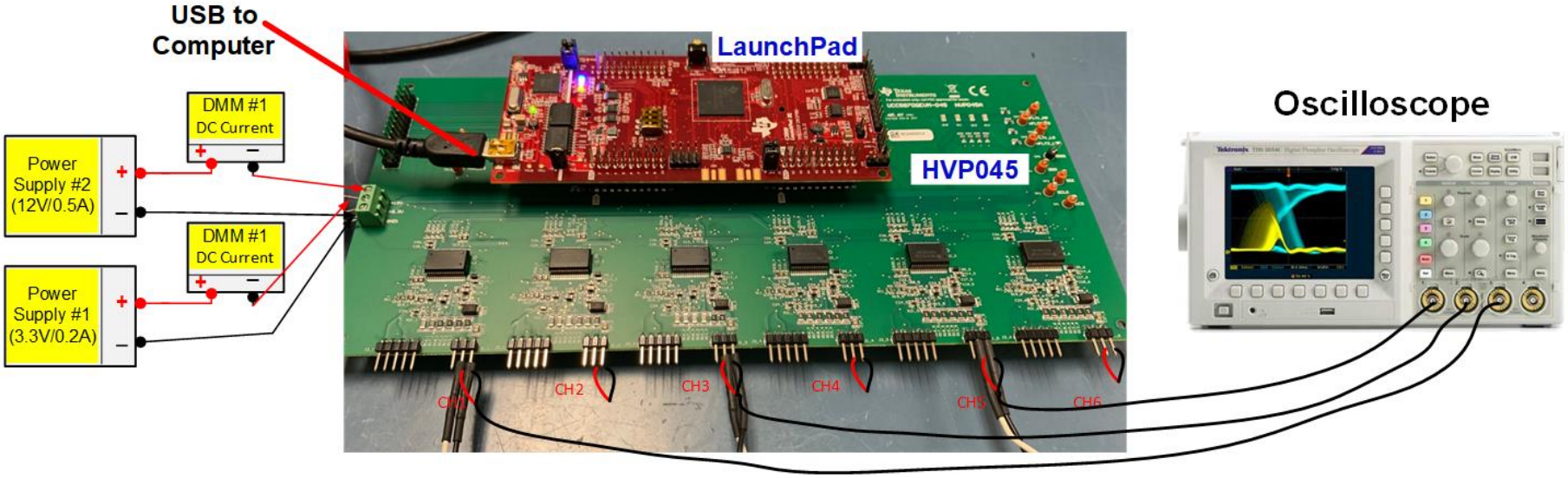
EVM link: https://www.ti.com/tool/UCC5870QDWJEVM-026
EVM quickstart demo: https://training.ti.com/ucc5870-q1-evm-quick-start-demo

EVM demo: GUI



EVM link: https://www.ti.com/tool/UCC5870QDWJEVM-026
EVM quickstart demo: https://training.ti.com/ucc5870-q1-evm-quick-start-demo

EVM demo: three-phase board



EVM link: https://www.ti.com/tool/UCC5870QEVM-045

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