Texas Instruments

HIGH VOLTAGE SEMINAR

WILL HADDEN

ELECTRIC VEHICLES

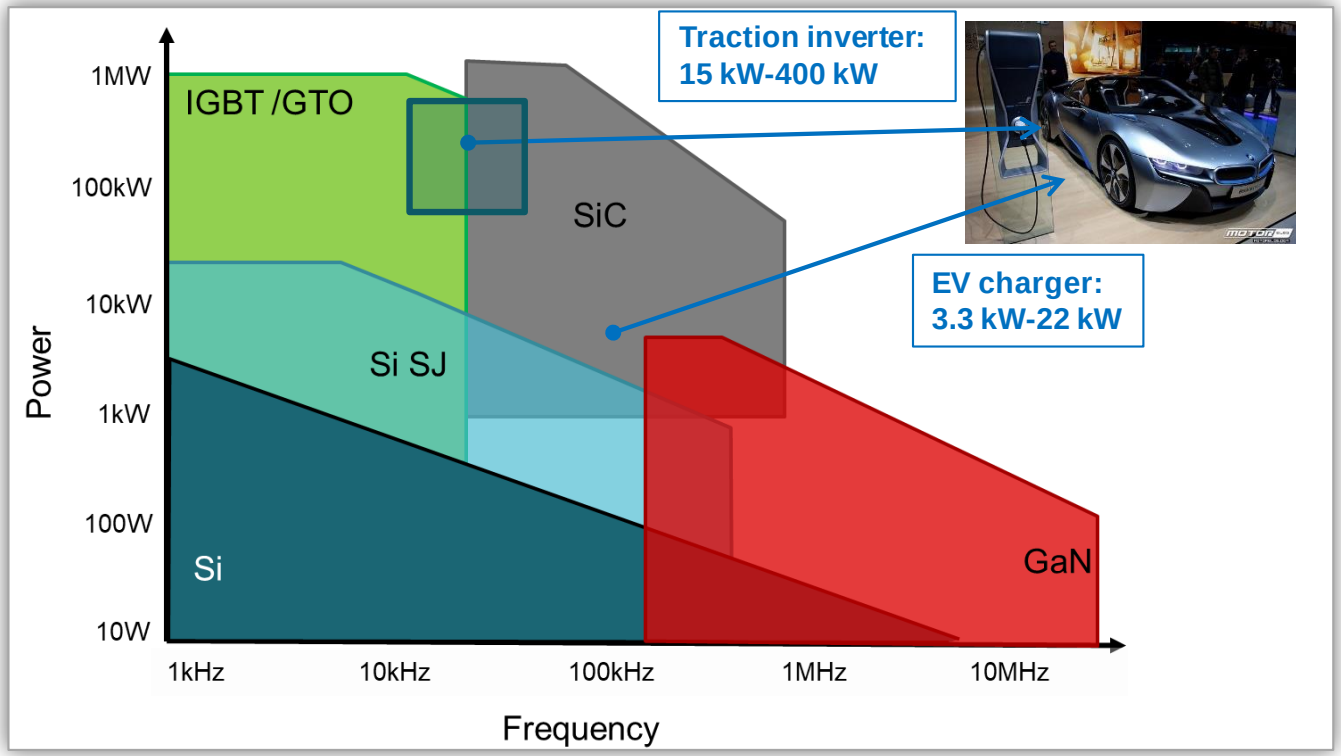
PROTECTING POWER DEVICES IN ELECTRIC VEHICLE APPLICATIONS

What will I get out of this session?

- Brief Description of Silicon Carbide performance
- Different short circuit current sensing and protection methods
- How to turn off MOSFET under short circuit safely
- Other diagnostics available to assist in ASIL designs

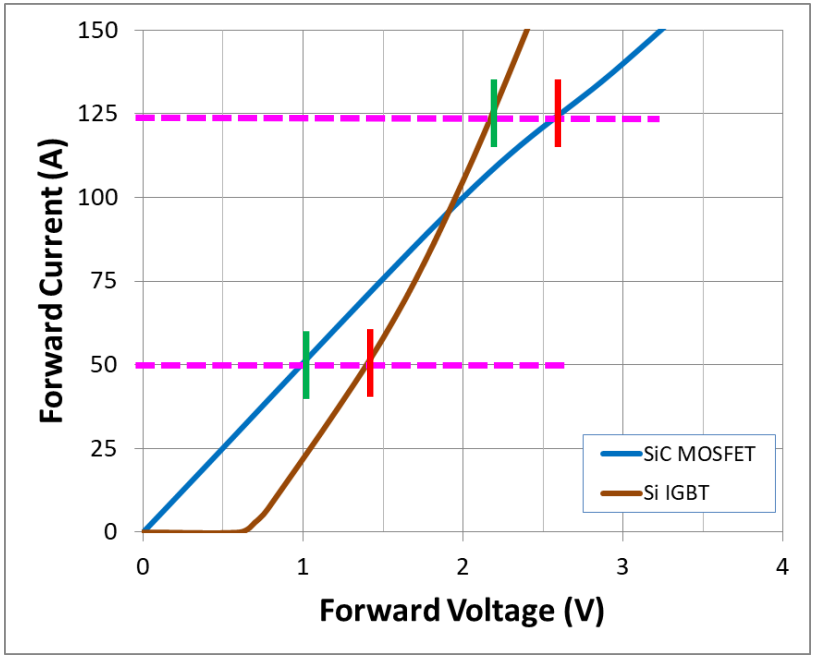
- Relevant part numbers:
  - UCC587x-Q1
  - UCC2152x
- Relevant reference designs:
  - TIDA-01605
  - TIDA-00917
- Relevant applications:
  - HEV/EV traction inverter, EV on-board charger

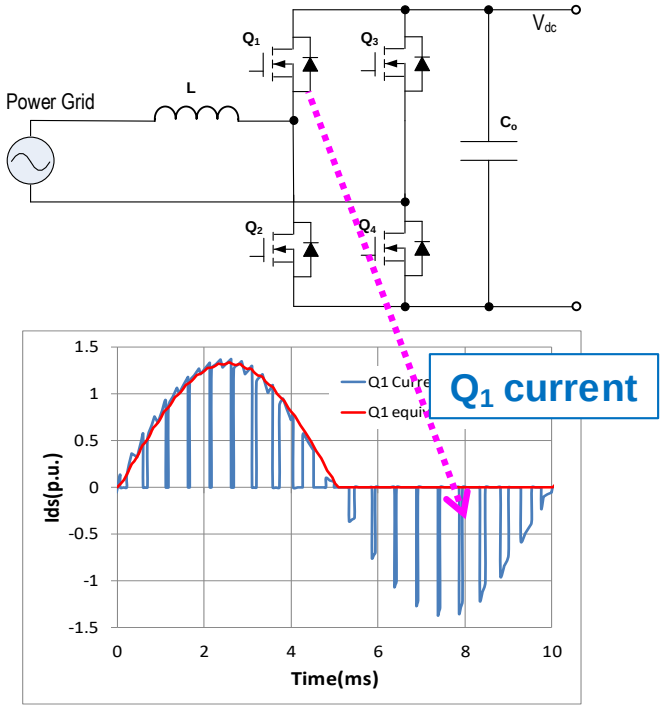
Power transistor application positioning



SiC MOSFET advantages over Si IGBT: conduction

1) No 0.5-1.0V knee voltage; 2) Has "body diode"; 3) 3rd quadrant operation mode





SiC MOSFET advantages over Si IGBT: switching

- **Low switching loss:**

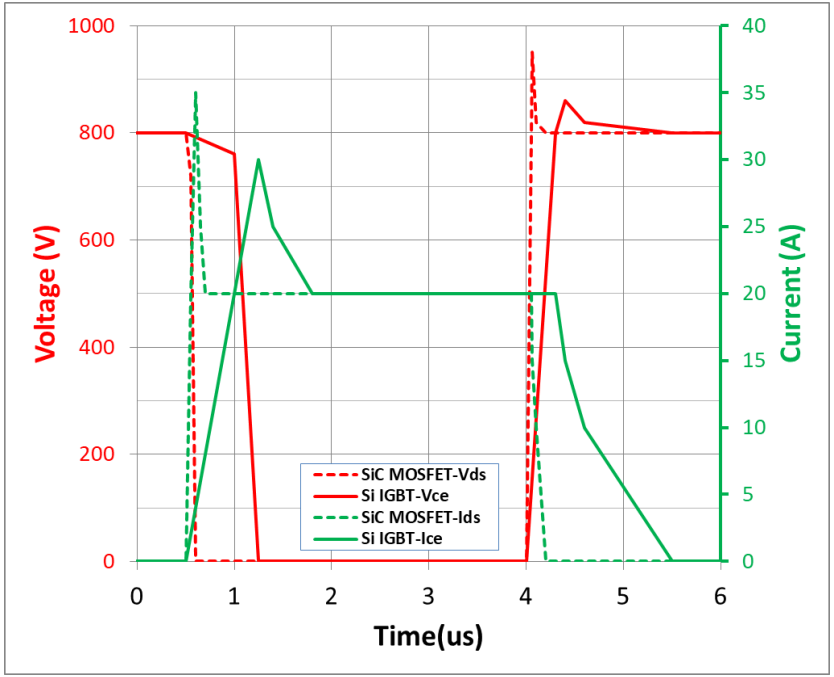
MOSFET (unipolar) vs IGBT (bipolar)- fundamental difference

- **Switch loss less increase at elevated temperatures:**

For 1000V SiC MOSFET, E_{sw}@25˚C = E_{sw}@150˚C

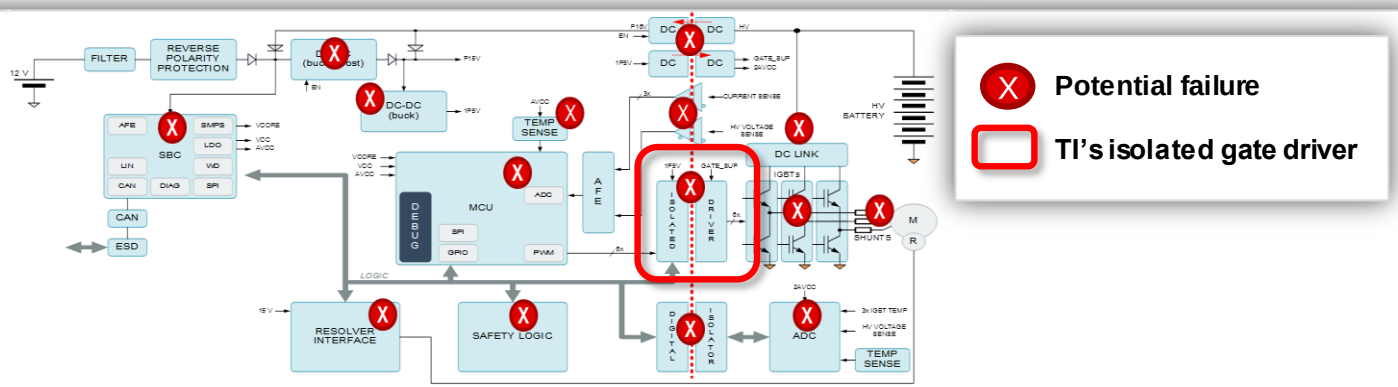
- **Low reverse recovery for the body diode:**

Silicon PiN diode has significant reverse recovery which has reverse recovery loss and also adds more turn on loss



Typical switching waveforms

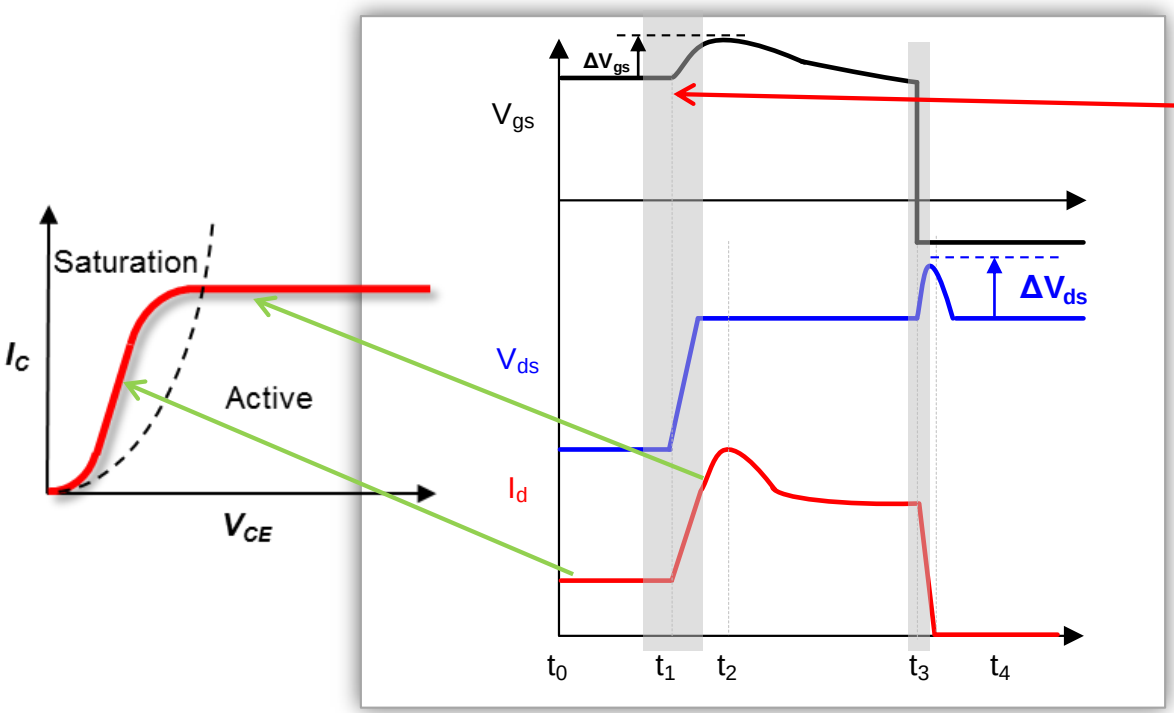
Traction motor: system failure mitigation

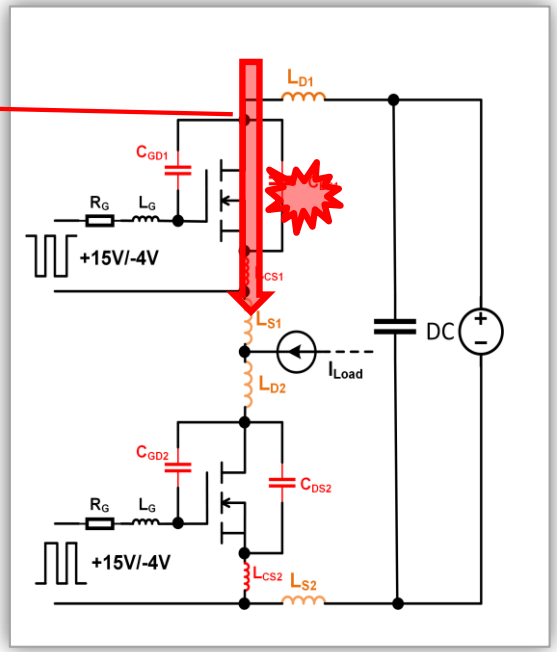


Failure mode	Possible prevention
Motor Coil Shorted/Open	Monitor Current through FET , Shut off Power FET PROTECTION
FET Short/Open/Damaged	Monitor Current through FET, Monitor Gate-Source, Shut off Power FET PROTECTION
Motor Driver Damaged	Monitor Internal signals, Implement Self Test, Disallow operation BIST MONITORS/ DIAGNOSTIC
MCU Failure	Watchdog on Motor driver or PMIC , Reset MCU if WD fails MCU WD
PMIC failure	Watchdog on Motor Driver. Reset MCU if MCU Browns Out PMIC MONITOR
Incorrect IC configuration	Checksum on configuration setups SECURE COMM
MCU Brownout	Monitor PMIC supply independently, Reset MCU for brownout MONITORS/ DIAGNOSTIC
Motor Driver Logic Incorrect	Monitor Gate driver logic voltages, Self test of Gate driver BIST

Overcurrent protection

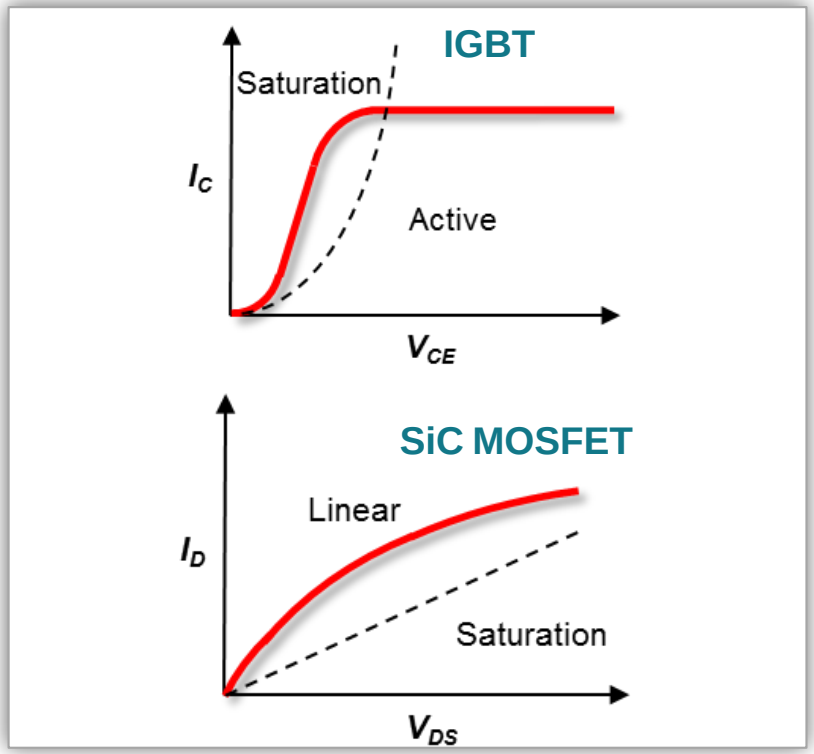
Overcurrent/short circuit fault





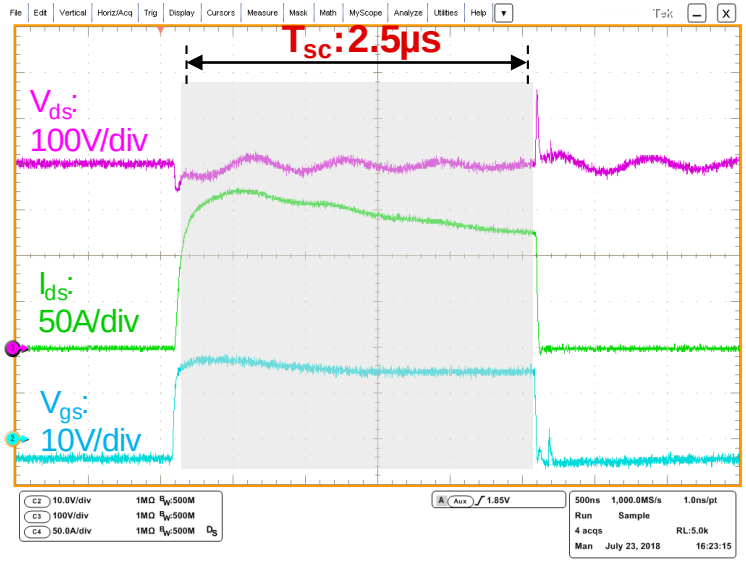
Short circuit happens at t_1

Overcurrent/short circuit fault mechanism: thermal limitation



- ***IGBT self-limits the current increase with lower saturation current***
  - Shape transient from saturation region to active region, collector current is limited to a constant value in active region
- ***SiC MOSFET has large linear region with high saturation current***
  - In the case of SiC, I_d continues to increase with increase in V_{ds}, eventually resulting in faster breakdown
- ***For same rated current & voltage, IGBT reaches active region for significantly lower V_{CE} as compared to SiC MOSFET***

Overcurrent/short circuit fault mechanism: thermal limitation

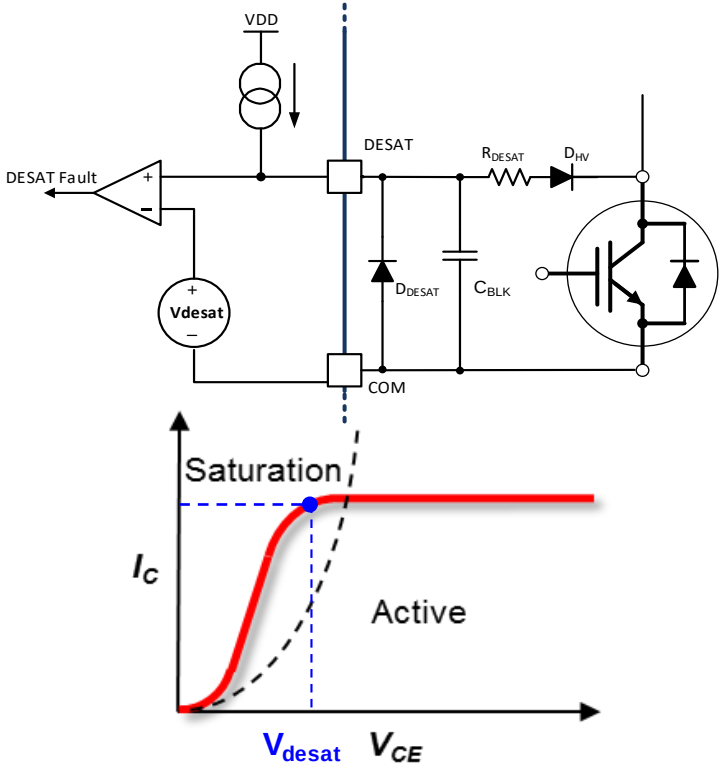


- The short circuit withstand time, t_{sc}, is determined by the critical energy
  - Minimal dissipated energy leading to device failure for one short circuit pulse

$$E_c = \int_{t_1}^{t_3} V_{ds} \cdot I_d \cdot dt$$

  - Vds is the DC link voltage, Id will be the device saturation current.
- SiC MOSFET short circuit withstand time is shorter than IGBT due to smaller chip size, less thermal capacity

Overcurrent/short circuit protection method: DESAT

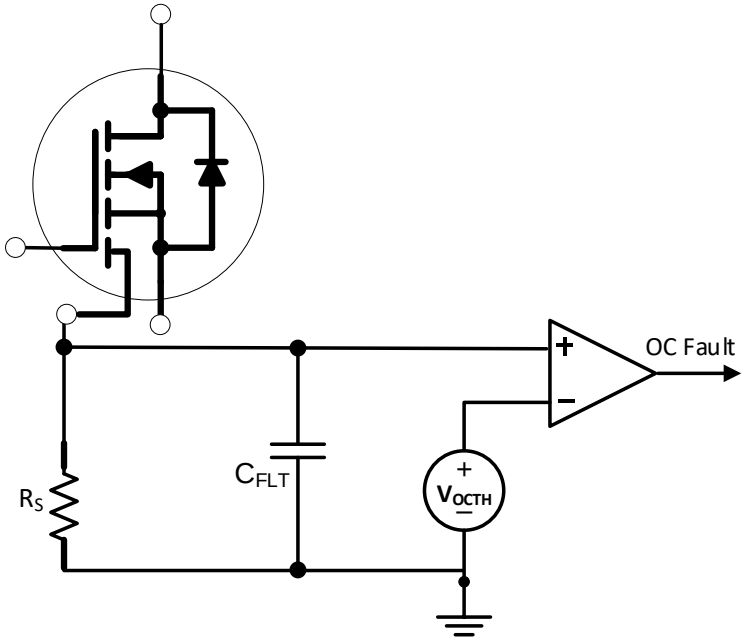


- Desaturation circuit detects the V_{ds} of MOSFET or V_{ce} of IGBT, protection is triggered when detected voltage is above pre-set reference voltage
- Blanking time is needed to prevent false trigger during switching turn on transients

$$t_{DS\_BLK} = \frac{V_{DESAT} \times C_{BLK}}{I_{CHG}}$$

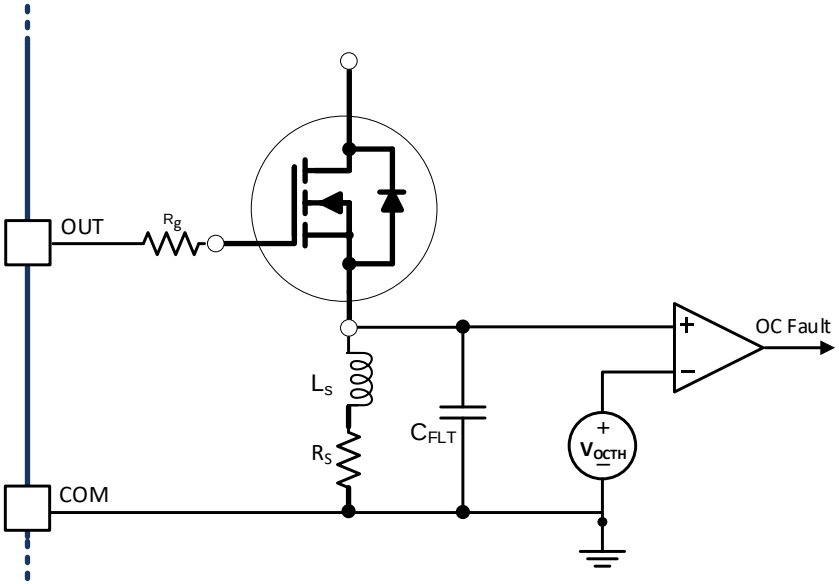
- DESAT threshold voltage varies between different devices due to the output characteristics, especially IGBT and SiC MOSFET
- Most common method for SiC where the IR drop is measured for current sense

Overcurrent/short circuit protection method: SenseFET / current mirror



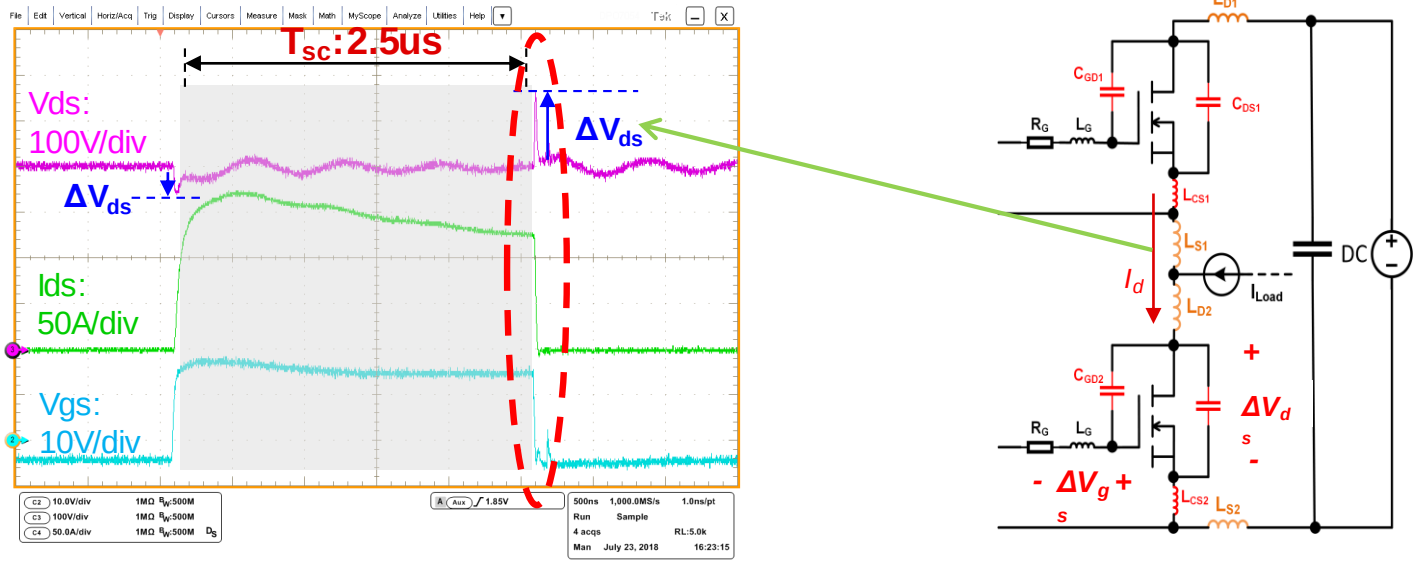
- SenseFET / current mirror is used to scale down main current, tens of mV voltage is measured on sense resistor
- Advantages
  - Fastest protection speed
  - Accurate for both AC and DC
- Challenges of SenseFET / current mirror
  - Module needs to be customized to integrate SenseFET / current mirror
  - Higher cost
  - Not currently available in SiC modules

Overcurrent/short circuit protection method: shunt resistor



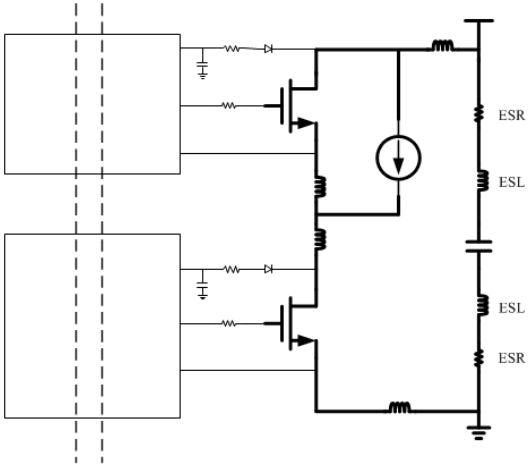
- Advantages
  - Accurate for both AC and DC
  - Fast protection speed
  - Low cost
- Challenges of shunt resistor
  - High power loss in high power applications
  - Weak noise immunity due to gate loop noise caused by parasitic inductance of shunt resistor and PCB trace

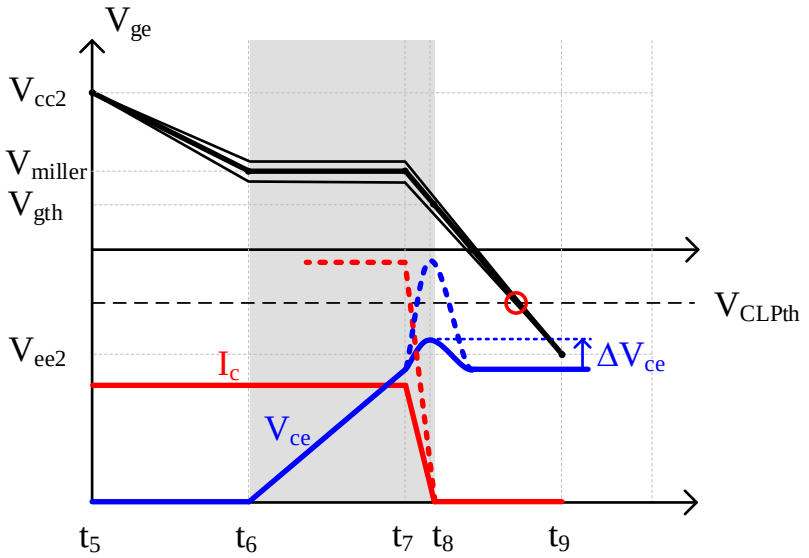
Overcurrent/short circuit safe turn-off: avalanche limitation



- ***Voltage and avalanche limit:*** device avalanche can be caused by the overshoot voltage on V_{ds}

SiC MOSFET protection: soft turn-off (STO) & 2L turn-off

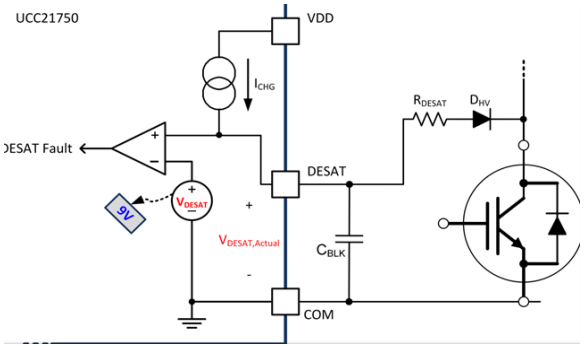


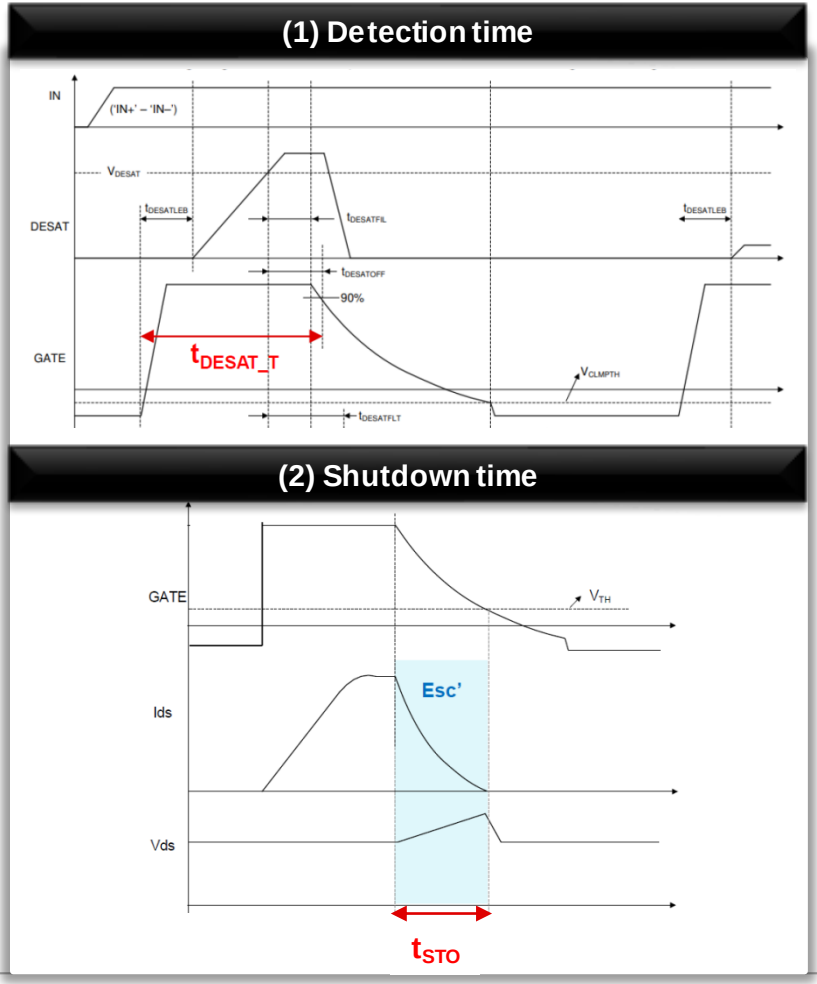


- There are parasitic inductances in the power loop
- Parasitic inductances together with di/dt cause voltage spikes
- The di/dt rate is much higher under short circuit fault so a preventive turn-off measure needs to be taken in order to limit the loop inductance induced voltage spike
- Effectively, there are two ways to slow down the turn-off process: *reduce di* or *extend dt*

DESAT Timing

- Gate Driver Parameters
  - tLEB
  - VDESAT
  - ICHG
  - tDSOFF
  - ISTO
- $t_{BLK} = \frac{C_{BLK} * V_{DESAT}}{I_{CHG}}$
  - Determined by the blanking capacitor C_{BLK}
- $t_{DESAT\_T} = t_{LEB} + t_{BLK} + t_{DSOFF}$
- $t_{STO} = Ciss * (VDD - V_{th}) / I_{STO}$
- $\boldsymbol{t_{Total} = t_{DESAT\_T} + t_{STO}}$

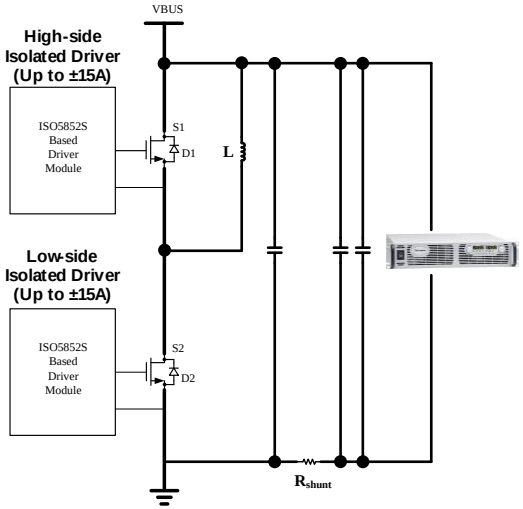


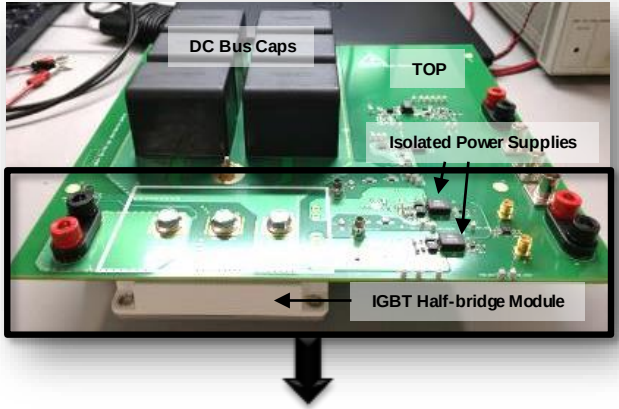


Short-circuit protection: hardware validation

Evaluation hardware

Schematic for double-pulse test setup

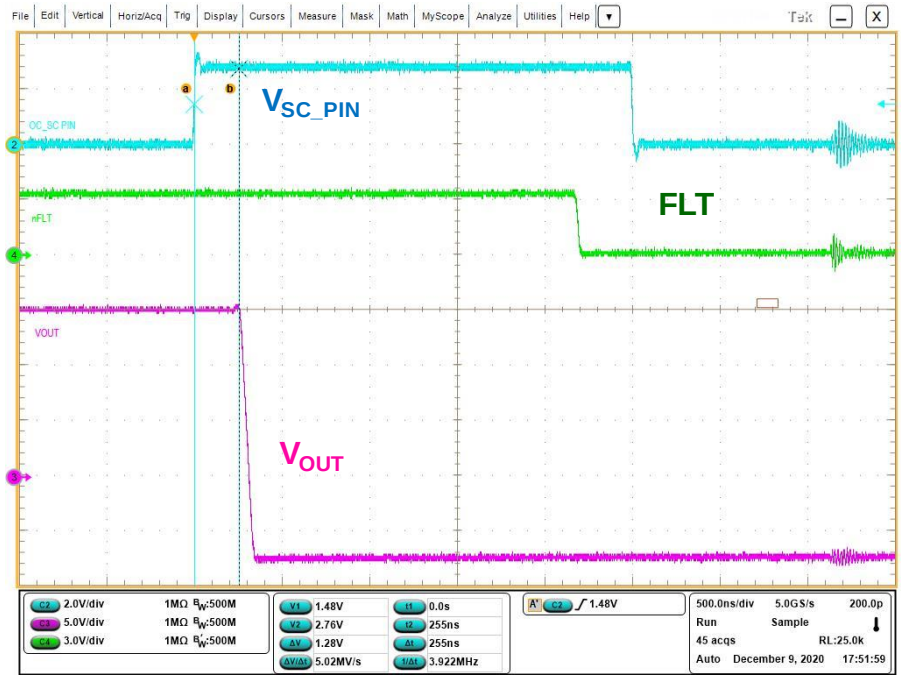




Isolated Half-bridge Drive Stage
using ISO5852S-Q1 + 15A Buffer Driver

SC protection response time

UCC5870-Q1

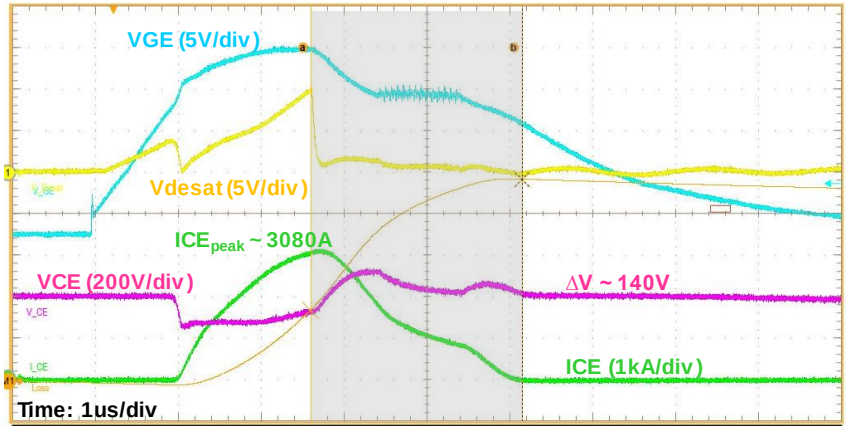


UCC5870-Q1 Response to SC event is 255ns

- The response time incorporates any deglitch and propagation delays in the device
- DESAT and OC features are designed to support SiC requirements, which also covers IGBT applications

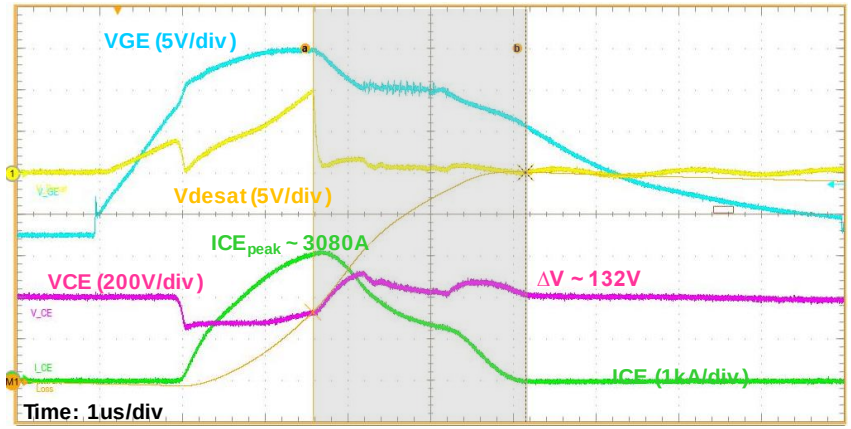
DESAT with Safe Shutdown: 2LTO

Soft Turn-off (STO): I_{STO}=0.3A, V_{2LOFF}=9V, t_{2LOFF}=1.0us



PARAMETER	MEASURED VALUE
Shutdown Energy	1.58J
V_{CE} Overshoot	140V

Soft Turn-off (STO): I_{STO}=0.3A, V_{2LOFF}=10V, t_{2LOFF}=1.0us

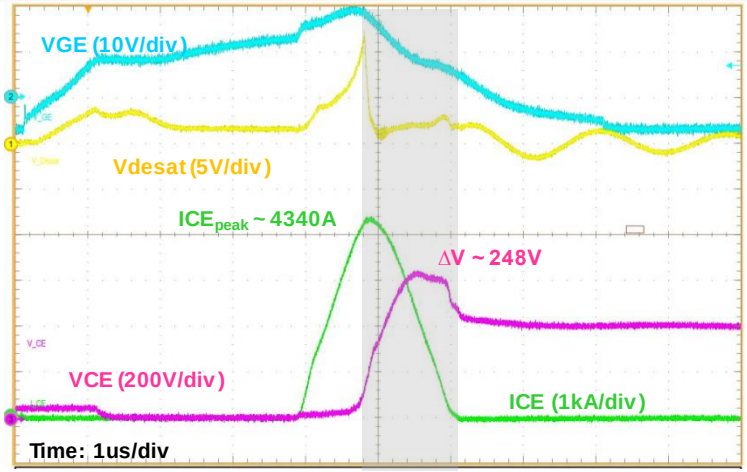


PARAMETER	MEASURED VALUE
Soft Turn Off Current	1.68J
V_{CE} Overshoot	132V

Programmable I_{STO} optimizes for the trade-off between shutdown energy and V_{CE} overshoot for IGBTs/MOSFETs

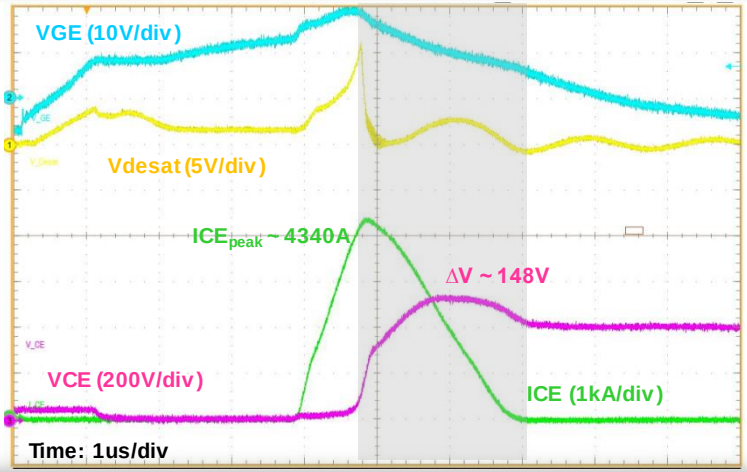
DESAT Response with Safe Shutdown: STO

Soft Turn-off (STO): I_{STO}=0.6A, V_{DESAT_th}=9V



PARAMETER	MEASURED VALUE
Shutdown Energy	1.01J
V_{CE} Overshoot	248V

Soft Turn-off (STO): I_{STO}=0.3A, V_{DESAT_th}=9V

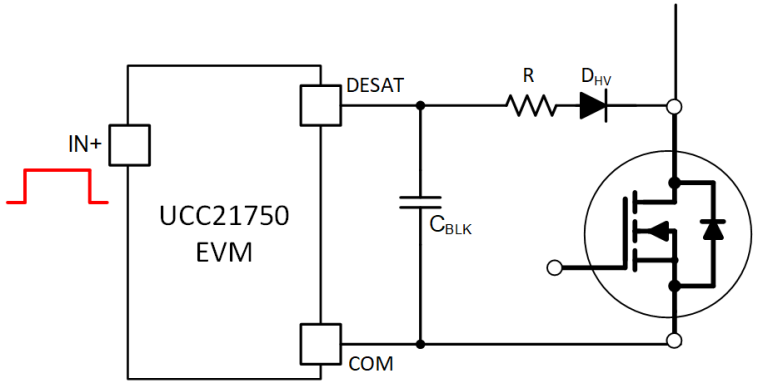


PARAMETER	MEASURED VALUE
Shutdown Energy	2.04J
V_{CE} Overshoot	148V

Programmable I_{STO} optimizes for the trade-off between shutdown energy and V_{CE} overshoot for IGBTs/MOSFETs

SiC with UCC21750: Soft turn-off, VDC=800 V

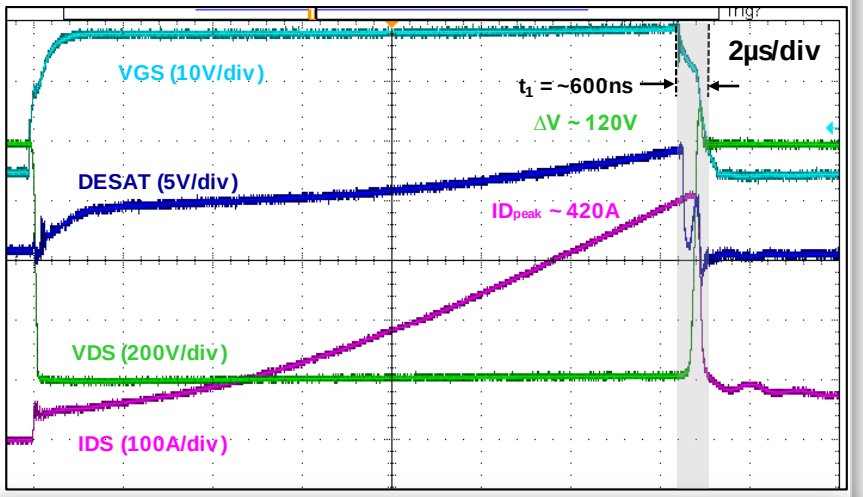
Overcurrent fault test circuit



- IN+ gives a long pulse to create Id ramp
- DESAT detects the fault and takes action

With the same *soft turn-off* characteristics, the only difference in shutdown between the UCC21750 and UCC21750 will be the detection timing

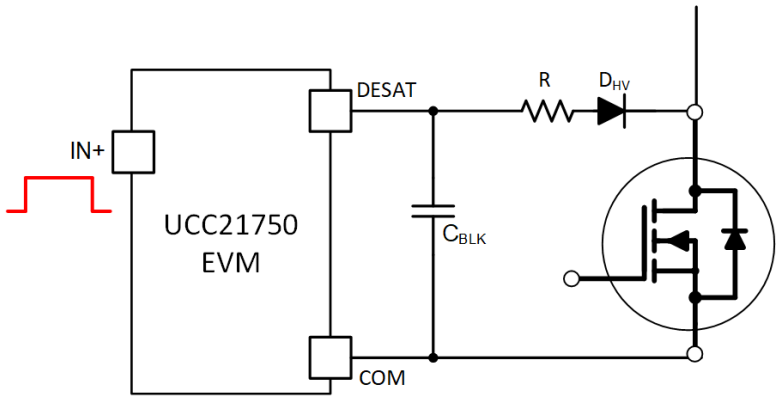
Soft turn-off (STO): UCC21750



PARAMETER	MEASURED VALUE
Shutdown Energy	~0.1J
V_{DS} Overshoot	120V

SiC with UCC21750: Soft turn-off, VDC=800 V

Short circuit fault test circuit



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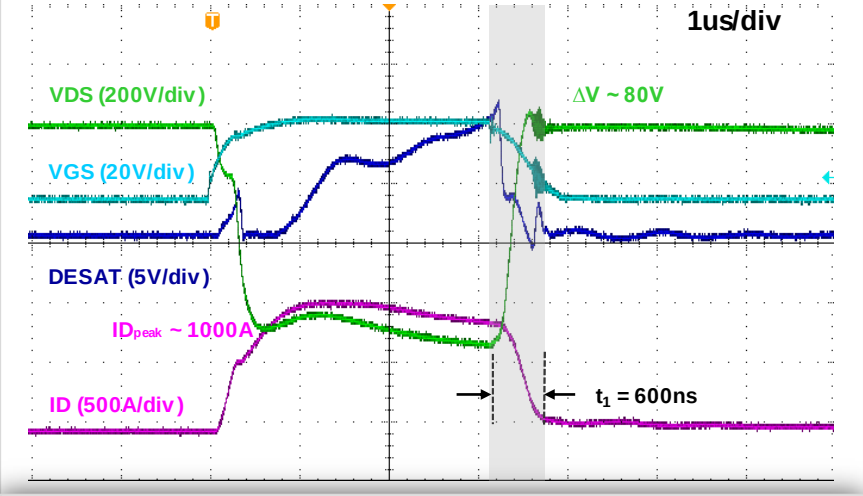
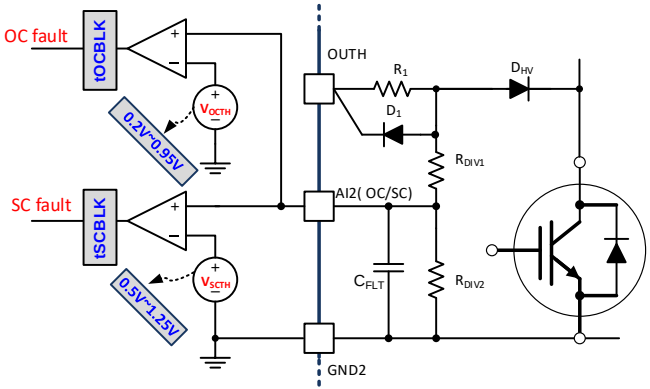
Soft turn-off (STO): UCC21750

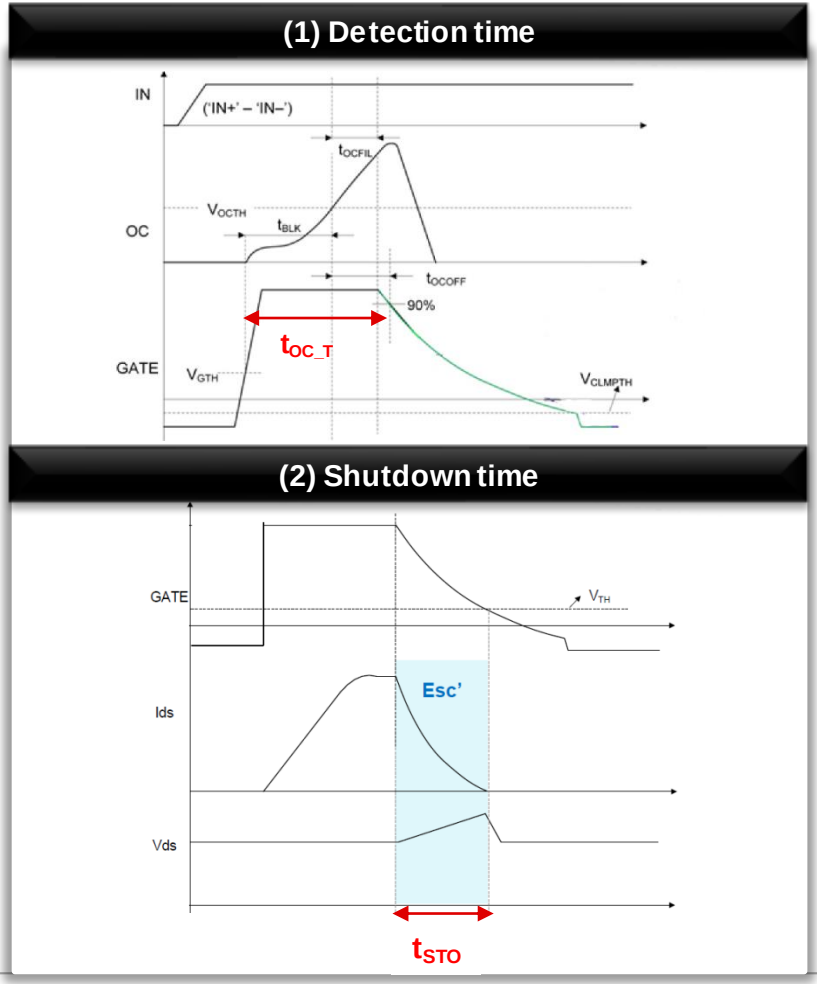


PARAMETER	MEASURED VALUE
Shutdown Energy	0.24J
V_{DS} Overshoot	80V

DESAT using OC

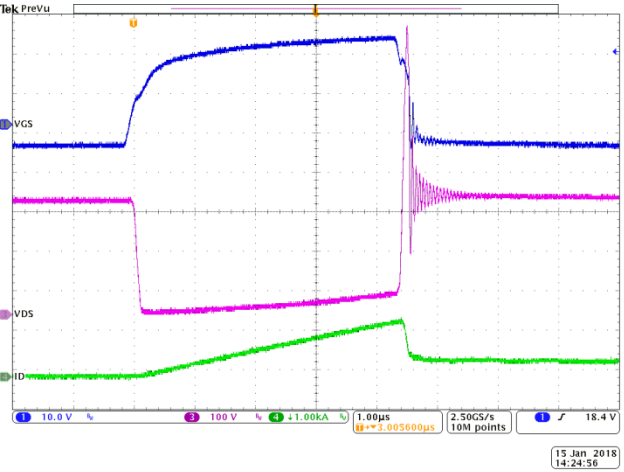
- Gate Driver Parameters
  - VOCTH
  - ICHG
  - tOCOFF
  - ISTO
- $t_{BLK} = -\frac{R1+R2}{R1+R2+R3} * R3 * C1 * \ln\left(1 - \frac{R1+R2+R3}{R3} * \frac{V_{OCTH}}{VDD}\right)$
- $t_{OC\_T} = t_{BLK} + t_{OCOFF}$
- $t_{STO} = Ciss * (VDD - V_{th})/I_{STO}$
- $\boldsymbol{t_{Total} = t_{OC\_T} + t_{STO}}$





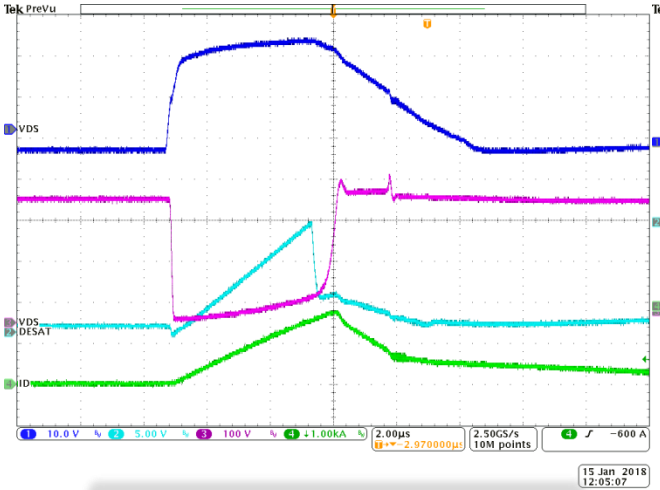
Short circuit protection for SiC MOSFETs: with or without soft turn-off

V_{DS}(100V/div), I_C(1kA/div), V_{GS}(10V/div)



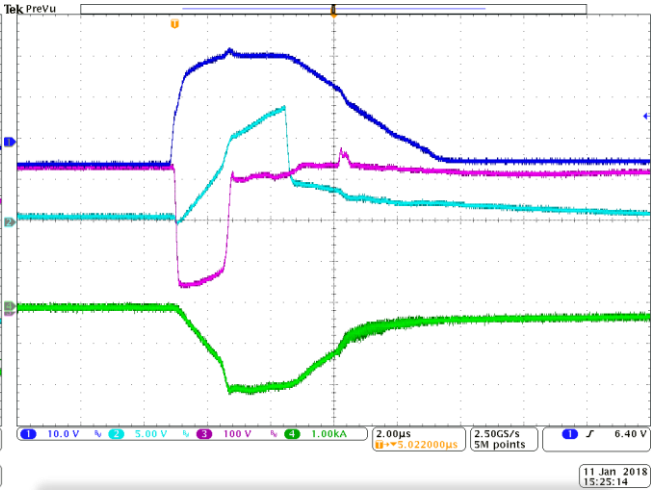
Hard turn-off

V_{DS}(100V/div), I_C(1kA/div), V_{GS}(10V/div), V_{DESAT}(5V/div)



Soft turn-off for hard SC

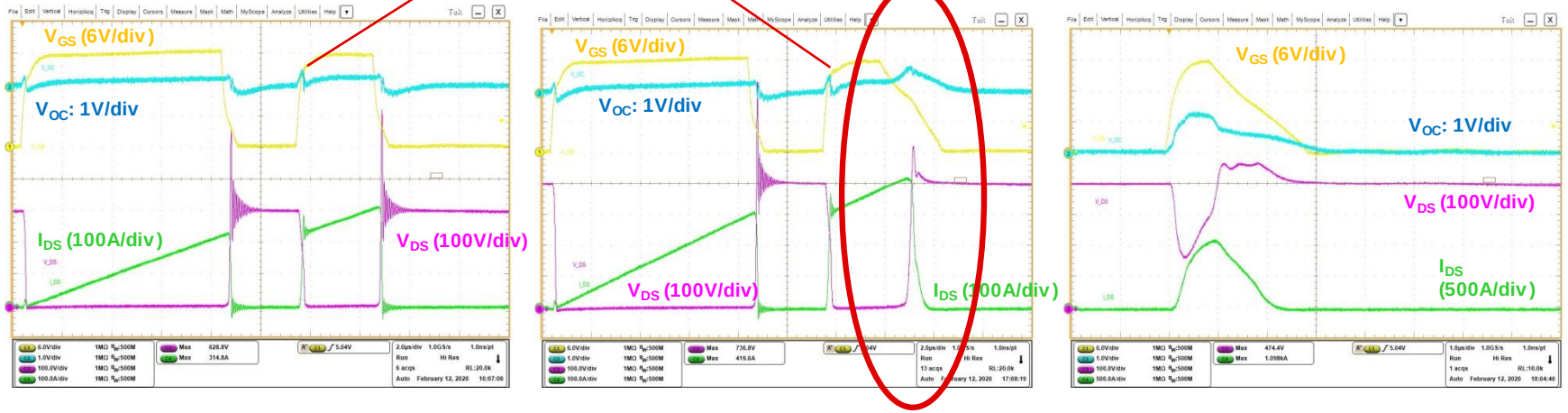
V_{DS}(100V/div), I_C(1kA/div), V_{GS}(10V/div), V_{DESAT}(5V/div)



Soft turn-off for SC under load

OC pin waveform

This noise must be less than the threshold



Normal switching

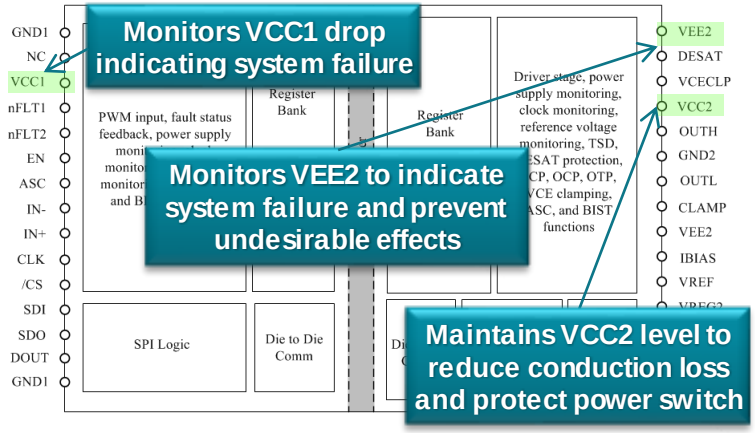
Soft turn-off after OC protection

Soft turn-off after SC protection

Additional protection features

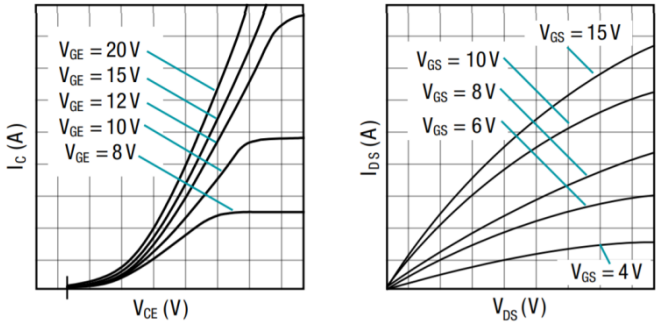
Over and undervoltage lockout: adjustability

System benefits



- ✓ **Flexible Supply Monitoring Across Platforms** : **Programmable OVLO and UVLO** thresholds for primary and secondary supplies
- ✓ **Adjustable to Fit Power Switch Requirements**: Monitor supply voltage to **protect IGBT and SiC MOSFETs** from undue stress
- ✓ **Gather Important Feedback**: **Configurable fault outputs** nFLT1 and nFLT2 to report various faults and warnings

Measurements & specifications



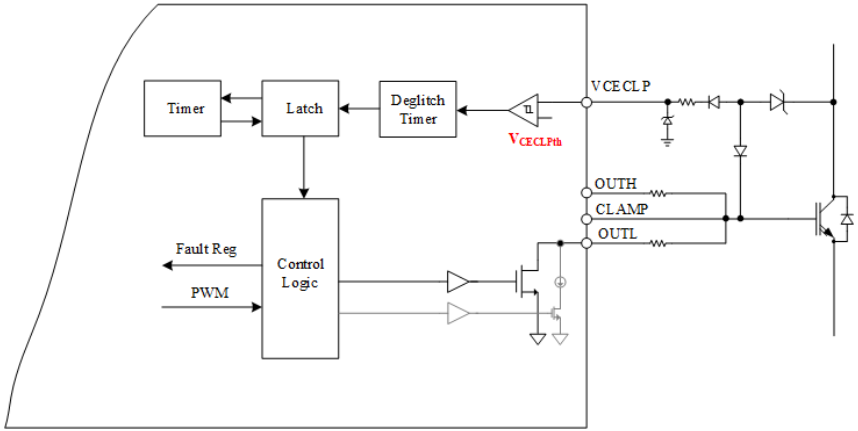
IGBT vs. SiC MOSFET I-V characteristics vary with respect to gate drive voltage (VCC2) and conduction loss

Supply	UVLO Options	OVLO Options
VCC1	3.3V, 5V	3.3V, 5V
VCC2	16V, 14V, 12V, 10V	23V, 21V, 19V, 17V
VEE2	-3V, -5V, -8V, -10V	-5V, -7V, -10V, -12V

Thresholds can be optimized based on gate voltage of power switch!

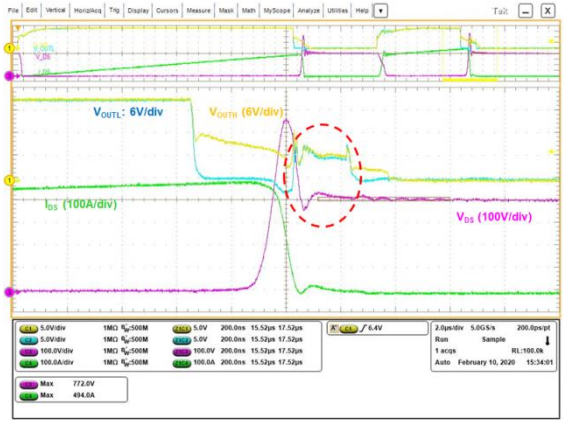
V_{CE} clamp: flexibility, protection

System benefits



- ✓ **System Flexibility:** Option between **3 communication modes** (address-based, daisy-chain, regular SPI)
- ✓ **Ease of System Programmability**: Simplify design time and engineering effort
- ✓ **Address-based SPI:** Only requires **4 I/O pins** and provides **6x shorter response time** compared to daisy chain configuration

Measurements & specifications

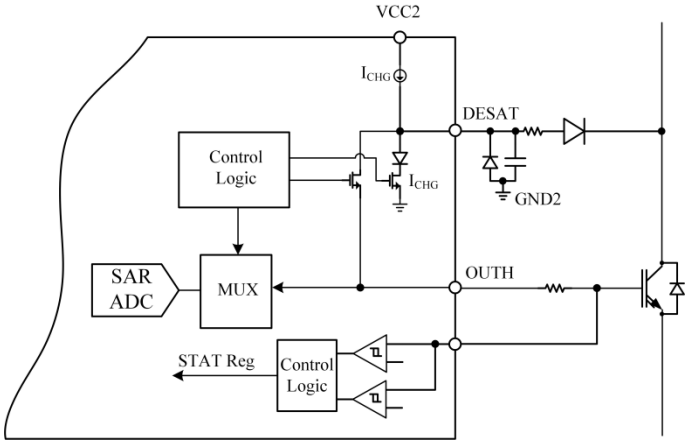


UCC5870-Q1 V_{CE} Clamp Characteristics		Typ. Value
V_{CE} Clamp Threshold	$V_{CECLPTH}$	2.2 V
V_{CE} Clamp Threshold Hysteresis	$V_{CECLPHYS}$	200 mV
V_{CE} Clamping Intervention Time	t_{VCECLP}	20 ns
V_{CE} Clamping Hold Time	t_{VCECLP_HLD}	Adjustable

High voltage clamping only active for a short time to prevent shoot-through

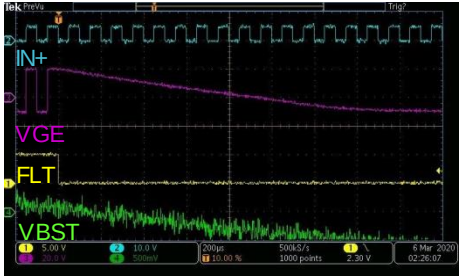
Gate voltage monitoring: flexibility, protection

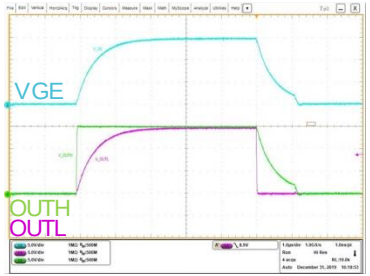
System benefits



- ✓ **Enhanced System Safety:** Ensure output follows the driver input as high or low to **detect a system failure** such as open resistor at gate or gate short
- ✓ **Real-Time Fault Monitoring:** **Dedicated fault output** to feed information back to MCU
- ✓ **Size Reduction:** **Removes external components** to monitor driver output voltage

Measurements & specifications



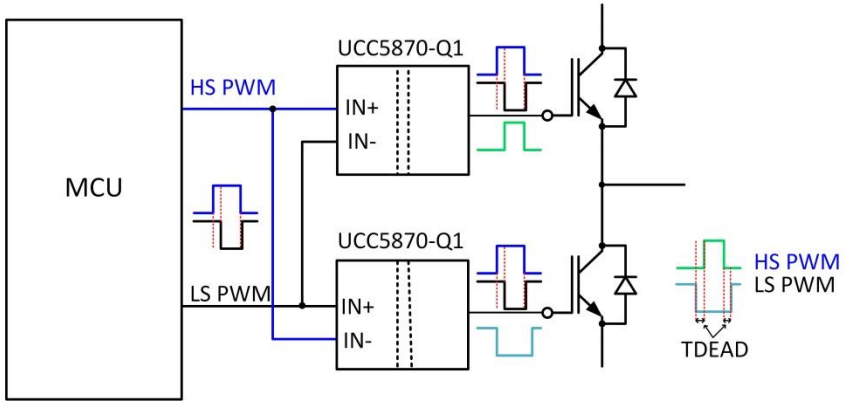


- ✓ VBST voltage drop triggers Gate Voltage Monitor Fault
- ✓ When Gate Voltage Monitor Fault is detected, the output is turned off

UCC5870-Q1 Gate Voltage Monitor Characteristics	Typ. Value
Gate Voltage Monitor Threshold Value (reference to V_{CC2})	-3 V
Gate Voltage Monitor Threshold Value (reference to V_{EE2})	3 V
Blanking Time (Programmable)	500-4000 ns
Deglitch Time	250 ns
Fault can be reported to nFLT1 or nFLT2, or report to state to nFLT2	

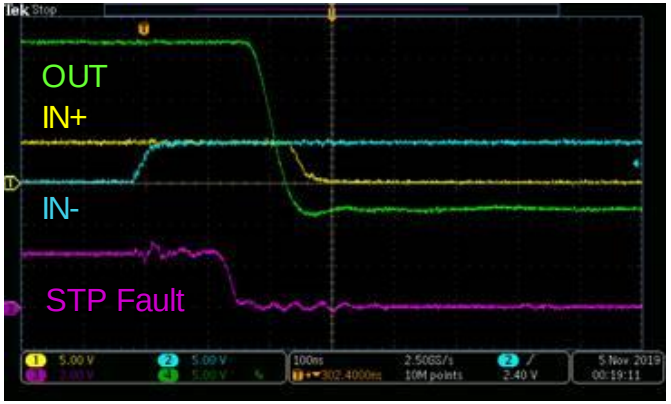
Motor controller interface: flexibility, protection

System benefits



- ✓ **System Flexibility:** Supports **100% duty cycle** operation (min 250ns input pulse, 30 kHz max frequency with ADC)
- ✓ **Shoot-through Protection:** Interlocking with two drivers prevents shoot-through with **programmable dead time** and **fault reporting**
- ✓ **Noise Immunity:** Minimum **pulse width rejection** on IN+ and IN-

Measurements & specifications

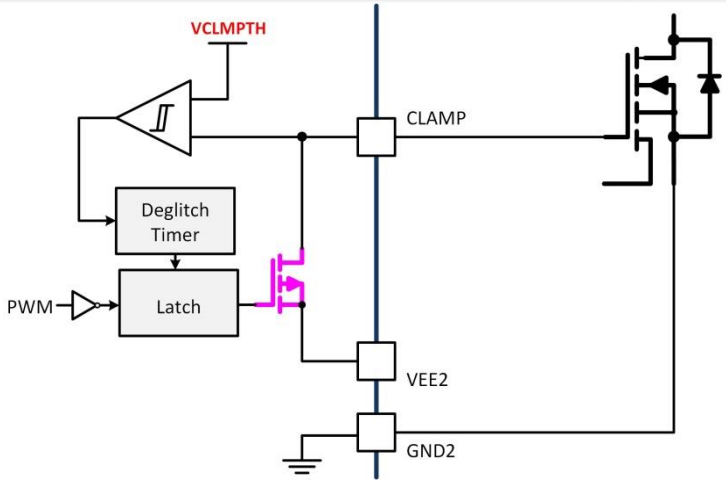


Shoot-through prevented and STP Fault triggered

- ✓ **100% Duty Cycle** possible with integrated charge pump
- ✓ **Programmable dead time**: 0ns, 105ns, 175ns…up to 4445ns in increments of 70ns
- ✓ **Noise rejection** chosen based on programming input pulse width rejection ranging from **0ns** to **210ns**

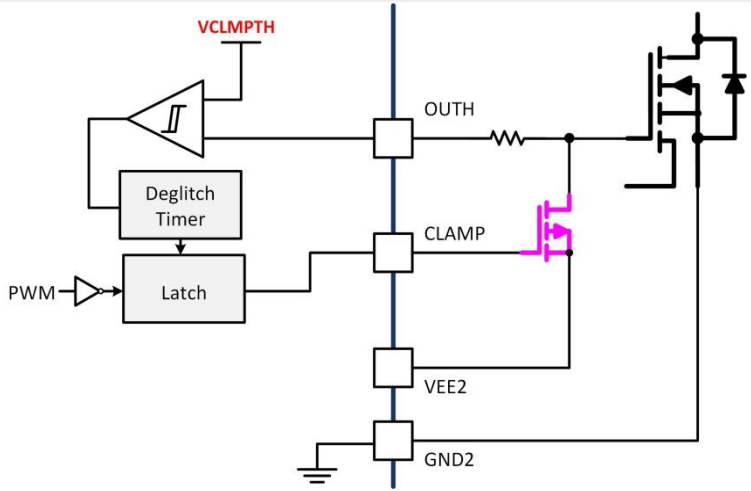
Active Miller Clamp

Internal Miller Clamp



- Miller Clamp **inside** IC
- **5A** peak pull-down current
- Adjustable VCLMPTH (1.5V, 2V, 3V, or 4V)
- Suitable for close connection of CLAMP pin to gate terminal of power switch
- System challenges when connection from CLAMP pin to Gate terminal of power switch is too long (high inductance)

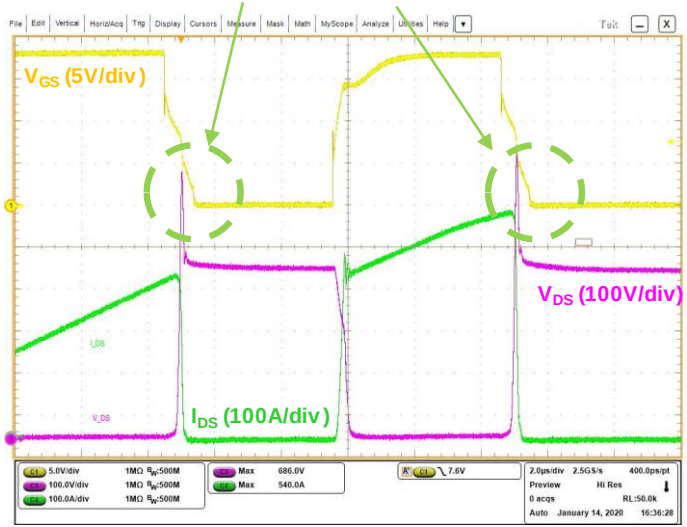
External Miller Clamp

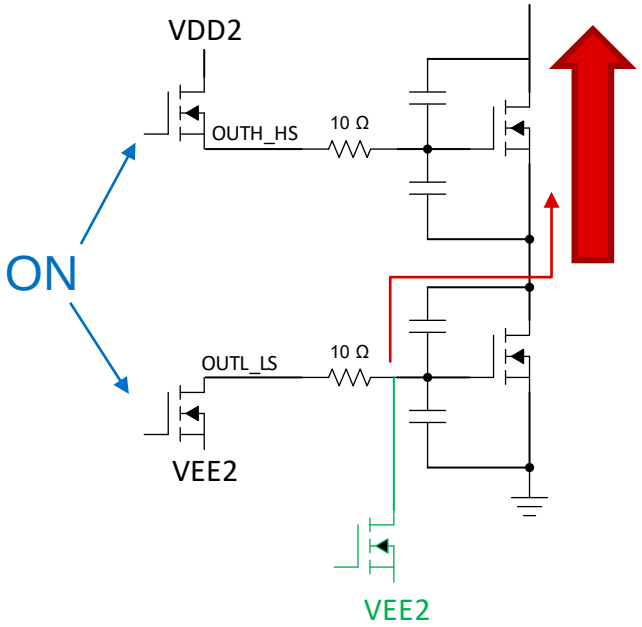


- Miller Clamp **outside** IC: Discrete Si MOSFET switch
- **Flexible peak pull-down current** +5V signal w.r.t. VEE2 @ CLAMP pin
- Adjustable VCLMPTH (1.5V, 2V, 3V, or 4V)
- Suitable when CLAMP pin is far away from gate terminal of power switch
  ⇒ Low inductance from clamp to gate terminal of power switch
- Better technique for power module implementation

Active Miller Clamping

Miller clamp kicks in an pulls the gate to VEE with a low impedance path

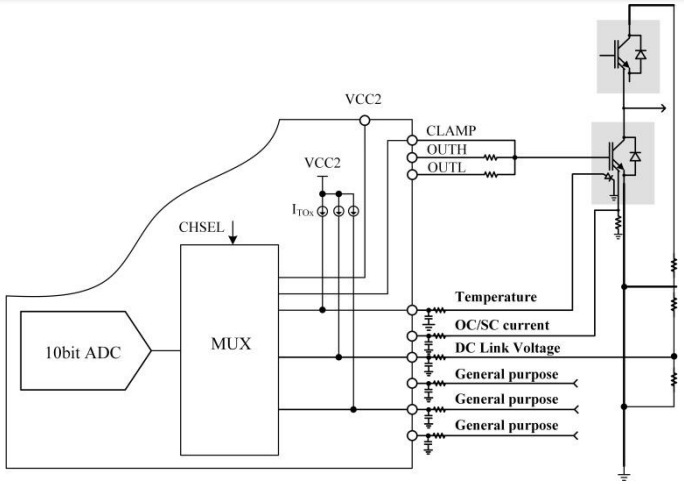




As the SW node rapidly changes, coupling can turn on the External power FETs through the parasitic coupling

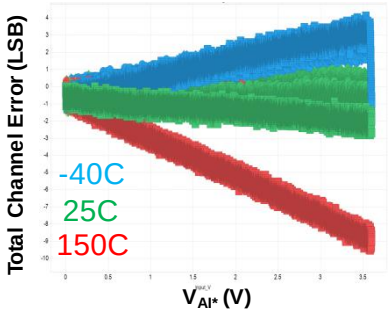
6-channel ADC: accuracy, integration, low noise

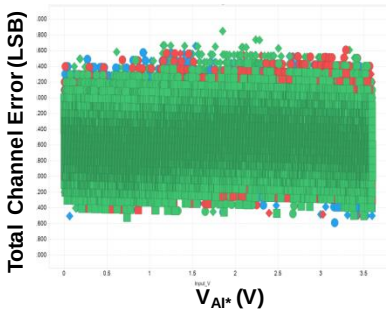
System benefits



- ✓ **System Flexibility:** Variety of configurations to measure **temperature, current, or voltage**
- ✓ **Higher Accuracy:** Integrated **10-bit** ADC and internal OR external **VREF**
- ✓ **System Cost/Size Reduction:** Save **~$0.37** per channel by eliminating external ADC

Measurements & specifications



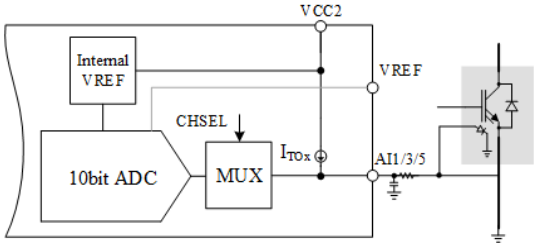


Precision reference can measure AI to within +1/-2 LSB (+3.5/-7 mV)*

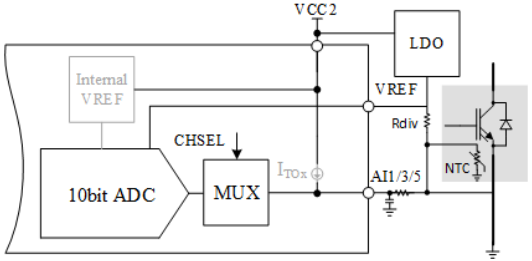
ADC	MIN	TYP	MAX
Input Voltage Range (A1 to A6)	0V	3.6V	3.636V
VREF (V)		4	
INL, external ref (LSB)	-1.2		1.2
DNL (LSB)	-0.75		0.75
External ADC Reference Turn-On Delay (us)	10		
NTC bias current (prog range, uA)	100		1000

6-channel ADC: use cases

Isolated switch temperature sensing: NTC/PTC/diode



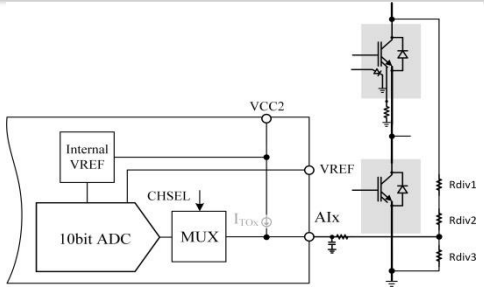
Example using thermal diode + internal VREF



Example using thermal diode + external VREF

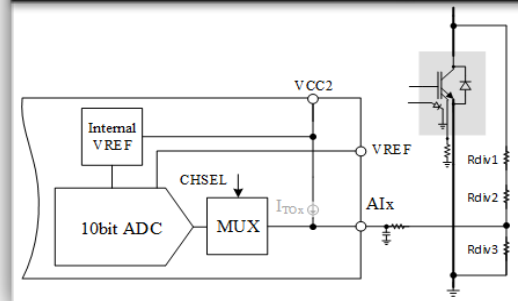
- Power switch junction temperature monitoring
- Power switch over-temperature configurable warning and shut-down
- Option for internal or external VREF to improve accuracy

Redundant Bus voltage measurement



- HV Bus Sensing
- Monitor DC link voltage
- Referenced to low-side driver common

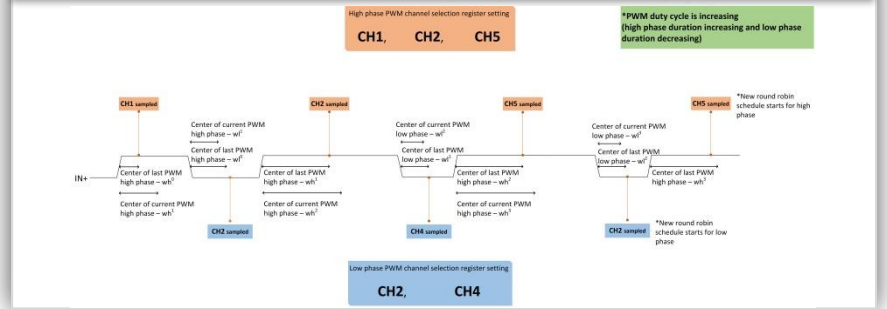
VCE voltage measurement



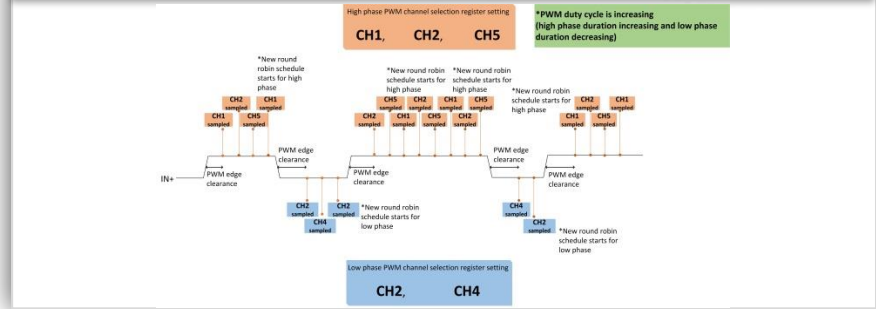
- HV VCE Sensing
- Monitor if phase open or closed
- Option to reference to high-side or low-side common

6-channel ADC: sampling modes

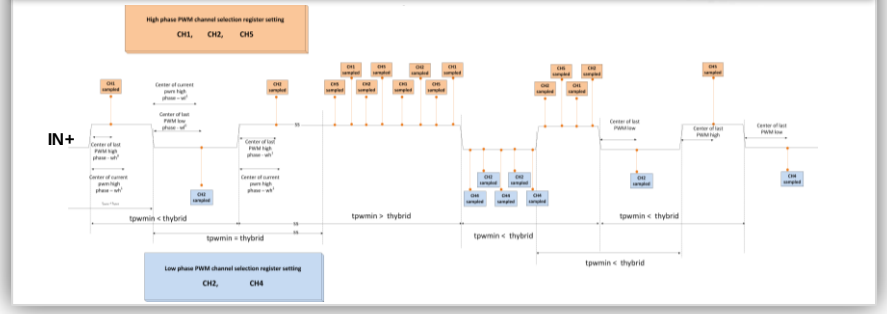
Center sampling mode



Edge sampling mode



Hybrid mode



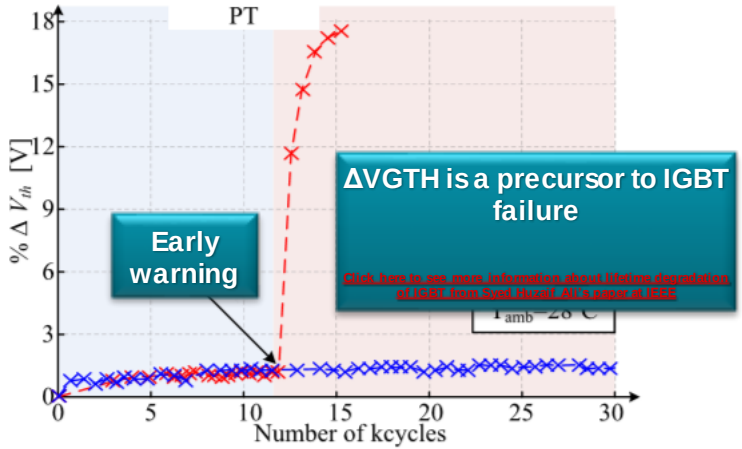
Configuring ADC modes

- Three modes available to ensure least amount of switching noise
- **Center sampling mode:** samples in middle of switching cycle
- **Edge sampling mode:** samples at start or end of each switching cycle
- **Hybrid sampling mode:** samples mode samples in the center until a cycle is significantly longer then the one before it

Power Switch V_{GTH} Monitor: System Reliability

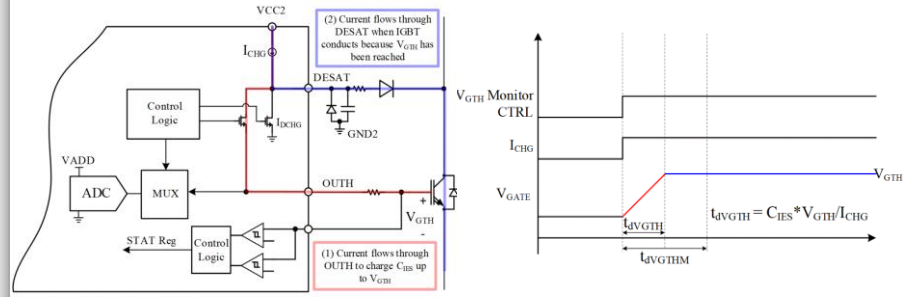
TI Unique Feature

System Benefits

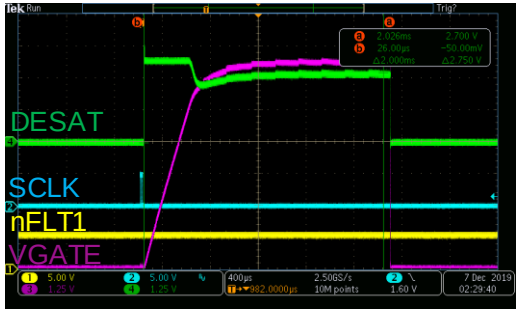


- ✓ **Integrated Health Monitor:** Gate driver used to perform **threshold voltage measurements** over system lifetime
- ✓ **Help System Anticipate Failure**: Works with MCU to provide **critical power switch data**

Measurements & Specifications



Operation of VGTH monitor and timing diagram



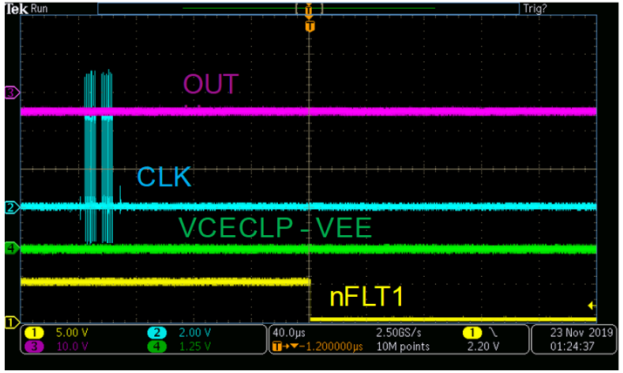
VGTH is accurate measure of health of external power switch

Test done with Cree SiC MOSFET C3M0065100K with voltage threshold of 1.8-3V

Built-in self-test (BIST): enhanced reliability

BIST (built-in self test) mechanisms	
UV/OV Comparators of **Internal Regulator**	Automatic on Power Up (Latent Fail Check)
UV/OV Comparators **(VCC1, VCC2, VEE2)**	Automatic on Power Up (Latent Fail Check)
Main **Clock**	Automatic on Power Up (Latent Fail Check)
Comparator for **Thermal Shutdown**	Automatic on Power Up (Latent Fail Check)
DESAT diagnostic	On-Demand (with SPI Command)
OCP, SCP and OTP comparator diagnostics	On-Demand (with SPI Command)
VCE clamping detection diagnostics	On-Demand (with SPI Command)
Gate Monitoring	On-Demand (with SPI Command)
CRC	On-Demand (with SPI Command)

Example & benefits

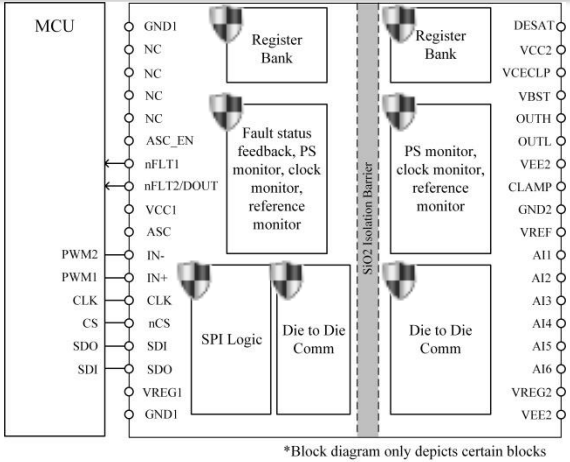


SPI command sent to check VCE Clamp and fault reported showing functioning detection mechanism

- ✓ **System and On-Demand Diagnostics:** Ensures operation of critical driver functions **at power up** and **on-demand** using SPI programming
- ✓ **Enables Easier ASIL-D Implementation**: Integrated diagnostics to **support system-level functional safety** requirements

Other diagnostics and protection: reliability and flexibility

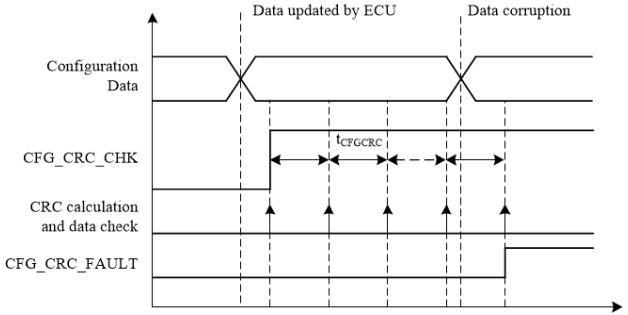
System benefits



*Block diagram only depicts certain blocks

- ✓ **Data Protection:** **CRC (cyclic redundancy check)** protects various registers against faulty data transmission when in the Active State
- ✓ **Communication Protection**: CRC checks for SPI transfer are **continuously updated** as SPI data is sent/received
- ✓ **Flexible Feedback**: **Configurable fault outputs** nFLT1 and nFLT2 to report various faults and warnings

Measurements & specifications



Configuration Data CRC Check Timing

- ✓ When the driver is in the ACTIVE state, the configuration and control registers are protected by the CRC engine (this can be disabled)
- ✓ An error can be induced on the primary or secondary side
- ✓ CRC checks on SPI transfers are continuously updated as traffic is sent/received and is updated with every 16-bits that are received

See the datasheet Detailed Description section for more information

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