Application Report
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TRF3765 Synthesizer Lock Time

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ABSTRACT

PLL lock time is an important metric in many synthesizer applications. Because the TRF3765 uses multiple VCOs and digitally switched capacitor banks to achieve extremely wideband operation, PLL lock is a two-step process of switching to the proper digital setting followed by analog frequency lock. This wideband operation along with digital frequency band selection requires a different set of timing metrics than traditional narrow-step and wide-step PLL lock-time measurements. This document describes the digital band select timing and provides detailed analog lock time measurements. The worst-case digital band select time is 15 µs, and typical analog lock time is 60 µs.

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1 Interaction of PLL Frequency Lock Steps

Frequencies in the TRF3765 are programmed by setting register bits through the four-wire interface (4WI). Divider programming is followed by initiating a calibration, again through the 4WI. The PLL lock process takes place in two steps. First, the PLL is unlocked while the device performs a digital search. Second, the analog PLL elements are allowed to converge on the desired frequency. The second step is familiar to PLL users as lock time, although it is affected by the initial conditions as determined by the digital settings. Figure 1 shows how the lock-detect indicator, LD, remains low through both steps until VTUNE has approached its steady-state value. 4WI write access times are below 5 µs and are not addressed in this report.

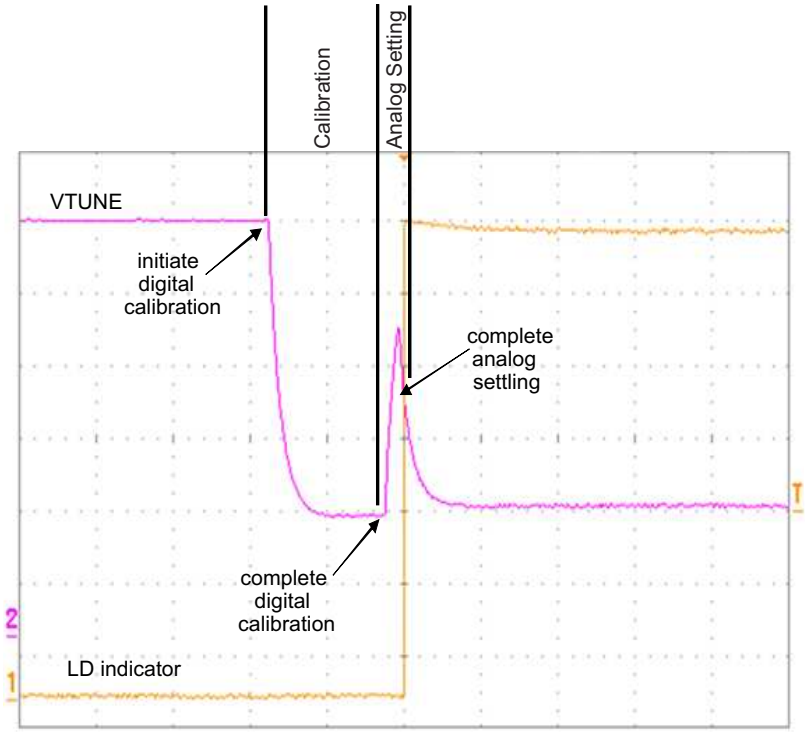

Figure 1. Lock Detect Remains Low During Two-Step, Frequency-Change Process

2 Digital Calibration

2.1 Structure of Digital Frequency-Select Elements

Wideband synthesizer operation from 300 MHz to 4800 MHz is achieved by using a combination of output frequency dividers, multiple integrated VCOs, and digitally switched capacitor banks. The fundamental frequency range of the VCOs extends in a contiguous band from 2400 MHz to 4800 MHz, then output frequency dividers operating in powers of 2 create frequency bands from 1200 MHz to 2400 MHz, 600 MHz to 1200 MHz, and 300 MHz to 600 MHz. This fundamental band represents a 100% range, too broad for a single, practical, integrated VCO.

The TRF3765 includes four VCOs with overlapping tuning frequency ranges to cover the entire fundamental range without gaps. A block diagram in Figure 2 illustrates the VCO arrangement. Each VCO is only required to cover a subset of the frequency range.

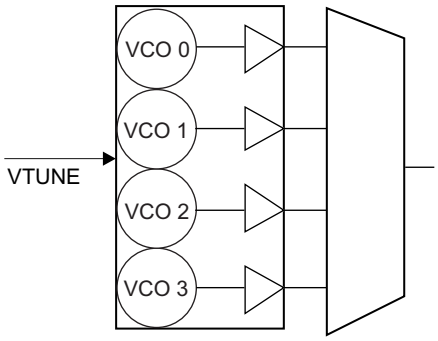

Figure 2. Four Integrated VCOs Cover a Broadband Tuning Range

Figure 3 shows the structure of each individual VCO. The cross-coupled differential pair with a pullup inductive load forms an oscillator. The input VTUNE is routed into a varactor, which provides a variable capacitance depending on the value of VTUNE. The combination of capacitance and inductance forms a tank circuit whose resonant frequency depends on the value of capacitance. Because VTUNE is driven from the charge pump through a loop filter, it can only vary from ground level to the power supply rail, with corresponding limits on varactor capacitance and resonant frequency. The range of possible capacitance can be expanded by including the digitally switched bank seen in Figure 3.

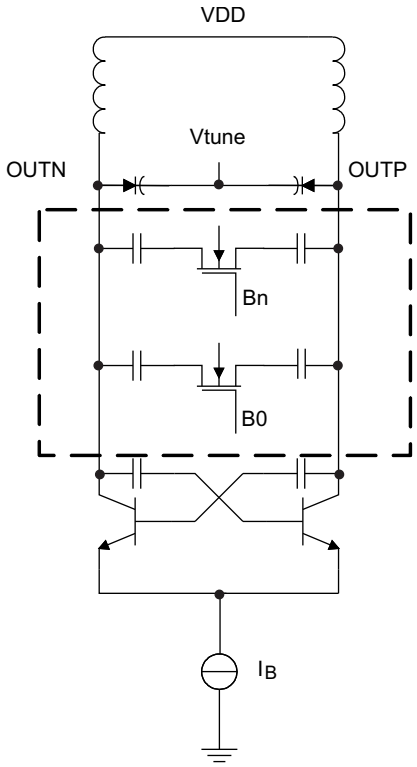

Figure 3. Structure of an Individual VCO

Figure 4 shows the resulting frequency ranges. For any condition of selected VCO and capacitive bank, a narrow range of VCO output frequencies can be generated. As long as adjacent selections of VCO and capacitor bank overlap, a continuous wideband frequency range can be achieved. However, if the selected VCO and digital capacitor does not support the desired frequency, VTUNE slides to either ground or the supply rail and the PLL cannot lock. No analog feedback mechanism is available to tune the PLL once the limit of supply rails has been exceeded.

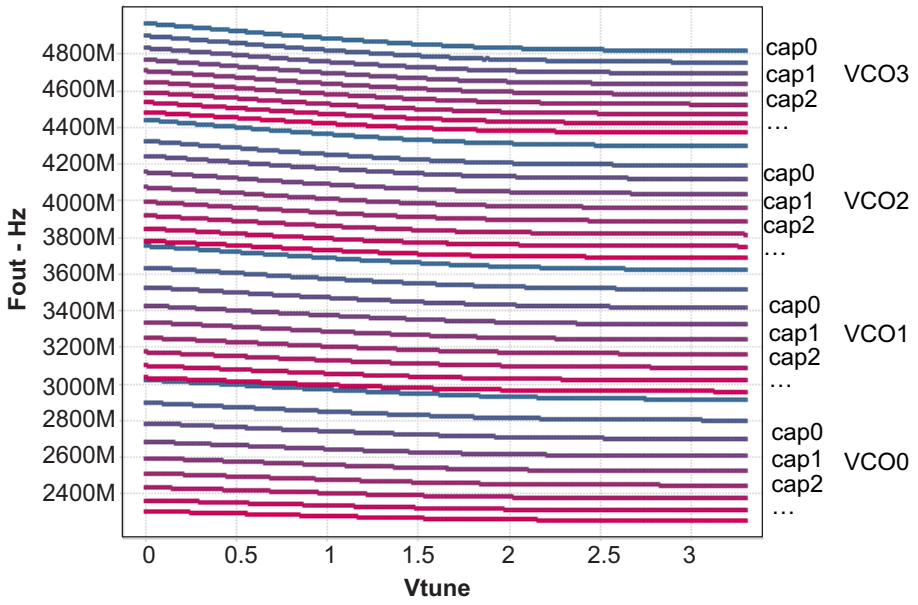

Figure 4. Overlapping VCO and Capacitor Settings Combine for Wideband Operation

2.2 Timing of the Digital Calibration

The device includes logic to drive an automated search algorithm, called a VCO calibration, to identify and select the appropriate VCO and capacitor setting for the desired frequency. The calibration logic is driven by a CAL_CLK derived from the phase frequency detector (PFD) frequency scaled according to the setting in CAL_CLK_SEL. The maximum number of CAL_CLK cycles required for the search can be calculated and is reported in Table 1.

Table 1. Maximum Digital Calibration Clock Cycles

CAL_BYPASS	VCOSEL_MODE	MAX CYCLES CAL_CLK	VCO	CAPACITOR ARRAY
0	0	46	Automatic	
0	1	34	VCO_SEL_n	Automatic
1	*don't care*	N/A	VCO_SEL_n	VCO_TRIM_n

Actual search cycles are generally lower than the maximum number shown in Table 1, because the device stops searching once the valid VCO and capacitor are found.

The CAL_CLK may be operated at frequencies up to 600 kHz. Because it is derived from the PFD frequency with a multiply or divide that scales by powers of 2, positive or negative, the CAL_CLK frequency can always be set at 300 kHz or faster. Therefore, calibration time can always be set at or below 15 µs.

The device also allows users to bypass the automated calibration function by setting VCO_SEL and VCO_TRIM in the registers, thereby eliminating calibration time. A system bypassing the automated calibration function refers to a lookup table constructed during factory calibration or includes an independent control mechanism.

3 Analog Lock

3.1 Lock-Time Measurements

Analog lock time is the time required for the PLL loop to settle to its steady-state frequency after

programming the VCO and capacitor array. Narrowband systems often characterize settling time referenced to small-step changes and large-step changes with large-step changes requiring longer times to charge capacitors and settle. Because the TRF3765 digitally switches capacitors and VCOs and generally executes a calibration with any frequency step, little correlation exists between step size and lock time except for the smallest frequency steps.

Analog lock time varies with loop bandwidth, with wider loop bandwidths leading to faster lock. Because the integer mode and fractional mode TRF3765 configurations have different bandwidths, results for both setups are included. To eliminate calibration time, VCO and capacitor were programmed before initiating the measured frequency change. The steady-state frequency is 2.4 GHz for all tests.

Three scenarios are tested for each configuration. Table 2 summarizes lock time as determined by settling within 10° or ±100 kHz of steady state. The first configuration makes a small frequency step within the same VCO and capacitor setting. Frequency and phase settling measurements are plotted in Figure 5 and Figure 6 for integer and fractional configurations.

Table 2. Summary of Measured Analog Lock Times

Step	100-kHz Frequency Settling Time (µs)		10° Phase Settling Time (µs)	
	Integer	Fractional	Integer	Fractional
Small, VTune shift	18	35	22	87
Medium, Capacitor Change	34	64	60	122
Large, VCO Change	32	36	48	60

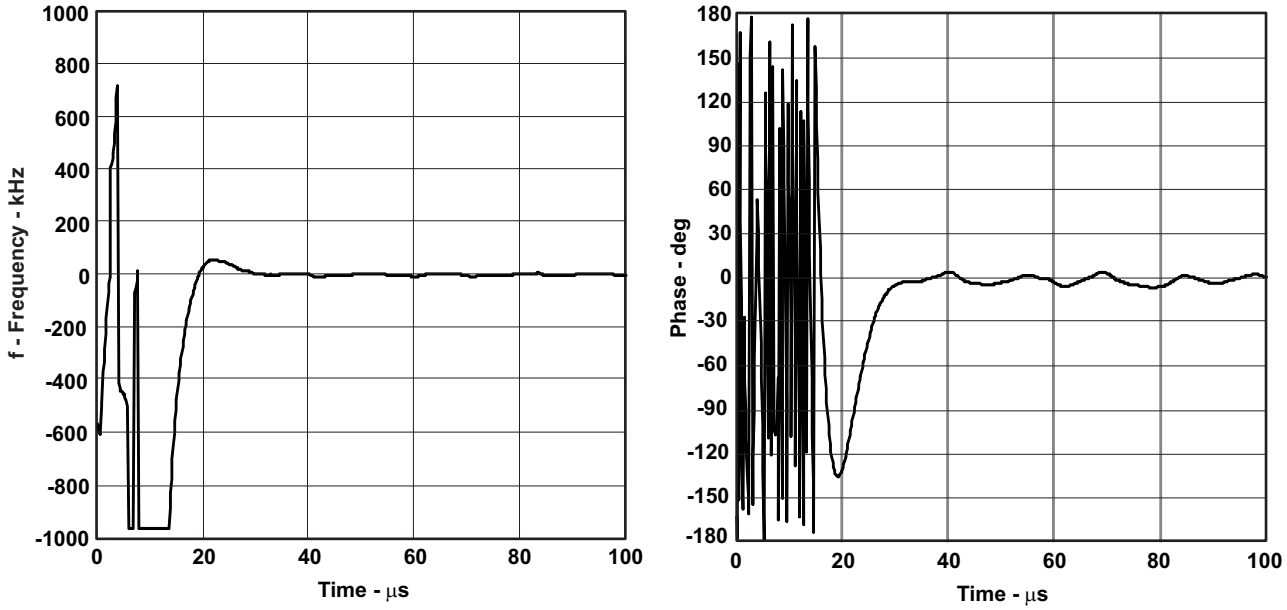

Figure 5. Frequency and Phase Settling for Integer Configuration Small Step

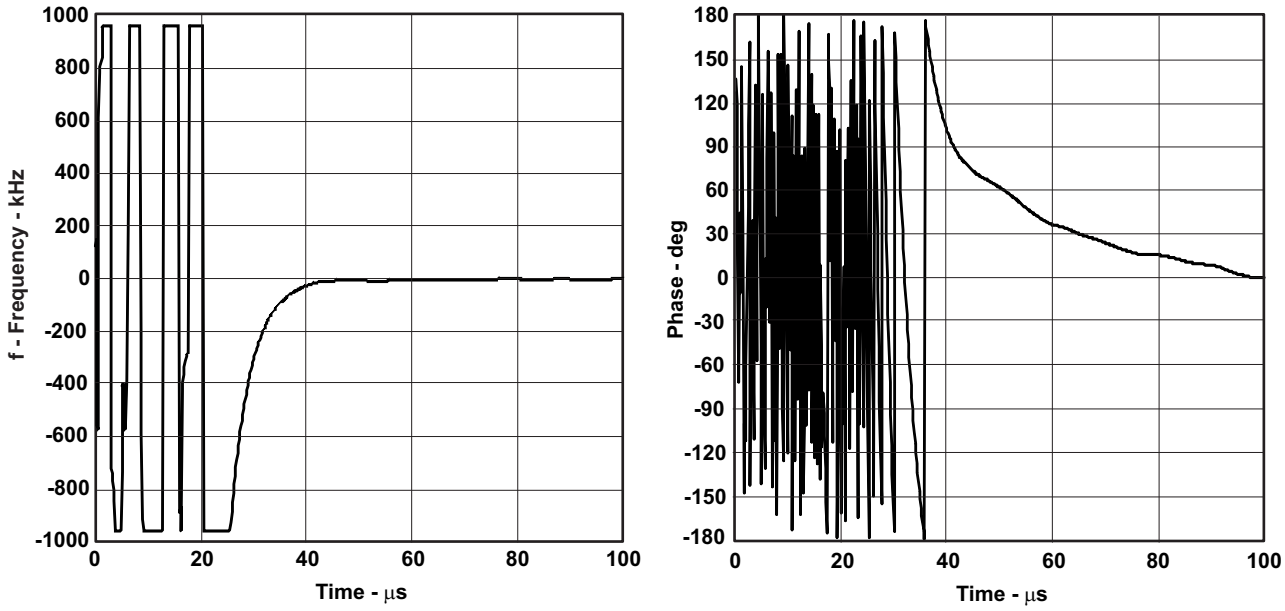

Figure 6. Frequency and Phase Settling for Fractional Configuration Small Step

The second configuration measures settling time for an intermediate frequency step by changing the capacitor array but remaining within the same VCO. Frequency and phase-settling measurements are plotted in Figure 7 and Figure 8 for integer and fractional configurations.

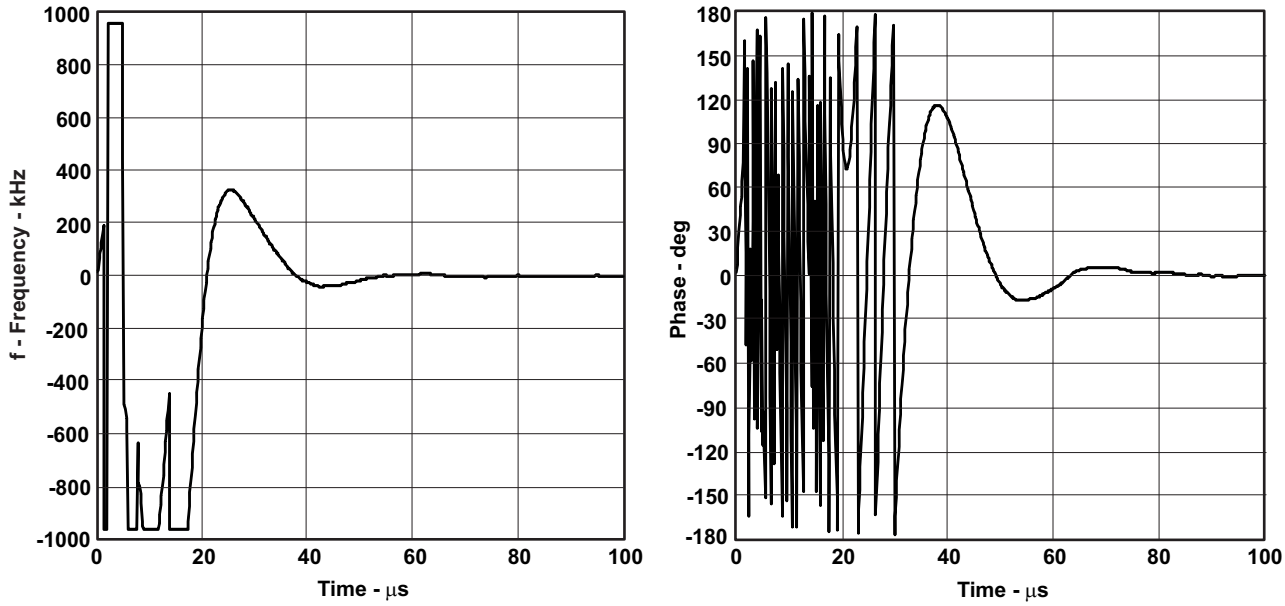

Figure 7. Frequency and Phase Settling for Integer Configuration Capacitor Change

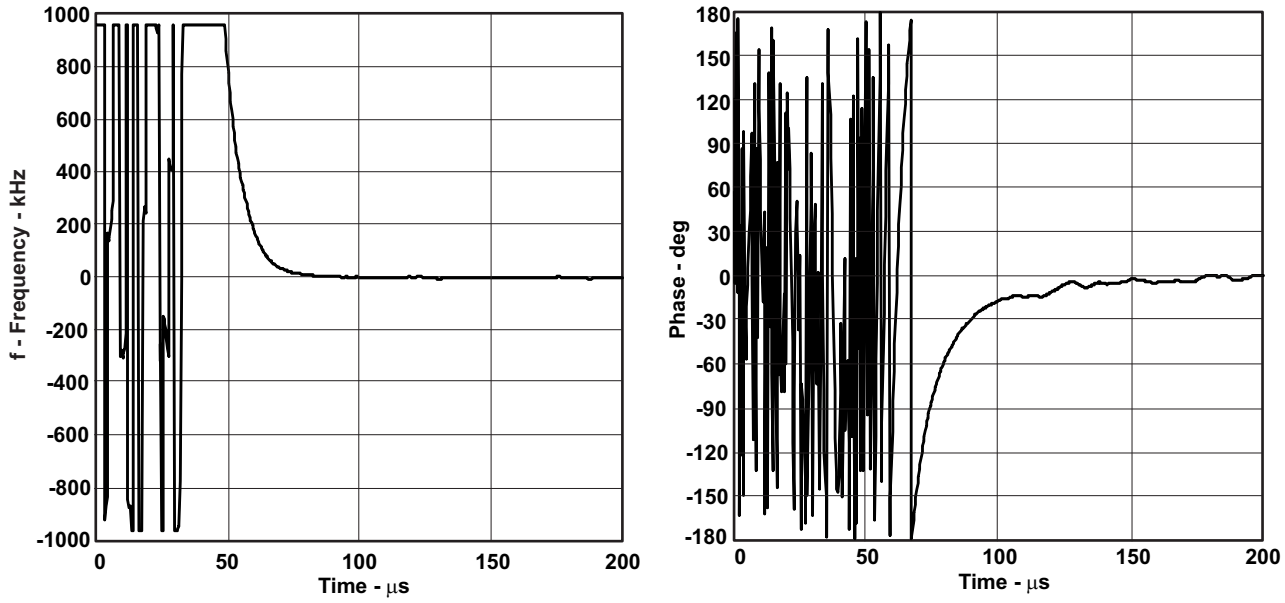

Figure 8. Frequency and Phase Settling for Fractional Configuration Capacitor Change

The third configuration measures settling time for a maximum frequency step, changing the selected VCO. Frequency and phase- settling measurements are plotted in Figure 9 and Figure 10 for integer and fractional configurations with SPEEDUP enabled.

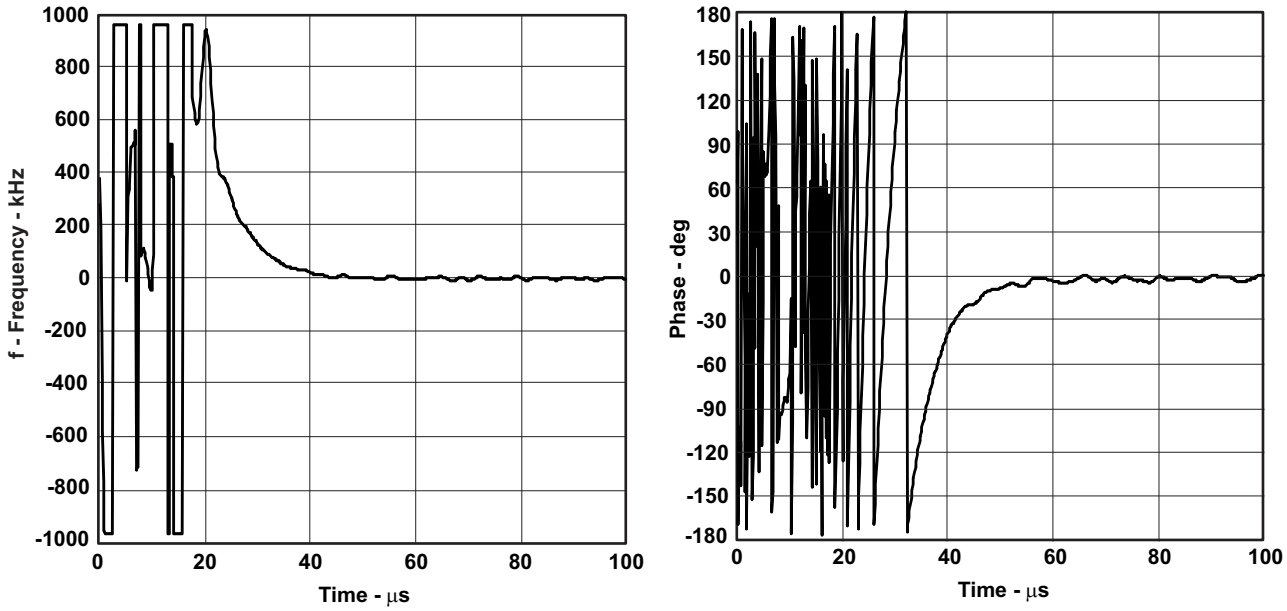

Figure 9. Frequency and Phase Settling for Integer Configuration VCO Change With SPEEDUP

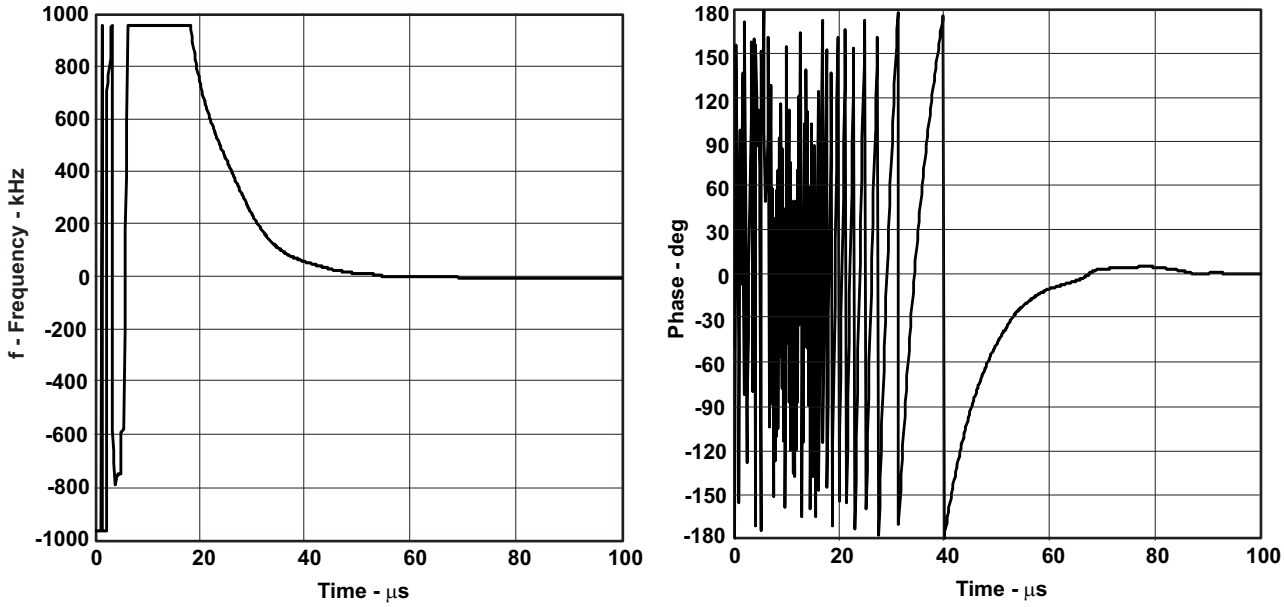

Figure 10. Frequency and Phase Settling for Fractional Configuration VCO Change With SPEEDUP

3.2 SPEEDUP Bit

To minimize power consumption, only one of the VCOs in the TRF3765 is biased, whereas the others are unbiased. Setting the SPEEDUP bit bypasses a portion of the bias stabilization filter, allowing the VCO to stabilize quickly. Lock time without SPEEDUP is much slower, as shown in Figure 11.

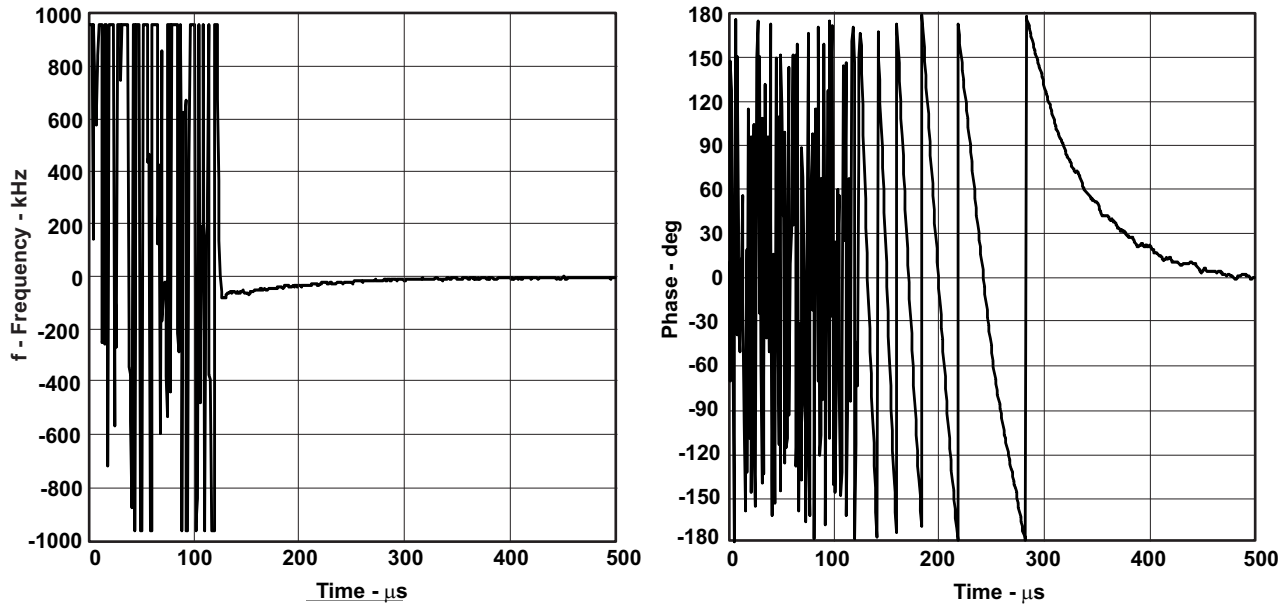

Figure 11. Frequency and Phase Settling for Integer Configuration VCO Change Without SPEEDUP

The VTUNE trajectory during lock with SPEEDUP is shown in Figure 12 alongside STROBE and the LD indicator. Tuning begins when STROBE pulses high. VTUNE climbs to its steady-state value within a few µs, with LD moving high after only 4 µs.

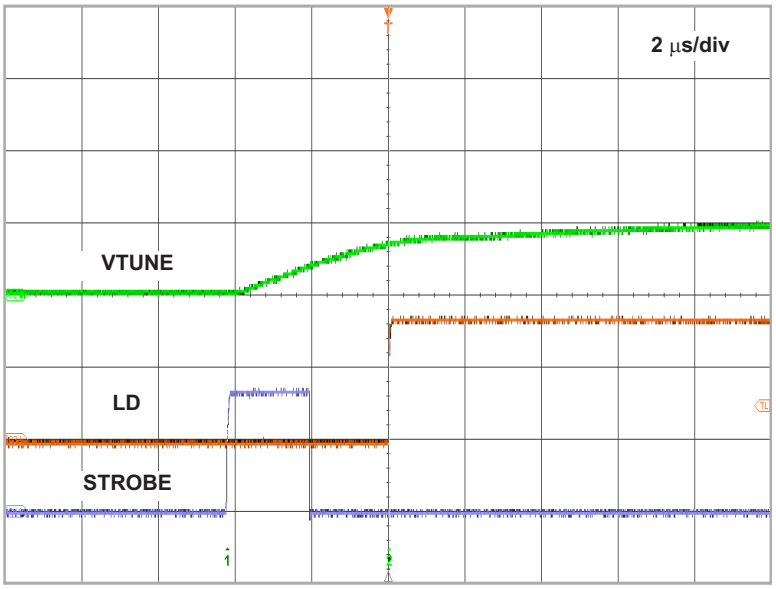

Figure 12. VTUNE Settling Trajectory With SPEEDUP

By contrast, the VTUNE trajectory during lock without SPEEDUP is shown in Figure 13. While the VCO bias current slowly settles internal to the TRF3765, VTUNE rails at the VCC limit. Then, VTUNE begins to settle only after the VCO has stabilized, with LD transitioning high 90 µs after the start.

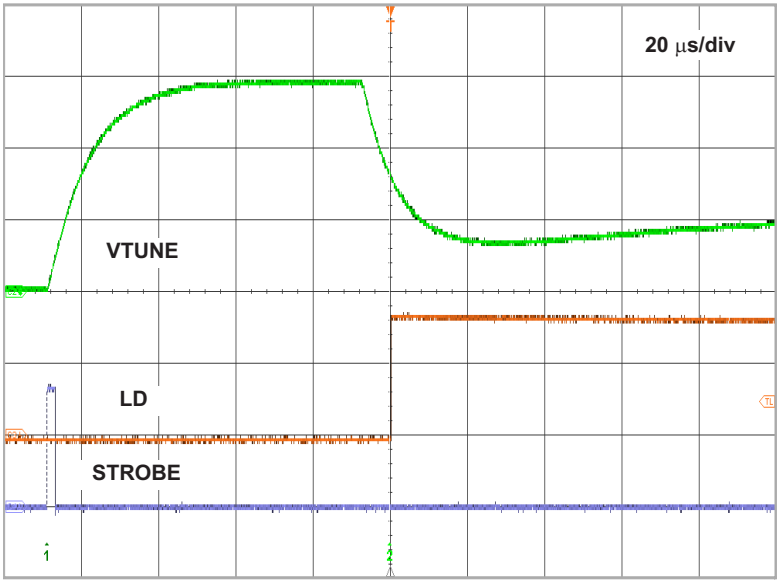

Figure 13. VTUNE Settling Trajectory Without SPEEDUP

For large frequency steps in applications where lock time is critical, set SPEEDUP high during frequency changes to minimize lock time. Then, disable SPEEDUP during normal operation to achieve the best-possible, phase-noise performance.

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