DAC5686/DAC5687 CLOCK GENERATION USING PLL AND EXTERNAL CLOCK MODES

Ken Chan *Wireless Infrastructure DAC*

1 INTRODUCTION

The DAC5686 and DAC5687 both have an onboard PLL and VCO, which allows for some diversity in the input clock (F_{clk}), data rates (F_{data}) and the update rate of the DAC (F_{dac}). There are three stages of interpolation (2x, 4x, and 8x) in the DAC5687 and an extra stage of interpolation (16x) in the DAC5686. The combination of this with options for interleaved data and a frequency divider in the PLL loop requires some clarification so that the clock modes can be better understood and used properly. The following documentation outlines various modes and settings to help the user understand how the clock modes are being set and the relationships between the input clock, data rate, and the DAC update rate.

There are slight differences between the PLL circuits of the DAC5686 and the DAC5687. The main difference is that the DAC5687 does not have the 16x interpolation and instead has two 4x interpolation modes (X4 and X4L) that use different interpolation filters.

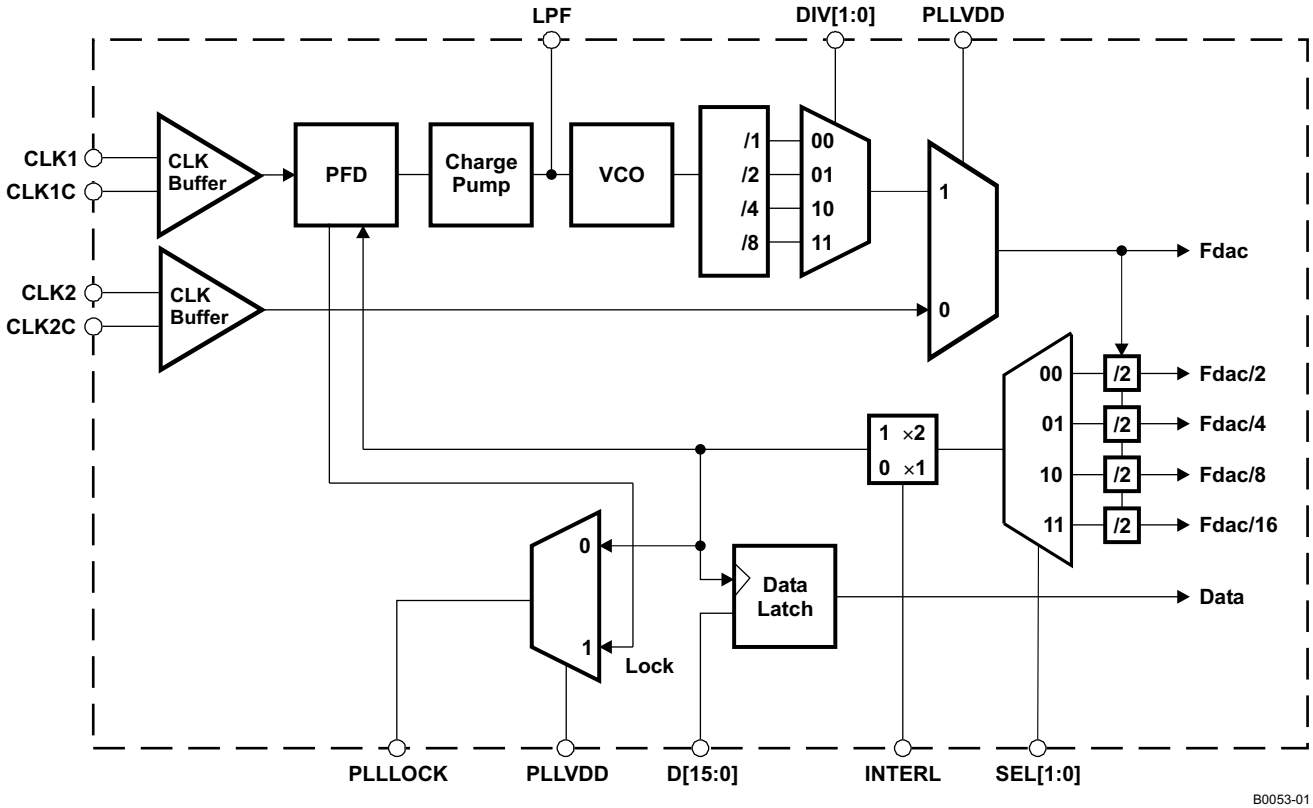

Figure 1. DAC5686 Block Diagram

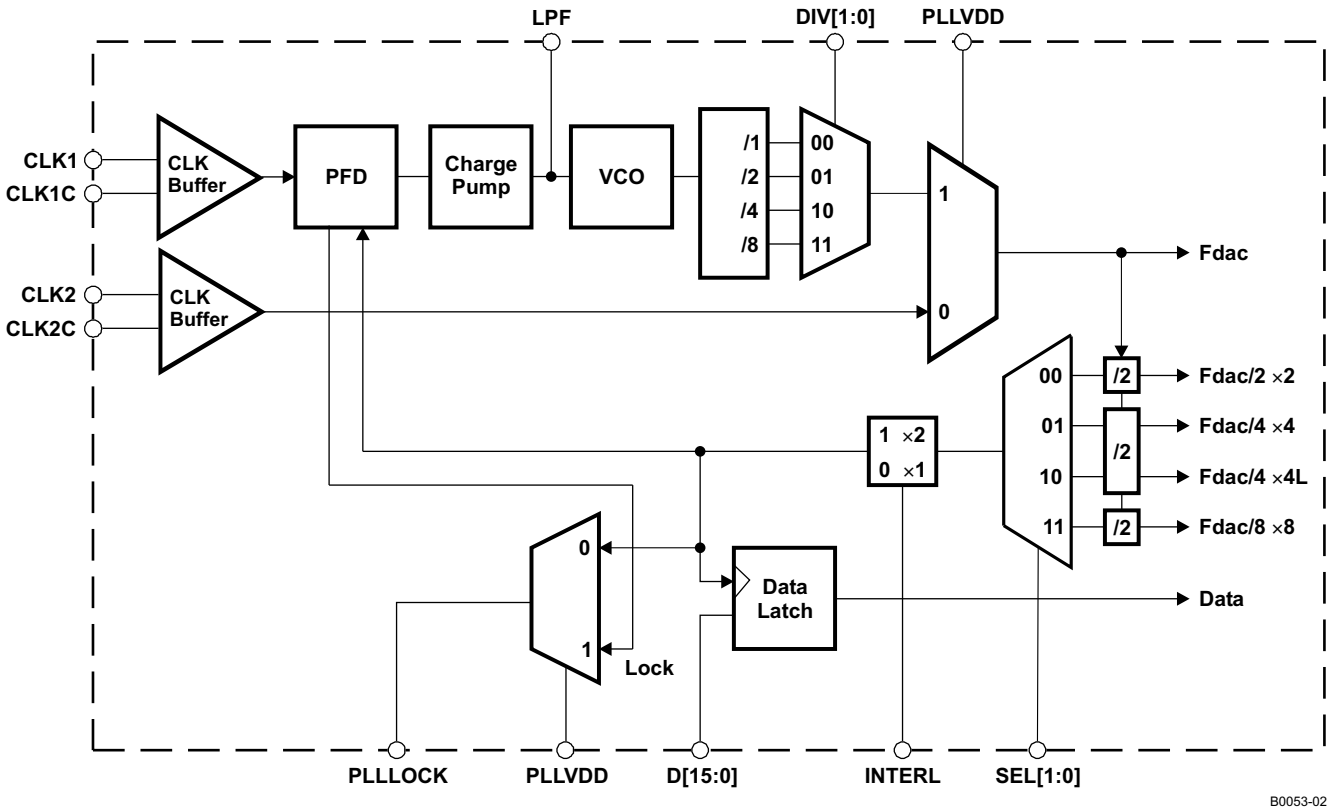

Figure 2. DAC5687 Block Diagram

The SEL[0:1] and INTERP[0:1] bits select the interpolation mode and determines which divided clocks are passed to the interpolation stages. The DIV[0:1] bits control the divide down ratio of the frequency divider (÷1 to ÷8). The INTERL bit determines if the data is coming in interleaved and activates a 2x stage if the data is interleaved. This clocks the latches at the incoming CLK1 rate. The data for channel A and B will be sampled at the ½ CLK1 rate, since they are interleaved on each period of CLK1. The interpolation filters will also run at the ½ CLK1 rate since that is the actual data rate of channel A and B.

Several examples are described below to illustrate the relationships between all these control bits for the PLL and the different clock modes using the DAC5687 block diagram. The settings for the DAC5686 and DAC5687 are similar. The only thing to be aware of is that the DAC5687 does not have the 16x mode. With this in mind, these examples will apply to both DACs.

Table 1. Possible PLL and Clock Register Settings

	DAC5686								DAC5687							
SEL[0:1]	00	2X	01	4X	10	8X	11	16X	00	2X	01	4X	10	4XL	11	8X
DIV[0:1]	00	/1	01	/2	10	/4	11	/8	00	/1	01	/2	10	/4	11	/8
INTERL	0		1						0		1					

2 EXTERNAL CLOCK MODE

The external clock mode is set by setting PLLVDD to GND. Since the PLL is not used the CLK1/CLK1C and the LPF (for the VCO) pins can be left unconnected. In this mode the PLLLOCK pin outputs a clock that can be used to drive the data input into the DAC. This output clock depends on the interpolation rate and the interleave mode.

In external clock mode, the PLL is completely turned off and the DIV[0:1] bits have no effect on the circuit. The INTERP or SEL bits are the only bits controlling the interpolation filter sampling rates and the data clock coming out of PLLLOCK. PLLLOCK can be used to drive the data source.

2.1 EXAMPLE 1:

Data is sampled at 80 MSPS, non interleaved. If the DAC rate needs to be at 320 MHz, using the external clock mode, CLK2 needs to be connected with 320-MSPS clock (DAC update rate). INTERL = 0 since the data is not interleaved. SEL needs to be set to 4x so that the clock sent out of PLLLOCK to clock the data is at 80 MHz and the clocks sent to the interpolation filters is 80 MHz for the first stage and 160 MHz for the second stage. The clock signal path is shown below in yellow.

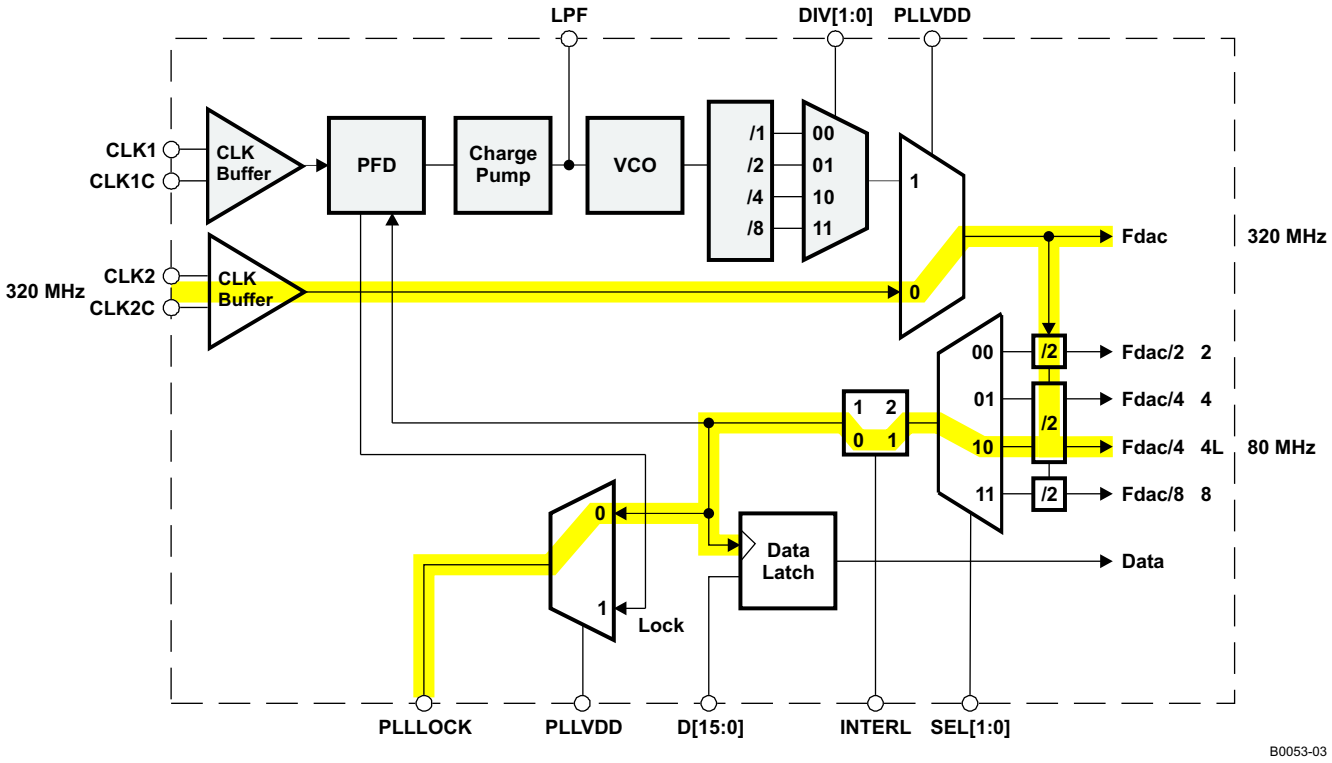

Figure 3. Example 1: External Clock, Non-Interleaved Data

2.2 EXAMPLE 2:

If the data in example 1 is interleaved, INTERL=1, then the interpolation rate must be changed to 8x to maintain the DAC rate at 320 MHz. With the 2x block activated the PLLLOCK outputs an 80-MHz clock, but the first interpolation filters will be running at the interleaved data rate of 40 MSPS, and the second interpolation filter at 80 MSPS.

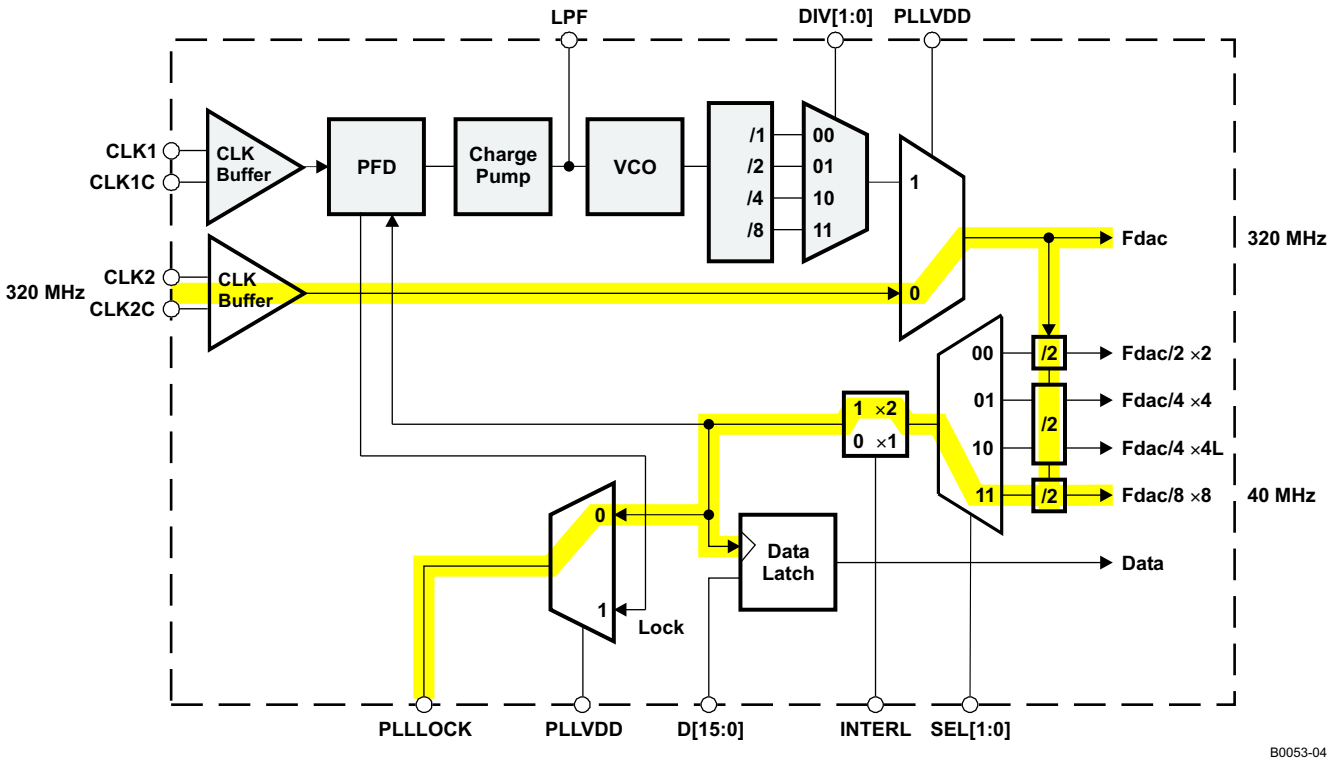

Figure 4. Example 2: External Clock, Interleaved Data

3 PLL MODE

The PLL mode is activated by supplying 3.3 Vdc to the PLLVDD. The data clock is supplied through CLK1. CLK2 is not used. The input frequency and control frequency of the phase frequency detector (PFD) must be the same if the PLL is in a locked state. For this condition to be true, the relationship between the frequency divider DIV, INTERL, and SEL can not be arbitrary and must be set such that the VCO frequency is divided down correctly to meet the lock conditions of the PFD. The DIV bits are set based on the operating range of the VCO and its associated LPF. See the DAC5687 and DAC5686 data sheet for the different operating modes and operating frequency bands of the VCO.

3.1 EXAMPLE 3:

Lets assume that we have an input clock rate of 80 MHz and the data is not interleaved. A 320-MSPS DAC update rate is still desired. For this mode, we can use DIV=1x assuming the VCO and LPF are optimized around 320 MHz and SEL is set to 4x. In this case, the VCO operates at 320 MHz and is not divided by the DIV control bits. The DAC rate is 320 MHz and the interpolation rate must be 4x to bring the 80-MSPS input data up to a 320-MSPS sampling rate.

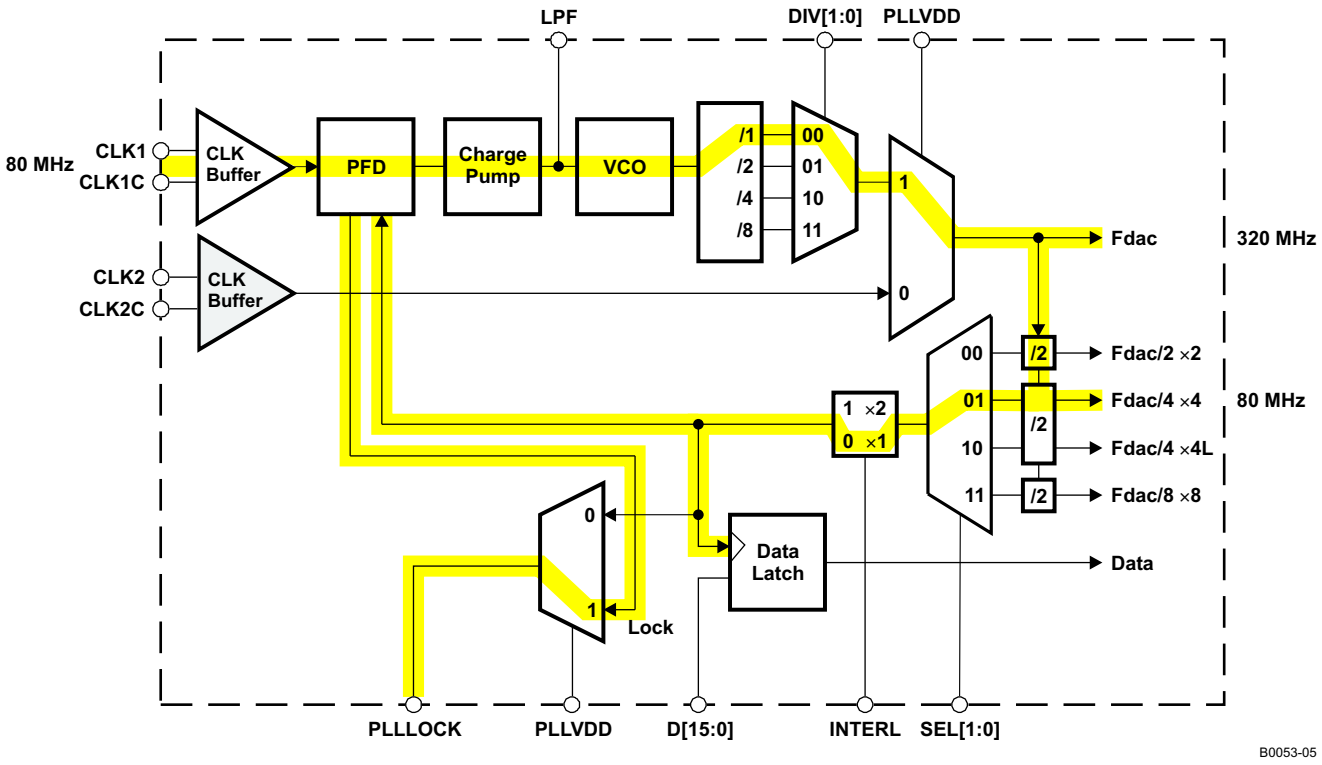

Figure 5. Example 3: PLL Mode Non-Interleaved Data

3.2 EXAMPLE 4:

Assume the data in example 3 is interleaved INTERL = 1. The first interpolation clocks will be at 40 MSPS instead of 80 MHz, requiring 8x interpolation to reach the DAC update rate of 320 MSPS.

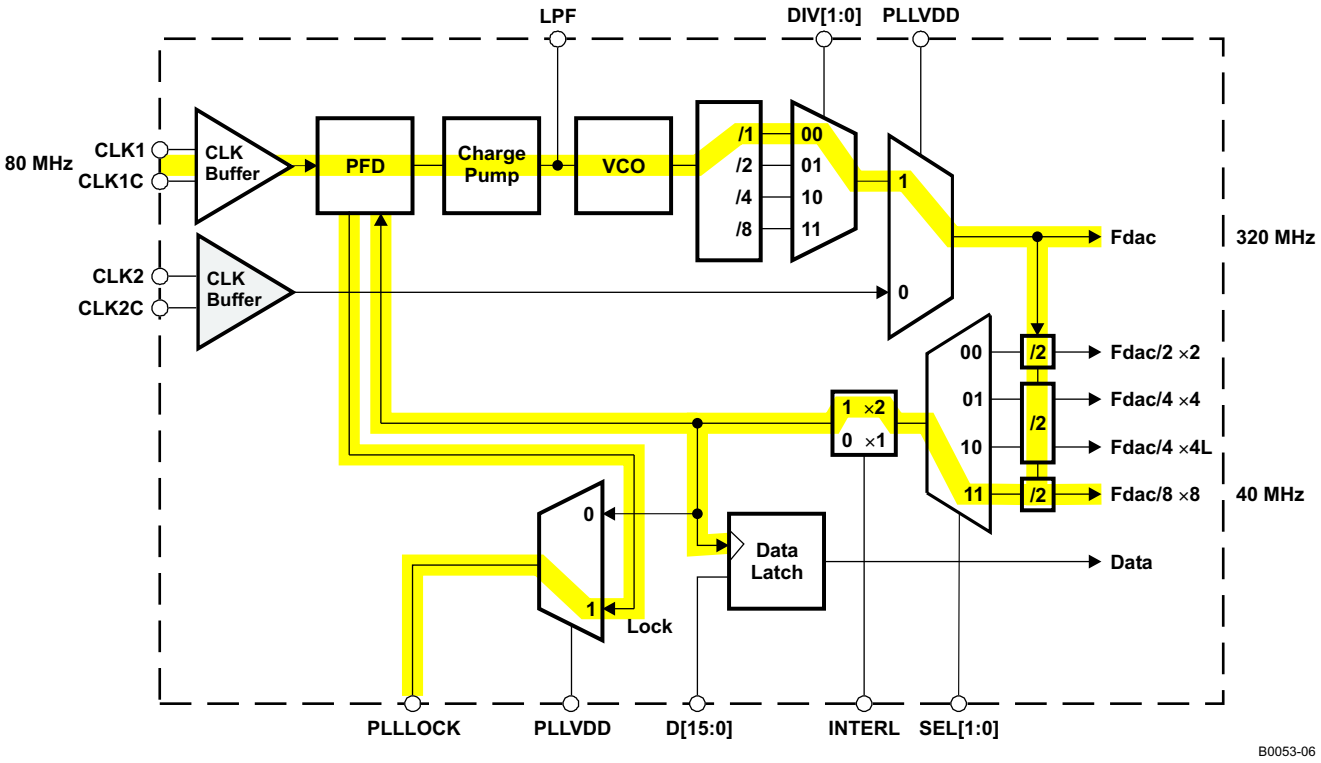

Figure 6. Example 4: PLL Mode With Interleaved Data

3.3 EXAMPLE 5:

Lets assume that we have an input clock frequency of 80 MHz and the data is not interleaved. A 160 MSPS DAC update rate is desired. For this mode, we can use DIV = 2x assuming the VCO and LPF are optimized around 320 MHz and SEL is set to 2x. In this case, the VCO operates at 320 MHz and IS divided by the DIV control bits. The DAC rate is 320/2 = 160 MSPS, and the interpolation rate must be 2x to bring the 80-MSPS input data up to a 160-MSPS sampling rate.

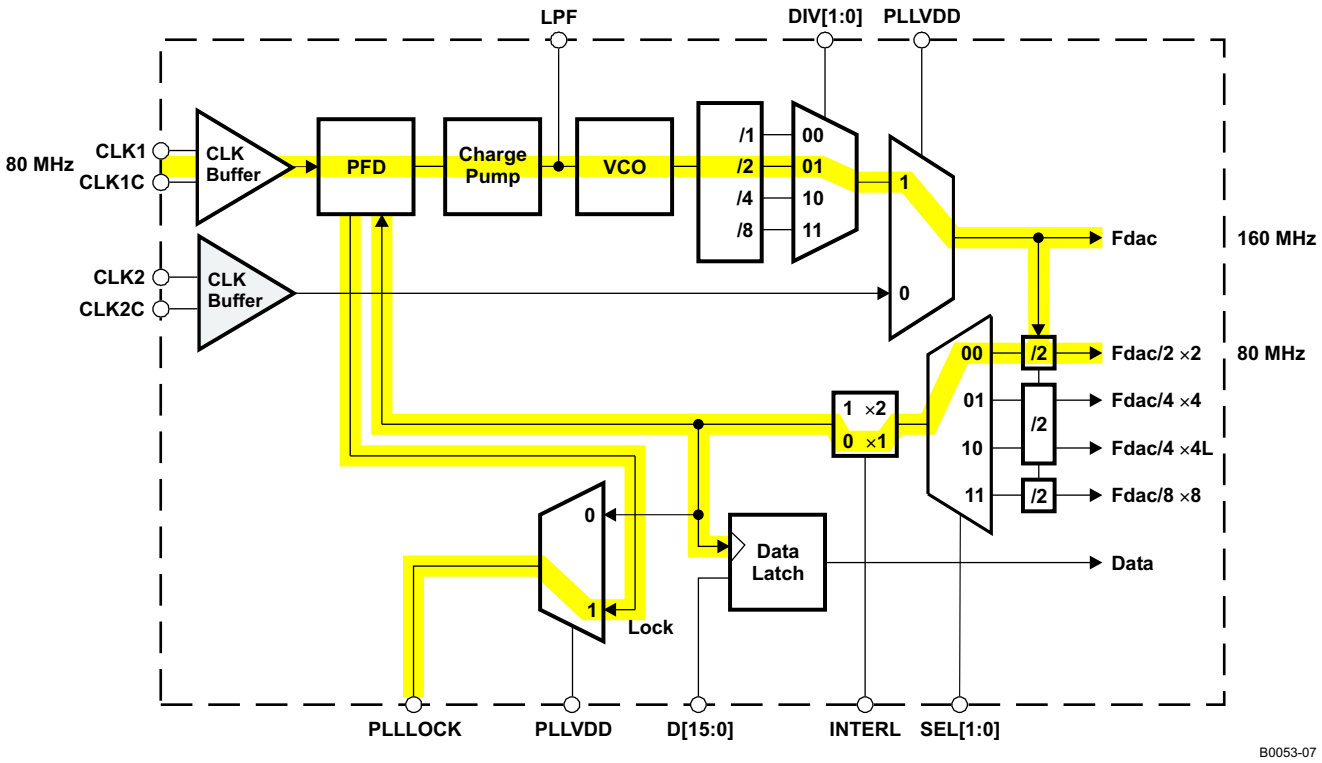

Figure 7. Example 5: Using DIV to Get Different DAC Update Rate

3.4 EXAMPLE 6:

If example 5 had interleaved data, INTERL=1, then 4x interpolation would have to be used. The first interpolation filter would run at 40 MSPS.

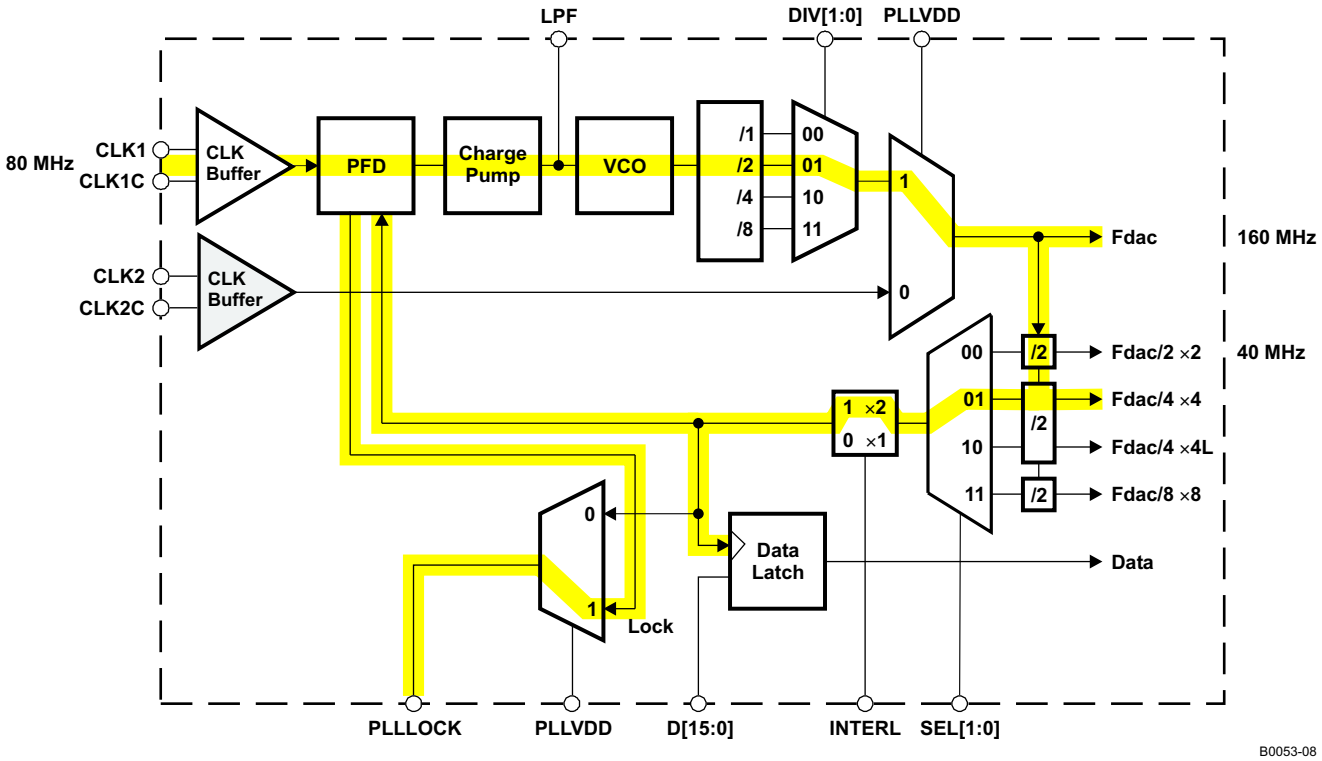

Figure 8. Example 6: Using DIV to Get Different DAC Update Rate With Interleaved Data

4 DUAL-CLOCK MODE

The final mode is the dual-clock mode. This mode allows CLK1 to drive the input data rate and CLK2 to drive the DAC. This mode uses different circuitry than is used in either the PLL mode or the external clock mode. There is a FIFO that can be used in this mode to eliminate the need to phase align the clocks to a tight specification. For details using this mode, see the respective data sheet.

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