User's Guide

TPS63900 Evaluation Module User's Guide

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ABSTRACT

This user's guide describes the operation and use of the TPS63900EVM evaluation module (EVM). The TPS63900EVM is designed to help easily evaluate and test the operation and functionality of the TPS63900 buck-boost converter. The EVM can be used over the full recommended operating range of the TPS63900.

This document includes setup instructions for the hardware, a schematic diagram, a bill of materials (BOM), and printed-circuit board (PCB) layout drawings for the EVM. Throughout this document, the abbreviations EVM, TPS63900EVM, and the term evaluation module are synonymous, unless otherwise noted.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The Texas Instruments TPS63900 is a high-efficiency synchronous buck-boost converter with an extremely low quiescent current (75 nA typical) in a 10-pin, 2.5-mm × 2.5-mm, 0.5-mm pitch WSON package.

1.1 Background

The TPS63900EVM uses the TPS63900 integrated circuit (IC) and operates with an input voltage up to 5.5 V.

1.2 Performance Specification

Refer to the TPS63900 data sheet for the full range of recommended operating specifications and design guidelines for driving loads. Table 1-1 provides a summary of the tested TPS63900EVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1-1. EVM Performance Specification Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		1.8		5.5	V
Output voltage		1.8		5	V
Output current	V_{IN} = 3.7 V , V_{OUT} = 3.3 V	330			mA

1.3 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate the TPS63900. Extra positions are available for additional input and output capacitors.

2 Setup

This section describes how to properly use the TPS63900EVM.

2.1 Input/Output Connector and Header Descriptions

2.1.1 J1, Pin 1 and 2 – VIN

Positive input connection from the input supply to the EVM

2.1.2 J1, Pin 3 and 4 – S+/S-

Input voltage sense connections. Measure the input voltage at this point.

2.1.3 J1, Pin 5 and 6 – GND

V_{in} GND return connection from the input supply to the EVM, common with J2, pin 5 and 6

2.1.4 J2, Pin 1 and 2 – VOUT

Output voltage connection. Connect the positive side of the load to these pins.

2.1.5 J2, Pin 3 and 4 – S+/S-

V_{out} Sense and GND Sense low-current sense lines for sampling the output voltage at the output capacitor.

2.1.6 J2, Pin 5 and 6 – GND

V_{out} GND return connection for the output voltage, common with J1, pin 5 and 6. Connect the negative side of the load to these pins.

2.1.7 J4 – GND

GND connection

2.1.8 JP1 – SEL

Shorting jumper between the center pin SEL and VO2 enables the output voltage according to Table 2-1. Shorting SEL and VO1 the output voltage will be set according to Table 2-2. Details on the output voltage selection is available in the TPS63900 data sheet.

2.1.9 JP2 – ENABLE

Short the jumper between the center pin EN and ON to turn the IC on. Short the jumper between the center pin EN and OFF to turn the IC off. Use the center pin to apply an external enable signal.

2.1.10 JP3 – CFG1

Pin 1 is routed to CFG1 for measuring its voltage at the IC. Measure the voltage against GND (Pin 2).

2.1.11 JP4 – CFG2

Pin 1 is routed to CFG2 for measuring its voltage at the IC. Measure the voltage against GND (Pin 2).

2.1.12 JP5 – CFG3

Pin 1 is routed to CFG3 to measure its voltage at the IC. Measure the voltage against GND (Pin 2).

2.1.13 S1, S2, S3, S4, S5, S6 – IC Configuration (R2D Interface)

The output voltage is set according to Table 2-1 and Table 2-2. The configuration pins CFG1, CFG2, and CFG3 must not be left floating. Every CFG pin has 16 switches for the different resistor values, but only one switch at a time can be set to ON for each CFG pin. Turn ON the corresponding switches written in Table 2-1 and Table 2-2 $V_{O(2)}$ is set by switch-blocks S1,S2, S4, and S5. $V_{O(1)}$ is set by switch-blocks S3 and S6.

Example: $V_{O(2)}$ (SEL = VO2) is set to 3.4 V and the current limit to unlimited. Set S1.1 to ON for CFG1, S5.1 to ON for CFG2, and S3.1 to ON to keep CFG3 from floating.

Table 2-1. Input Current Limit and Output Voltage $V_{O(2)}$ (SEL = VO2) Settings

OUTPUT VOLTAGE $V_{O(2)}$ (SEL = VO2)	INPUT CURRENT LIMIT							
	UNLIMITED	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
1.8 V	S1.1							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
1.9 V	S1.2							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.0 V	S1.3							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.1 V	S1.4							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.2 V	S1.5							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.3 V	S1.6							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.4 V	S1.7							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.5 V	S1.8							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.6 V	S4.1							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.7 V	S4.2							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.8 V	S4.3							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
2.9 V	S4.4							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
3.0 V	S4.5							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
3.1 V	S4.6							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
3.2 V	S4.7							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
3.3 V	S4.8							
	S2.1	S2.2	S2.3	S2.4	S2.5	S2.6	S2.7	S2.8
3.4 V	S1.1							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
3.5 V	S1.2							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
3.6 V	S1.3							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
3.7 V	S1.4							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
3.8 V	S1.5							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
3.9 V	S1.6							

Table 2-1. Input Current Limit and Output Voltage $V_{O(2)}$ (SEL = VO2) Settings (continued)

OUTPUT VOLTAGE $V_{O(2)}$ (SEL = VO2)	INPUT CURRENT LIMIT							
	UNLIMITED	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.0 V	S1.7							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.1 V	S1.8							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.2 V	S4.1							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.3 V	S4.2							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.4 V	S4.3							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.5 V	S4.4							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.6 V	S4.5							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.7 V	S4.6							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
4.8 V	S4.7							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8
5.0 V	S4.8							
	S5.1	S5.2	S5.3	S5.4	S5.5	S5.6	S5.7	S5.8

Table 2-2. Output Voltage $V_{O(1)}$ (SEL = VO1) Settings

OUTPUT VOLTAGE $V_{O(1)}$ (SEL = VO1)	CFG3
1.8 V	S3.1
2.0 V	S3.2
2.1 V	S3.3
2.2 V	S3.4
2.3 V	S3.5
2.4 V	S3.6
2.5 V	S3.7
2.6 V	S3.8
2.7 V	S6.1
2.8 V	S6.2
3.0 V	S6.3
3.3 V	S6.4
3.6 V	S6.5
4.0 V	S6.6
4.5 V	S6.7
5.0 V	S6.8

2.2 Setup

To operate the EVM, only one switch per CFG pin must be turned ON. The switch-blocks pair S1 and S4 is connected to CFG1, the pair S2 and S5 is connected to CFG2, and the pair S3 and S6 is connected to CFG3. Table 2-1 and Table 2-2 define the switches to be turned ON corresponding to the desired output voltage and current limit. Make sure exactly one switch per switch-block pair is set to ON. Connect an input supply with the positive lead to J1, pins 1 and 2, and negative lead to J1, pins 5 and 6. Connect a load with the positive lead to J2, pins 1 and 2, and the negative lead to J2, pins 5 and 6. Short EN and ON (pins 2 and 3) of JP2 with a shorting jumper.

3 Board Layout

This section provides the TPS63900EVM board layout and illustrations.

3.1 Layout

Figure 3-1 through Figure 3-4 show the board layout for the TPS63900EVM PCB.

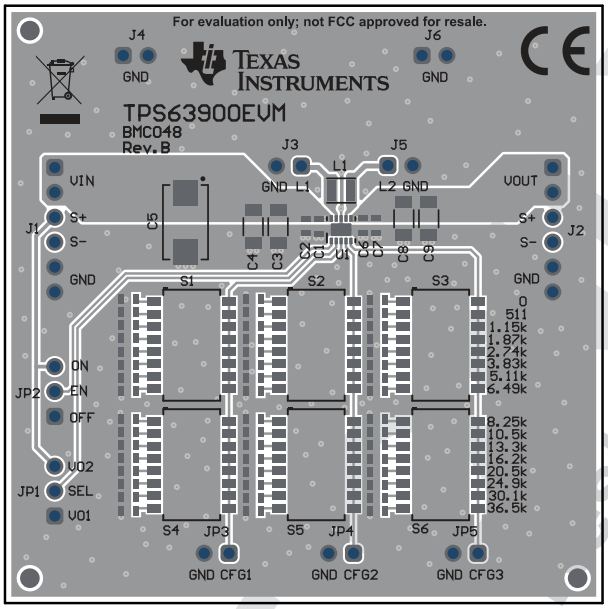

Figure 3-1. Assembly Layer

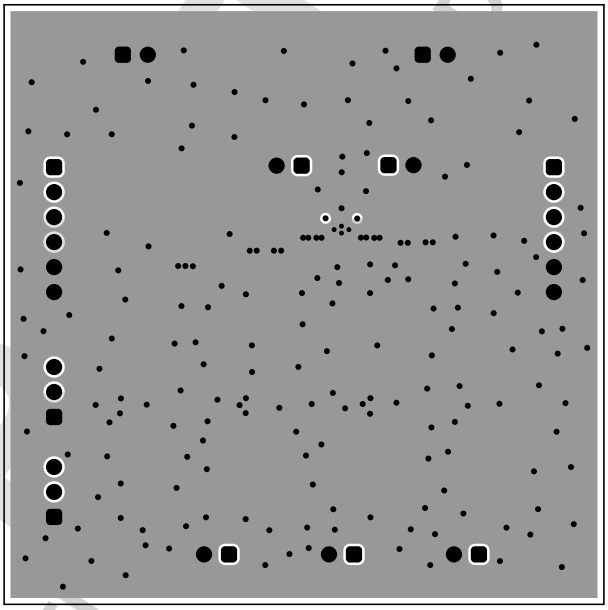

Figure 3-2. Internal Layer 1

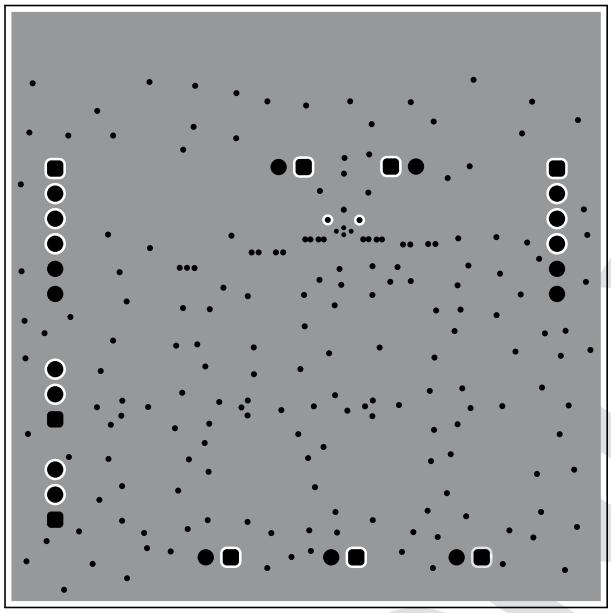

Figure 3-3. Internal Layer 2

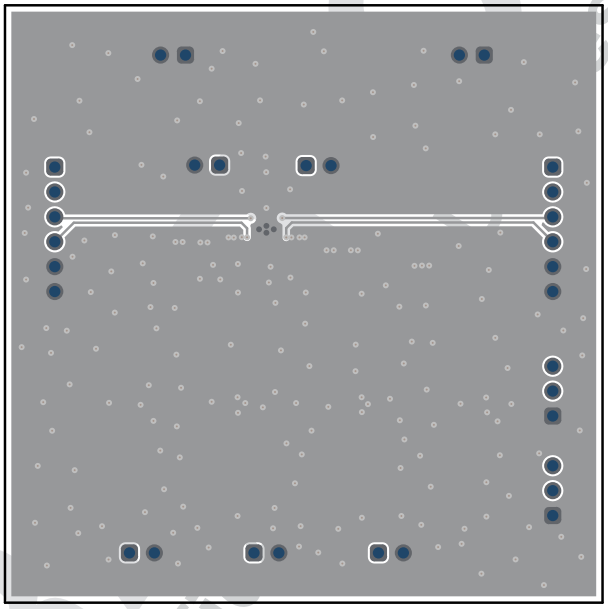

Figure 3-4. Bottom Layer (Mirrored)

4 Schematic

The red crosses indicate that these components are not populated.

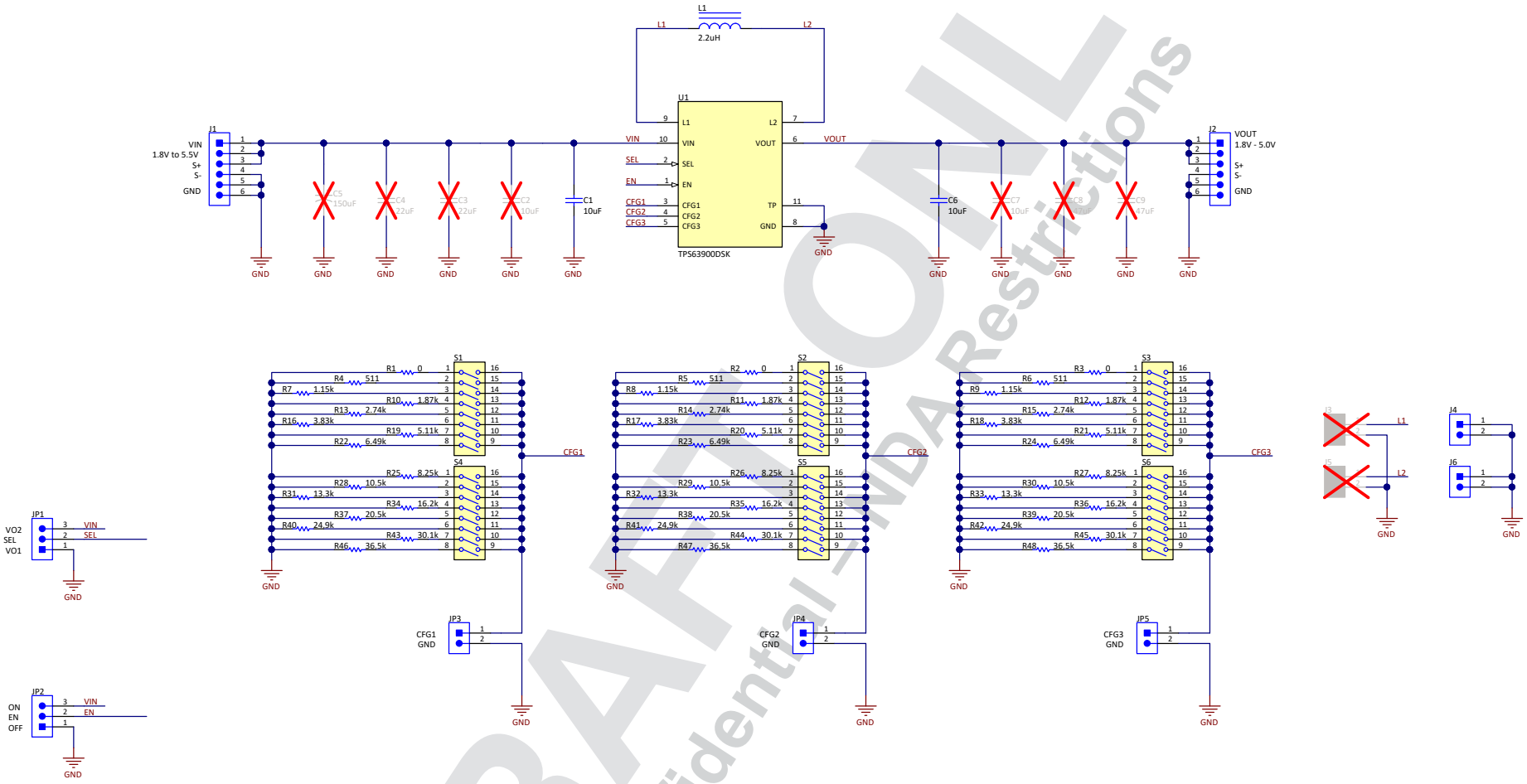

Figure 4-1. Schematic

5 Bill of Materials

Table 5-1. TPS63900EVM Bill of Materials

COUNT	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
1	C1	10 µF	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J106ME84	muRata
1	C6	22 µF	CAP, CERM, 22 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J226MEA0	muRata
1	L1	2.2 µH	Inductor, Shielded, Powdered Iron, 2.2 µH, 2.3 A, 0.082 Ω, SMD	2.5 × 2 × 1.2 mm	DFE252012F-2R2M=P2	muRata
1	R1, R2, R3	0	RES, 0, 1%, 0.1 W, 0603	0603	Std	Std
1	R4, R5, R6	511	RES, 511, 1%, 0.1 W, 0603	0603	Std	Std
1	R7, R8, R9	1.15 k	RES, 1.15 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R10, R11, R12	1.87 k	RES, 1.87 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R13, R14, R15	2.74 k	RES, 2.74 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R16, R17, R18	3.83 k	RES, 3.83 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R19, R20, R21	5.11 k	RES, 5.11 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R22, R23, R24	6.49 k	RES, 6.49 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R25, R26, R27	8.25 k	RES, 8.25 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R28, R29, R30	10.5 k	RES, 10.5 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R31, R32, R33	13.3 k	RES, 13.3 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R34, R35, R36	16.2 k	RES, 16.2 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R37, R38, R39	20.5 k	RES, 20.5 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R40, R41, R42	24.9 k	RES, 24.9 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R43, R44, R45	30.1 k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	Std	Std
1	R46, R47, R48	36.5 k	RES, 36.5 k, 1%, 0.1 W, 0603	0603	Std	Std
1	S1, S2, S3, S4, S5, S6	-	Switch, SPST, 8 Pos, 25 mA, 24VDC, SMD	11.33 × 5.8mm	218-8LPST	CTS Electrocomponents
1	U1	-	IC, Single Inductor Buck-Boost Converter	2.5 × 2.5 × 0.5 mm	TPS63900DSK	TI

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (September 2020)	Page
• Changed 200 nA to 75 nA.	2
• Added ...tested in Chapter 1.2.	2
• Deleted Note about Preliminary Material Issue.	2
• Added "Use the center pin to apply an external enable signal."	3
• Changed "Short the jumper between the pins to set the CFG1 pin to GND." to "Measure the voltage against GND (Pin 2)."	3
• Changed "Short the jumper between the pins to set the CFG2 pin to GND." to "Measure the voltage against GND (Pin 2)."	3
• Changed "Short the jumper between the pins to set the CFG3 pin to GND." to "Measure the voltage against GND (Pin 2)."	3
• Added … Every CFG pin has 16 switches for the different resistor values, but only in Chapter 2.1.13	3

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