TPS61391EVM-058 Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPS61391EVM-058 evaluation module (EVM). The EVM contains the TPS61391 device, which is a step-up converter with the current mirror and sample and hold circuitry being integrated, which is designed for biasing and monitoring the avalanche photodiodes (APD) in the optical receivers. The user's guide includes EVM specifications, recommended test setup, test result, schematic diagram, bill of materials, and the board layout.

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1 Introduction

1.1 Performance Specification

Table 1 provides a summary of the TPS61391 EVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
V_{IN}		3.6			V
V_{OUT}	V_{IN} = 3.6 V, Io ≤ 3.5 mA	35			V
V_{PP+}	V_{IN} = 3.6 V, I_VPP ≤ 2 mA	70			V
$V_{PN–}$	V_{IN} = 3.6 V, I_VPN ≤ 3.5 mA	–35			V

1.2 Modification

The printed-circuit board (PCB) for this EVM is designed to accommodate some modifications by the user. The external component can be changed according to the user's application.

1.3 Input capacitor

A 100-µF tantalum capacitor (C1) is added as the input capacitor in the EVM. The ESR of the tantalum capacitor is 0.1 Ω which helps to damp the ringing of the input voltage when the EVM is powered by a power supply with a long cable. The capacitor is not required for proper operation and can be removed in a user's application.

1.4 Output Capacitor Selection

Two 0.1-µF ceramic capacitors (C3 and C4) are added as the output capacitors. These capacitors help ensure the low output ripple at heavy load.

1.5 APD Decoupling Capacitor Selection

The default APD decoupling capacitor is 220 pF (C10) on the EVM board. In the user's application, if there is already a decoupling capacitor on the optical module, then the decoupling capacitor C10 must be deleted from the EVM board. Too much decoupling capacitance results in poor optical detection sensitivity.

2 Setup

This section describes how to properly connect, set up, and use the TPS61391EVM.

2.1 Input/Output Connector Descriptions

Use the following connector descriptions to set up the EVM:

- J1-VIN: Positive input connection from the input supply for the EVM
- J2-GND: Return connection from the input supply for the EVM
- J3-VOUT: Positive connection for the output voltage
- J4-GND: Return connection for the output voltage
- J5- VPP+: Positive charge pump output voltage connection
- J6-GND: Positive charge pump output voltage return connection
- J7- VPN-: Negative charge pump output voltage connection
- J8-GND: Negative charge pump output voltage return connection
- JP1-APD: Power supply for the APD pin
- JP2-Vo_ADJ: Adjust the output voltage
- JP3-EN: EN pin input jumper. Place a jumper across EN and pin 3 to turn on the IC, place a jumper across EN and pin 1 to turn off the IC

3 Schematic, Bill of Materials, and Board Layout

This section provides the TPS61391EVM schematic, bill of materials (BOM), and board layout.

3.1 Schematic

Figure 1 shows the EVM schematic.

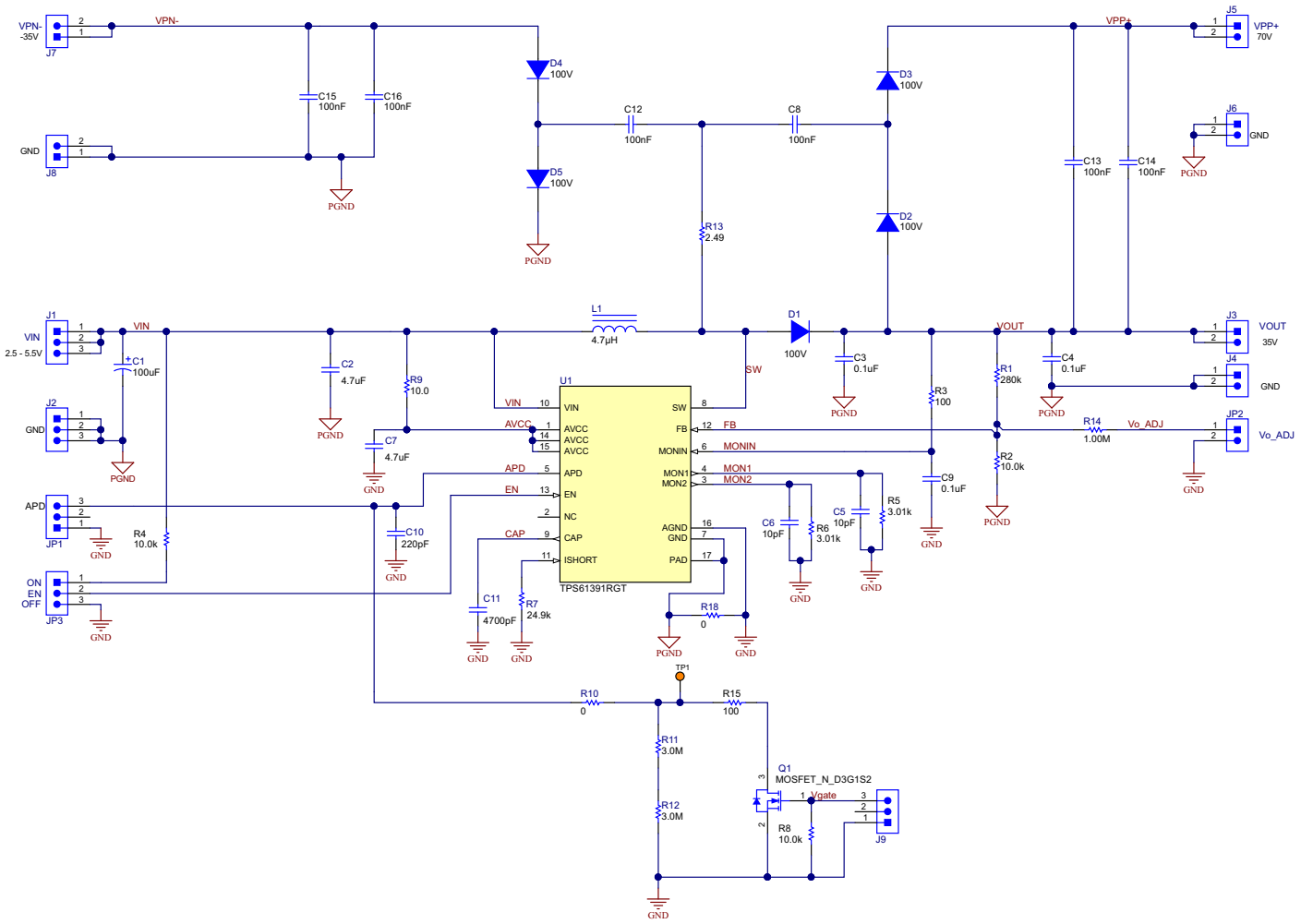

Figure 1. TPS61391EVM Schematic

3.2 Bill of Materials

Table 2 lists the EVM BOM.

Table 2. TPS61391EVM Bill of Materials

Designator	QTY	Value	Description	Package	Part Number	MFG
C2,C7	1	4.7 µF	CAP, CERM, 4.7 µF, 10 V, ±10%, X5R, 0603	0603	0603ZD475KAT2A	AVX
C3, C4, C8, C9, C12, C13, C14, C15, C16	9	0.1 µF	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, 0603	0603	GRM188R72A104KA35D	MuRata
C5, C6	2	10 pF	CAP, CERM, 10 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GCM1885C2A100JA16D	MuRata
C10	1	220 pF	CAP, CERM, 220 pF, 100 V, ±5%, C0G/NP0, 0603	0603	GCM1885C2A221JA16D	MuRata
C11	1	4700 pF	CAP, CERM, 4700 pF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R2A472K080AA	TDK
D1, D2, D3, D4, D5	5	100 V	Diode, Switching, 100 V, 0.25 A, AEC-Q101, SOD-123	SOD-123	BAS16D-E3-08	Vishay-Semiconductor
J1, J2, J9, JP1, JP3	5		Header, 100 mil, 3 × 1, Tin, TH	Header, 3 PIN, 100 mil, Tin	PEC03SAAN	Sullins Connector Solutions
J3, J4, J5, J6, J7, J8, JP2	7		Header, 100 mil, 2 × 1, Tin, TH	Header, 2 PIN, 100 mil, Tin	PEC02SAAN	Sullins Connector Solutions
L1	1	4.7 µH	Inductor, Shielded, Metal Composite, 4.7 µH, 1.2 A, 0.252 Ω, SMD	2 × 1.6 mm	DFE201612E-4R7M=P2	MuRata
Q1	1	100 V	MOSFET, N-CH, 100 V, 0.17 A, SOT-23	SOT-23	BSS123	Fairchild Semiconductor
R1	1	280 kΩ	RES, 280 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603280KFKEA	Vishay-Dale
R2, R4, R8	3	10.0 kΩ	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R3, R15	2	100 Ω	RES, 100, 0.5%, 0.1 W, 0603	0603	RT0603DRE07100RL	Yageo America
R5, R6	2	3.01 kΩ	RES, 3.01 k, 0.5%, 0.1 W, 0603	0603	RT0603DRE073K01L	Yageo America
R7	1	24.9 kΩ	RES, 24.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060324K9FKEA	Vishay-Dale
R9	1	10.0 Ω	RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEA	Vishay-Dale
R10, R18	2	0	RES, 0, 5%, 0.125 W, 0603	0603	MCT06030Z0000ZP500	Vishay/Beyschlag
R11, R12	2	3.0 Meg	RES, 3.0 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06033M00JNEA	Vishay-Dale
R13	1	2.49	RES, 2.49, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06032R49FKEA	Vishay-Dale
R14	1	1.00 Meg	RES, 1.00 M, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M00FKEA	Vishay-Dale
SH-JP1	1	1 × 2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1	1		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone
U1	1		85-V_{OUT} boost converter with current mirror and sample / hold, RGT0016C (VQFN-16)	RGT0016C	TPS61391RGT	Texas Instruments
C1	0	100 µF	CAP, TA, 100 µF, 16 V, ±10%, 0.1 ohm, SMD	7343-43	T495X107K016ATE100	Kemet

3.3 Board Layout

Figure 2 through Figure 5 illustrate the EVM board layouts.

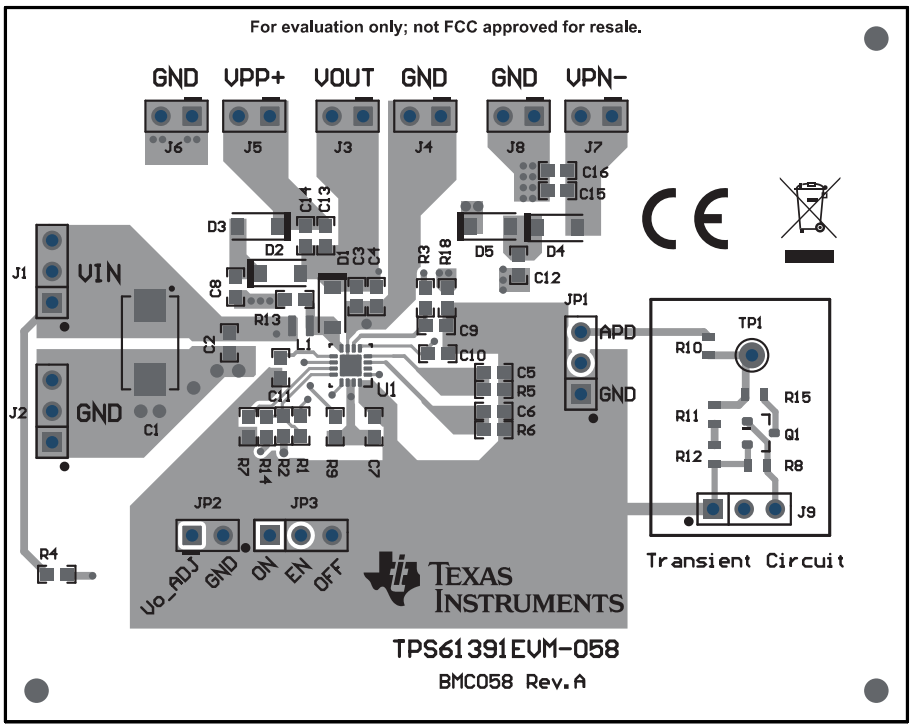

Figure 2. TPS61391EVM Top-Side Layout

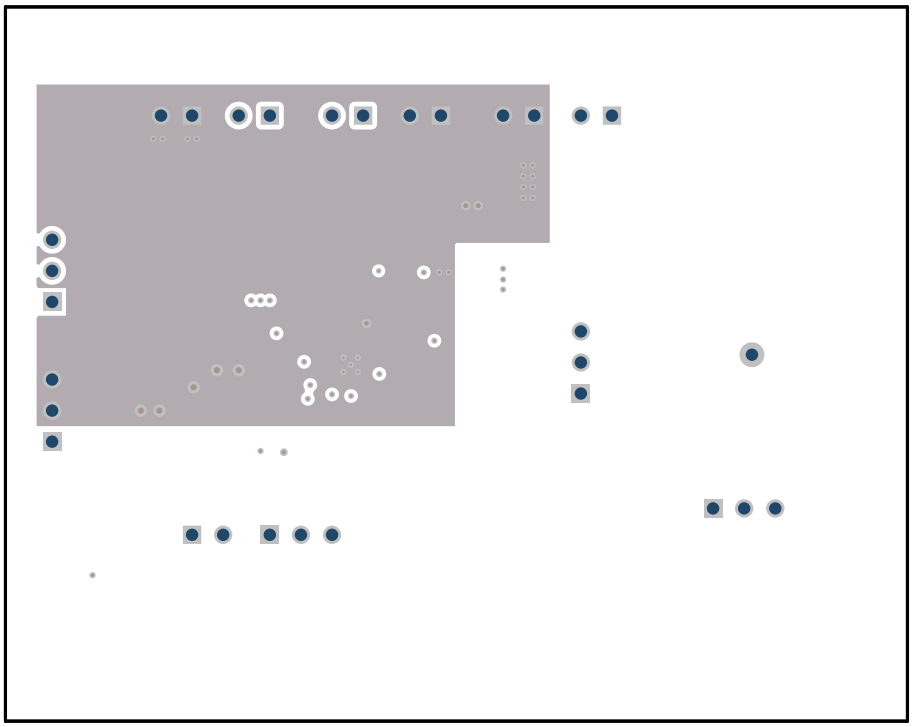

Figure 3. TPS61391EVM Inner Layer 1

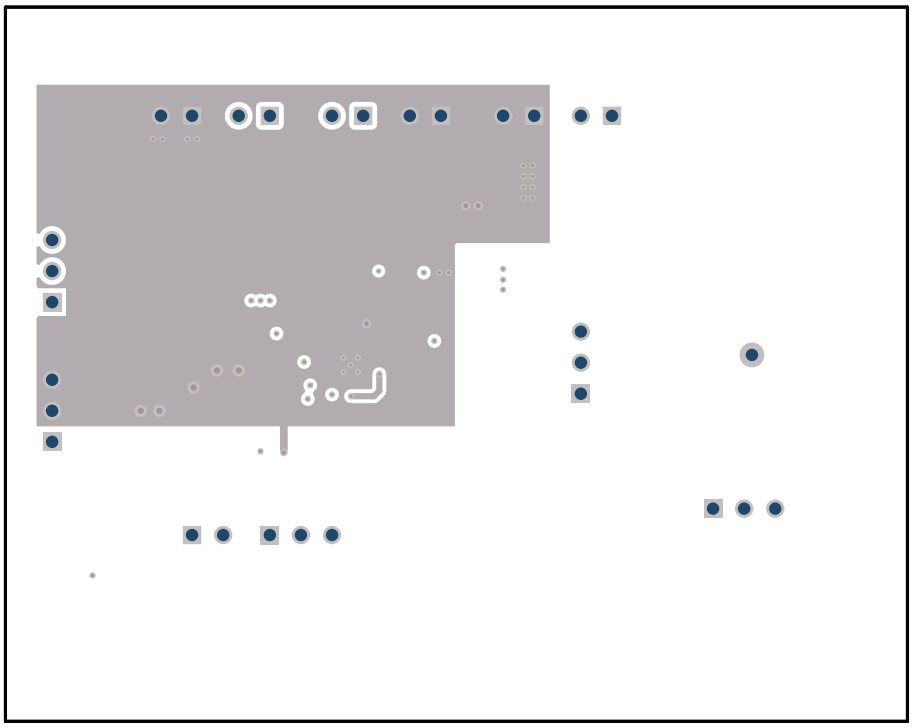

Figure 4. TPS61391EVM Inner Layer 2

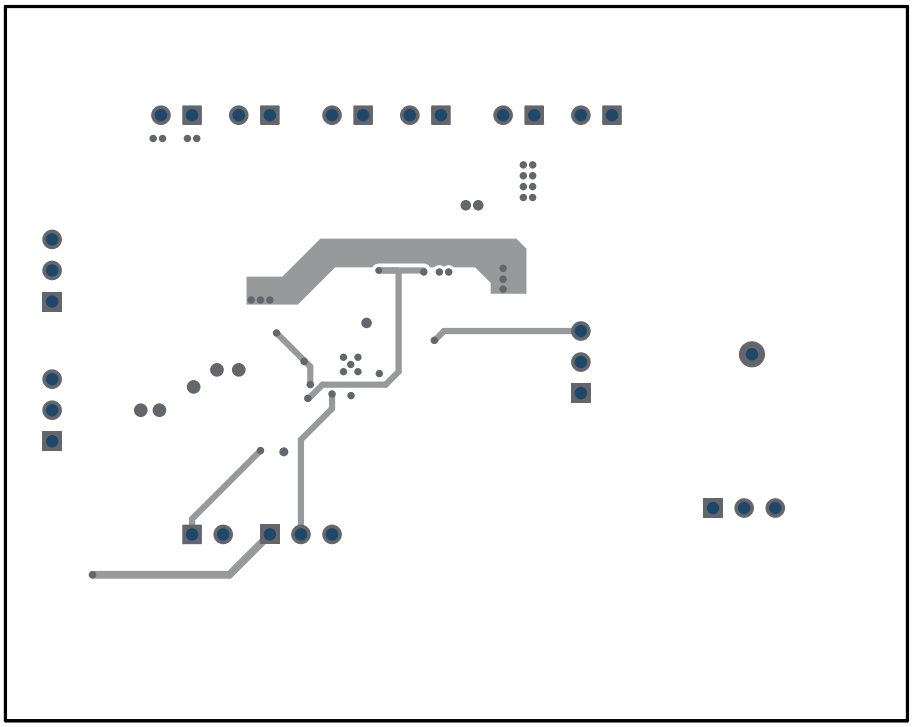

Figure 5. TPS61391EVM Bottom-Side Layout

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