User's Guide

TPS7H1101SPEVM User's Guide

Table of Contents

List of Figures

Trademarks

1 Introduction

This user's guide describes the characteristics, operation, and use of the TPS7H1101SP evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS7H1101-SP and the TPS7H1101A-SP ultra-low dropout (LDO) regulator.

It is a radiation-hardened LDO linear regulator that uses a PMOS pass element configuration. It operates over a wide range of input voltage, from 1.5 V to 7 V while offering excellent PSRR. The TPS7H1101A-SP features a precise and programmable foldback current limit implementation with a very-wide adjustment range. To support the complex power requirements of FPGAs, DSPs, or microcontrollers, the TPS7H1101A-SP provides enable on and off functionality, programmable soft start, current sharing capability, and a Power Good open-drain output. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the EVM.

1.1 Related Documentation

1. TPS7H1101A (SLVSDW6) Data Sheet

2 Description

The TPS7H1101SPEVM helps designers evaluate the operation and performance of the TPS7H1101A-SP ultra LDO regulator.

Table 2-1. Summary of Performance

Test Conditions	Output Current Range
V_{IN} = 1.5 V to 7 V	Max 3 A

The evaluation module is designed to provide access to the features of the TPS7H1101A-SP. Some modifications can be made to this module to test performance with various input and output voltages and loads. Please reference TI E2E™ support forums for information and questions related to this EVM.

3 Test Setup

3.1 Equipment

3.1.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 7-V at 5-A or higher is required.

3.1.2 Load Number 1

Electronic load, that is, Chroma 63640-80-80 module along with 63600-2 DC electronic load Mainframe or Decade Resistor Box.

3.1.3 Meters

Four (4) Fluke 75, (equivalent or better) or two (2) equivalent voltage meters and two (2) equivalent current meters.

The current meters must be able to measure 5 A current. Note: Shunt along with DVM can be used to monitor output current.

3.1.4 Oscilloscope

An Tektronix Oscilloscope, for example, DPO 7104CCurrent Probe Tektronix TCP202 or equivalent.

3.2 Bench Test Setup Conditions

3.2.1 Headers Description and Jumper Placement

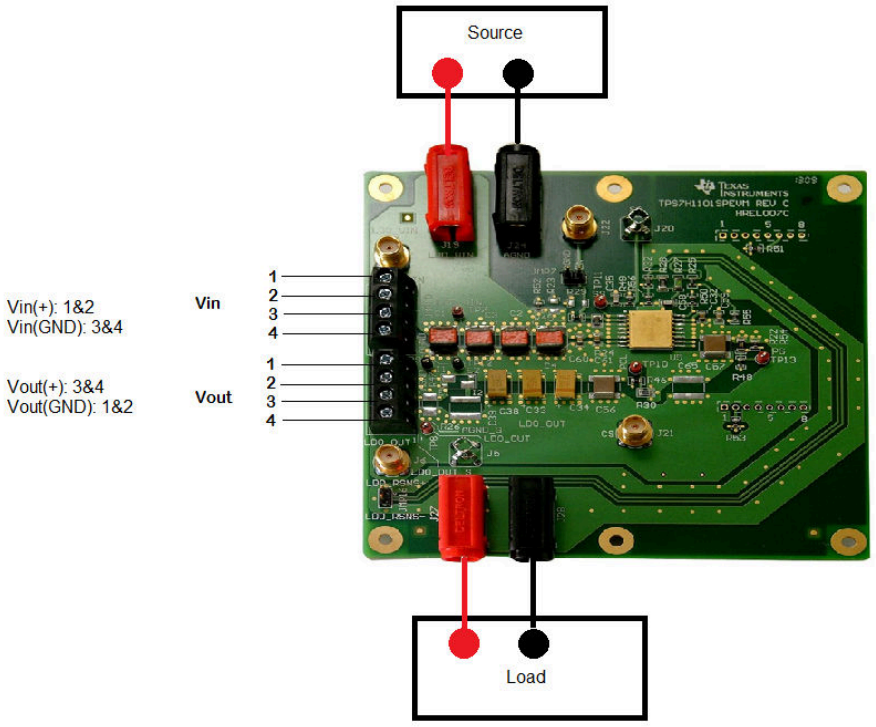

Figure 3-1. Headers Description and Jumper Placement

3.2.2 Testing

Table 3-1. Power Connectors

No.	Function
J19	V_{IN} input voltage connector (see Section 3.2.2 for V_{IN} range)
J24	V_{IN} input voltage connector to ground
J27	V_{OUT} output voltage connector
J28	V_{OUT} output connector to ground
J7	Vin_SMA
J22	EN_SMA
J20	SS_Probe
J5	LDO_OUT_Probe
TP8	LDO Vout measure point (+)
TP9	LDO Vout measure point (GND)
J6	LDO_OUT_SMA
TP7	LDO Vin measure point (+)
TP12	LDO Vin measure point (GND)
TP10	PCL
J21	CS_SMA
TP13	PG (Power Good)
TP11	SS
JMP10	V_{IN} alternative connection: 1,2 (+) and 3,4 (GND)
JMP8	V_{OUT} alternative connection 3,4 (+) and 1,2 (GND)

3.3 Power-Up Procedure

The following test proceedure and results are based on testing of the default configuration of the EVM. The EVM by default is configured to output 1.8 V.

Table 3-2. Test Results

	V_{OUTMIN}	V_{OUTMAX}	Current Limit	Current Foldback	
V_{OUT} = 1.8 V	1.76 V	1.836 V	< 3.8 A	< 1.9 A	**OUTPUT SET POINT**
I_{OUT} = 3 A	1.8166 V		3.5 A		**CURRENT LIMIT**

3.3.1 I_{OUT} and V_{OUT} Measurements

1. Make sure all power supplies in workstation are OFF.
2. Locate connectors J19 and J24.
3. Connect V_{IN}(+) to J19 and V(GND) to J24. Set it to 2.3 V.
4. Locate measure points TP7 and TP12.
5. Connect voltmeter: V_{IN}(+) to TP7 and V(GND) to TP12.
6. Locate connectors J27 and J28 and connect load here (be aware of polarities).
7. Locate measure points TP8 and TP9.
8. Connect voltmeter: V_{OUT}(+) to TP8 and V(GND) to TP9.
9. Output voltage should be per Table 2-1. This is done by setting R27 = 19.8 kΩ and R28 = 10 kΩ.

   V_{OUT} can be determined by equation highlighted below or per equation 1 in the data sheet.

$$V_{OUT} = \frac{(R_{27} + R_{28}) \bullet V_{REF}}{R_{28}} \quad (1)$$

   Where V_{REF} = 0.605 V.

3.3.2 Output Current Limiting

A resistor value R30 connected from PCL pin to GND determines the output current limit set point based on Equation 2.

Maximum programmable current limit is 3800 mA.

$$R_{pcl} = R_{30} = \frac{CSR(V_{ref})}{(I_{cl} - .0403)} \quad (2)$$

Where V_{REF} = 0.605 V, I_{cl} = programmable current limit (A), CSR = Current sense ratio (typical value = 52000).

CSR between I_{cs} pin and I_{OUT} can be measured as shown in Figure 3-2.

See Figure 3-3 for device Iload vs PCL pin current ranges.

- Make sure all power supplies in workstation are OFF.
- Connect V_{IN}(+) to J19 & V(GND) to J24 and set it to 2.3 V.
- Set V_{OUT} to 1.8V. (R27 = 19.8 kΩ and R28 = 10 kΩ)
- Connect load as previously instructed, set it to zero load.
- Increase I_{load} (steps of 0.100 A are suggested) until V_{load} starts to drop.
- Current limit trip point < 3.8 A.

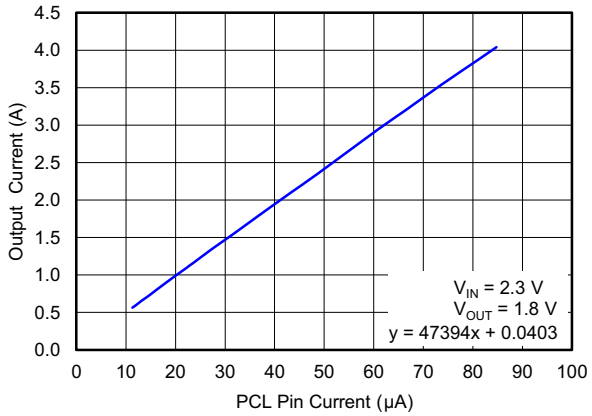

Figure 3-2. I_{OUT} (A) vs I_{PCL} (uA)

I_{LOAD} Vs I_{PCL} across CSR range

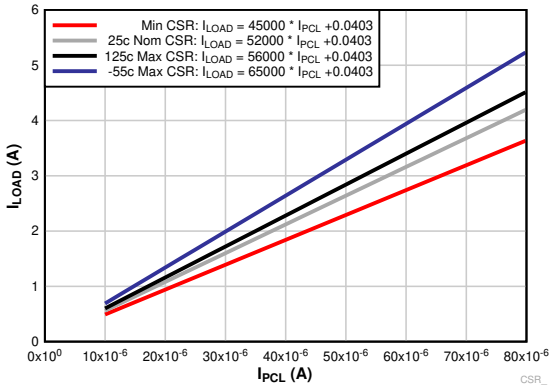

Figure 3-3. I_{OUT} (A) vs I_{PCL} (A) across CSR range

3.3.3 High-Side Current Sense

Monitoring the voltage at the CS pin will indicate voltage proportional to the output current. Figure 3-4 shows typical curve V_{CS} vs I_{OUT} for Vin = 2.28 V and R23 = 3.65 kΩ. A resistor connected from current sense (CS) pin to V_{IN} indicates voltage proportional to the output current.

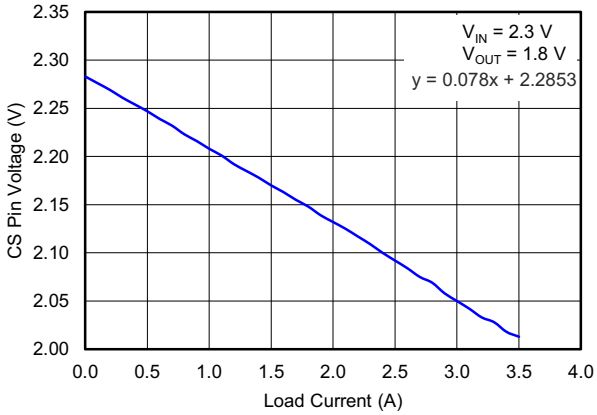

Figure 3-4. V_{CS} (V) vs I_{OUT} (A)

Monitoring current in CS pin (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMOSFET and the current sense MOSFET as shown in Figure 3-5. This plot shows that the CSR ratio is independent of V_{CS} voltage. Note that V_{CS} must be above 0.3V to insure proper biasing, and also must be greater than 0.9 x V_{REF} (0.544 V) to have foldback current limit enabled.

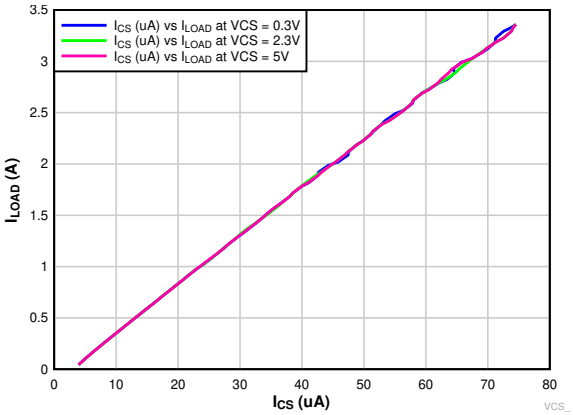

Figure 3-5. I_{OUT} (A) vs I_{CS} (A)

3.3.4 Current Foldback

1. When current sense (CS) pin is held high, foldback current limit is enabled. Shorting CS low will disable the foldback current limit.
2. With foldback current limit enabled, when current limit trip point is activated,
   a. Output voltage will drop low.
   b. output current will fold back to approx. 50% of the current limit trip point.

   This results in minimizing the power loss under fault conditions.

3.3.5 Power Good

Power good pin is an open-drain connection, connect it high via pull up resistor to external voltage source. Power Good pin indicates the status of the output voltage.

3.3.6 Dropout Voltage

Drop out voltage (V_{DO}) is the difference between the input voltage and output voltage needed to maintain regulation. V_{DO} vs I_{OUT} is highlighted in Figure 3-6.

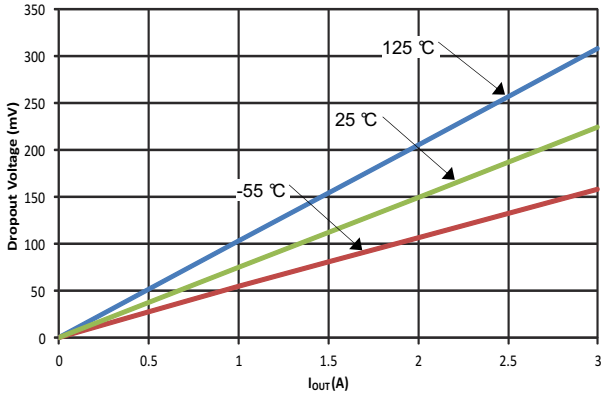

Figure 3-6. V_{DO} vs I_{OUT}

3.3.7 Transient Response

Waveforms below indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Output voltage overshoot / undershoot

Channel 2: Step load in current

Channel 3: Input voltage

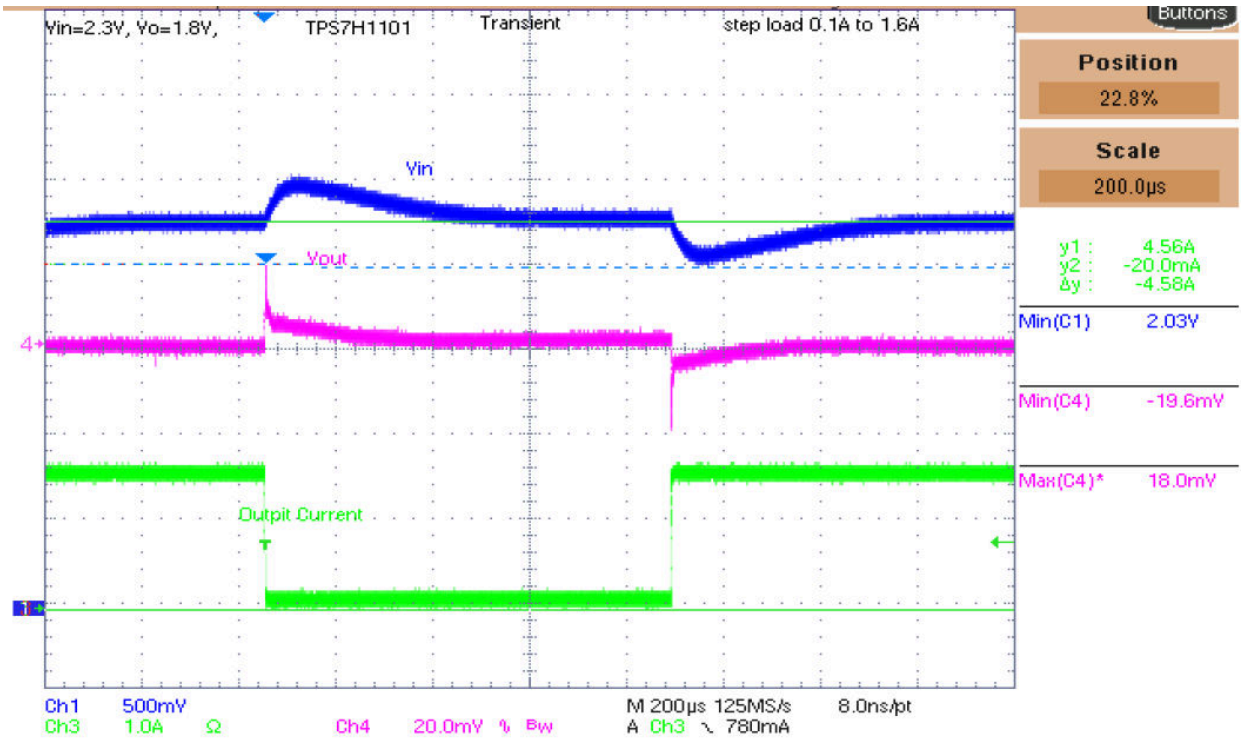

Figure 3-7. Load Transient Response: Step Load 0.1 A to 1.6 mA

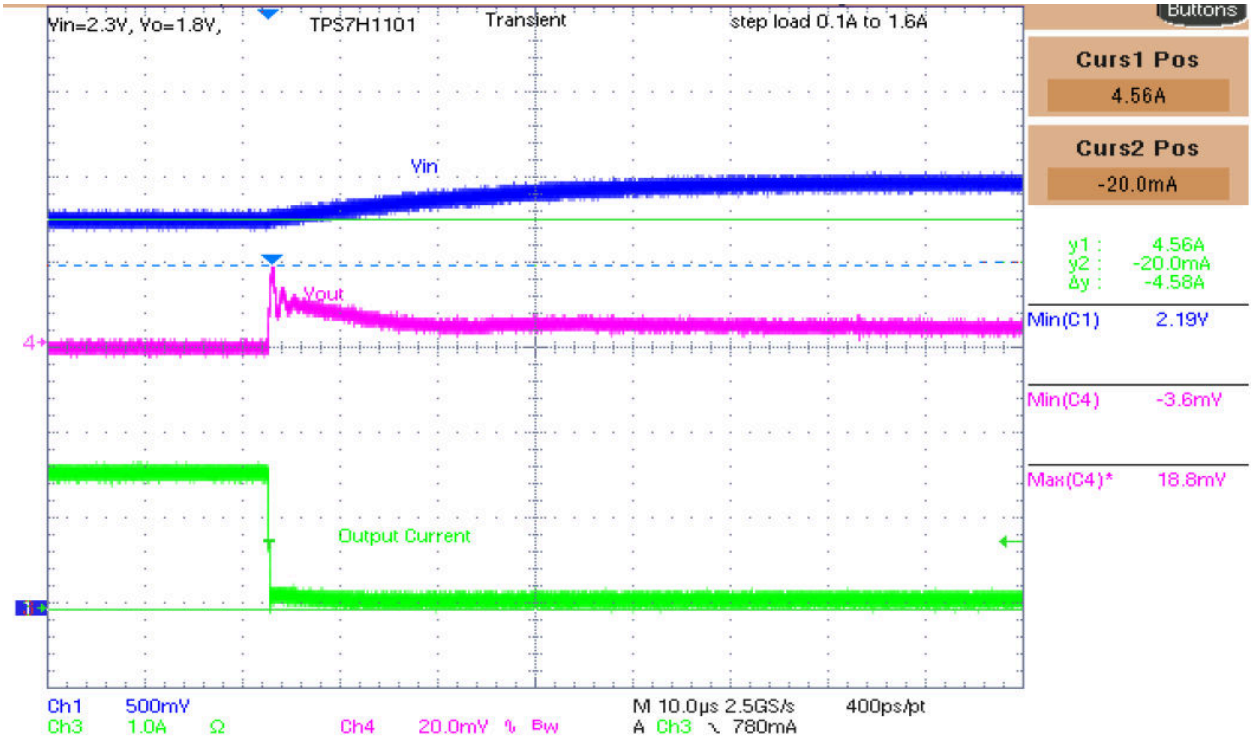

Figure 3-8. Expanded View Overshoot

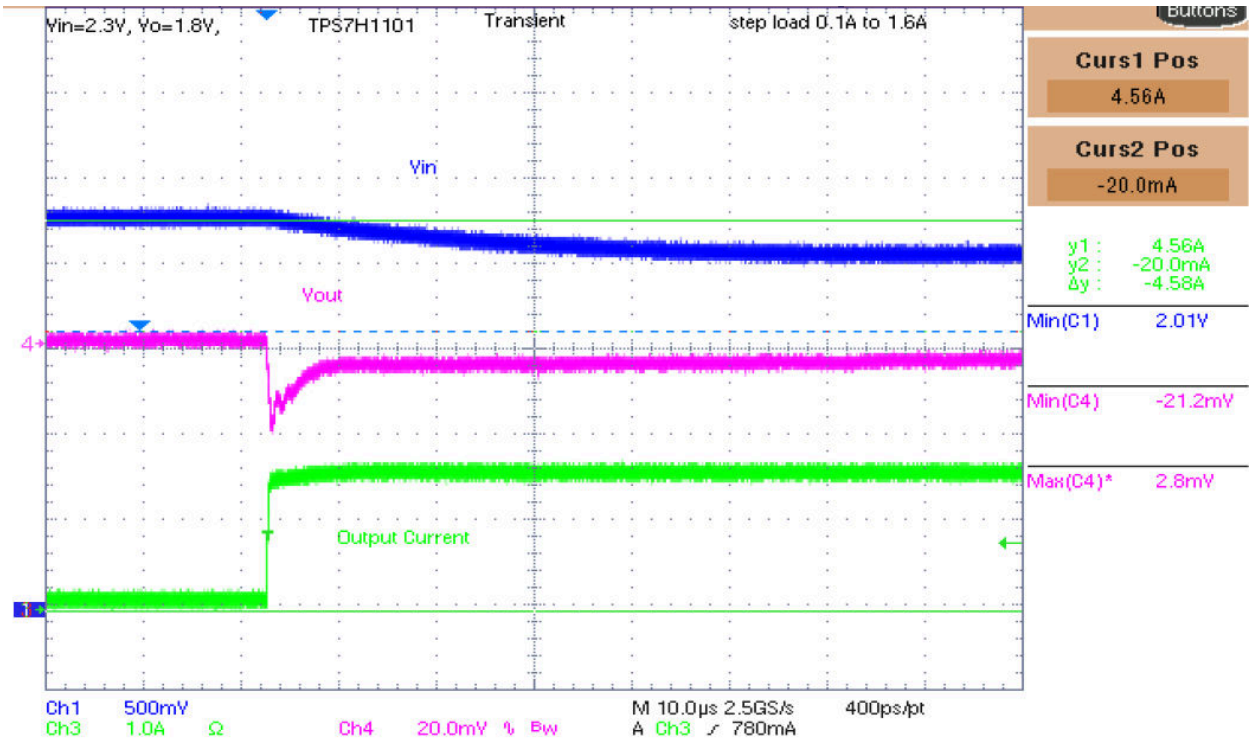

Figure 3-9. Expanded View Undershoot

3.3.8 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled.

- In parallel mode CS pin of LDO#1 must be connected to PCL pin of LDO#2 via a series resistor (3.75 kΩ) and CS pin of LDO#2 must be connected to PCL pin of LDO#1 via series resistor (3.75 kΩ).
- In parallel configuration R30 (resistor from PCL to GND) and R23 (resistor from CS pin to V_{IN}) must be left open (unpopulated).

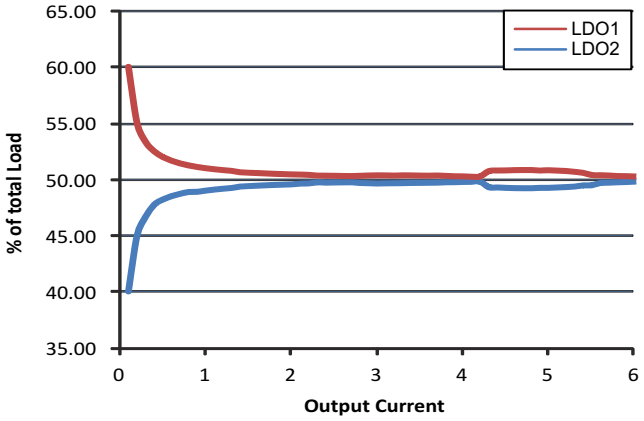

Figure 3-10. Current Sharing LDO_1 and LDO_2

3.3.9 Soft-Start

Connecting a capacitor on CS pin to GND (C_{35}) slows down the output voltage ramp rate. The soft-start capacitor will charge up to 1.2 V.

$$C_{35} = \frac{t_{ss} \bullet I_{ss}}{V_{REF}} \quad (3)$$

Where:

t_{ss} = Soft-start time

I_{ss} = 2.5 µA

V_{REF} = 0.605 V

3.3.10 Enable and Disable

EVM can be disabled via pulling the enable pin low via shorting JMP7-1 (Enable) to JMP7-2 (GND). Enable pin is tied high to V_{IN} via R24 (20 kΩ) resistor, thus keeping the EVM enabled.

Alternately, EVM can also be disabled via pulling SS pin (U6 pin 1) low via an external circuit comprising of 2N7002 MOSFET as shown in Figure 3-11. A high signal at the gate of Q100 will discharge the SS pin and disable the device.

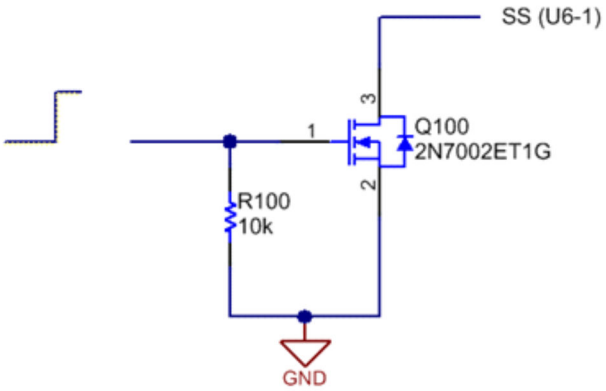

Figure 3-11. Disabling the LDO via Soft-Start Pin

3.3.11 Turn-Off

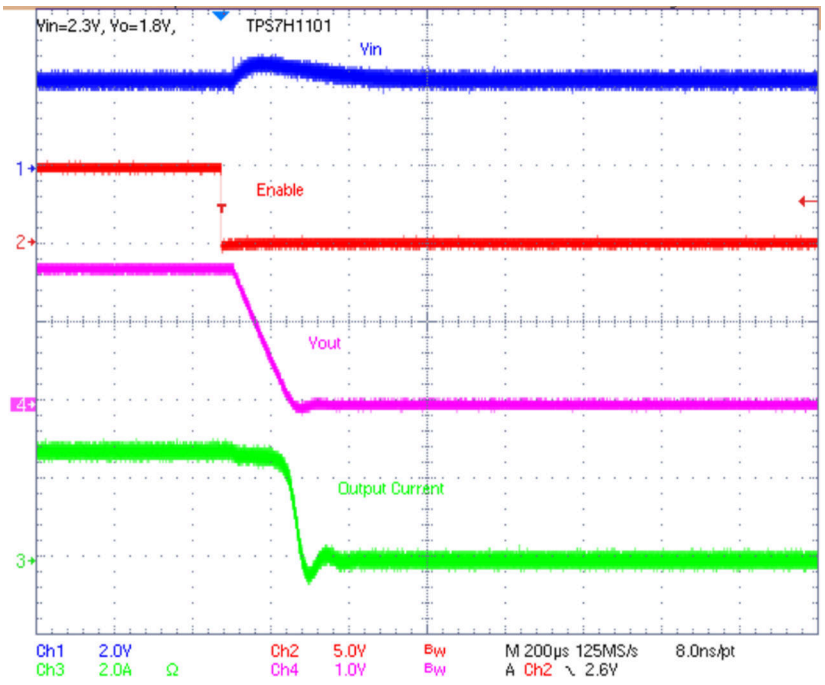

Figure 3-12. Turn-Off

4 Board Layout

4.1 EVM Layout Flexibility

The EVM is layed out to provide flexibility for the customer evaluation thus providing test points and or cold nose probes to monitor various critical nodes of the design as highlighted in the schematic.

Additionally, placeholder is provided thus one can add esr in series with the output capacitor (R47 in series with C39) thus making it easier to evaluate performance with increased capacitor esr.

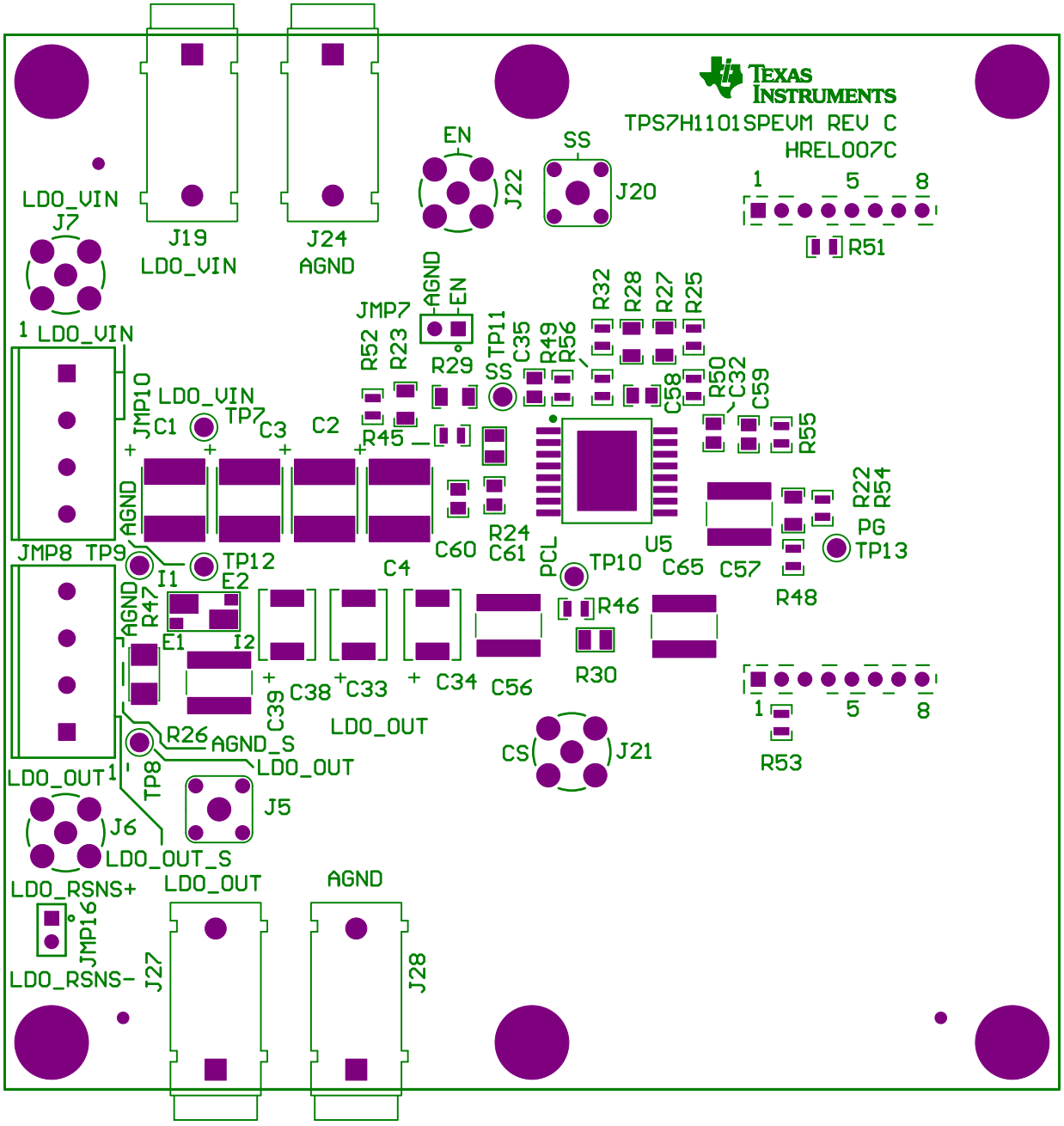

Figure 4-1. Component Placement (Top Side)

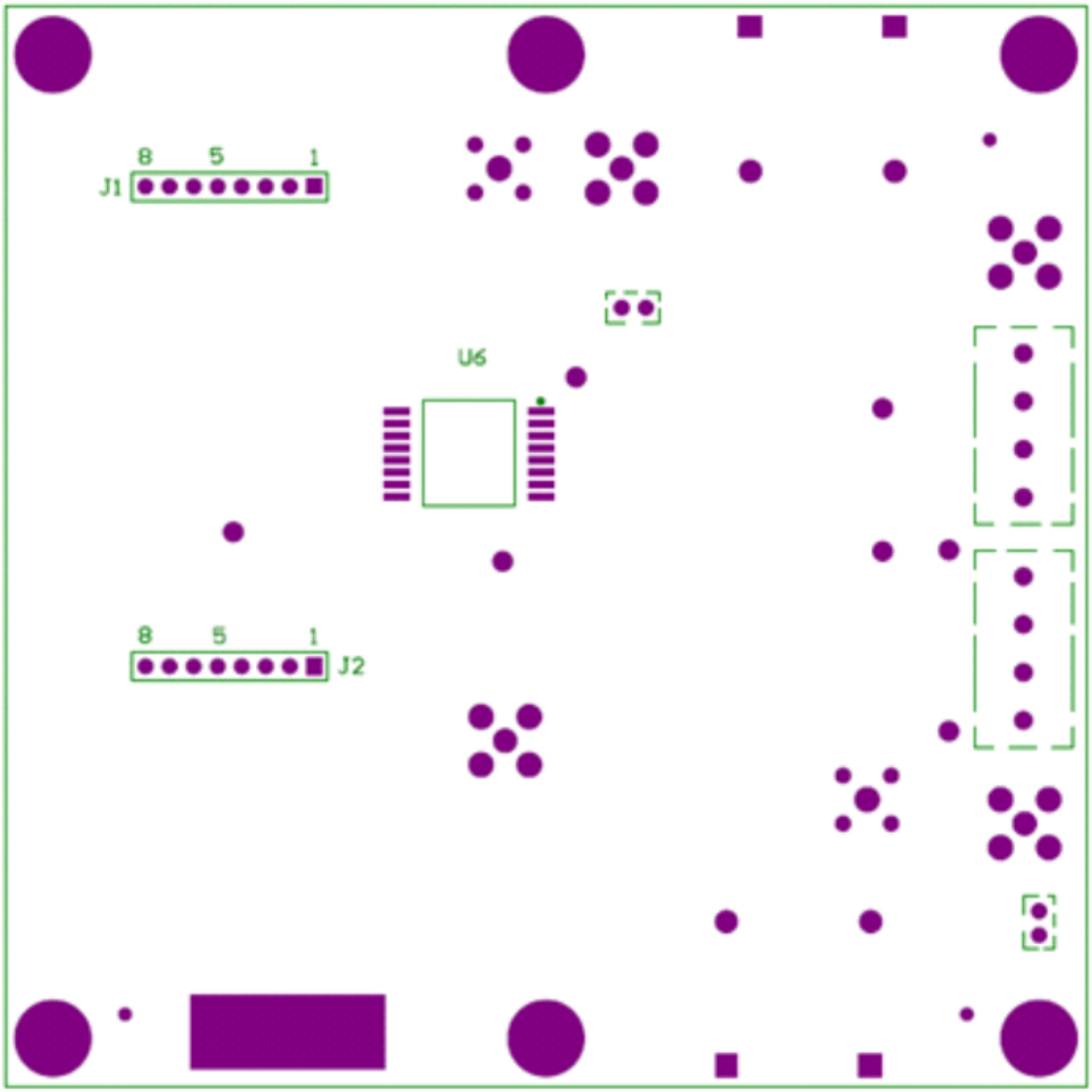

Figure 4-2. Component Placement (Bottom Side)

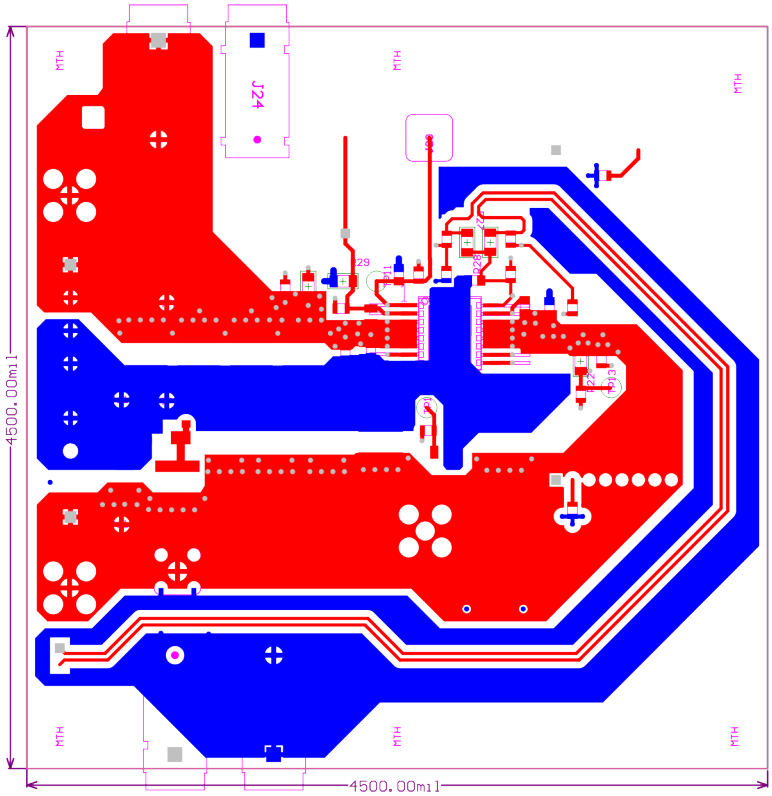

Figure 4-3. PCB Layout (Top Layer)

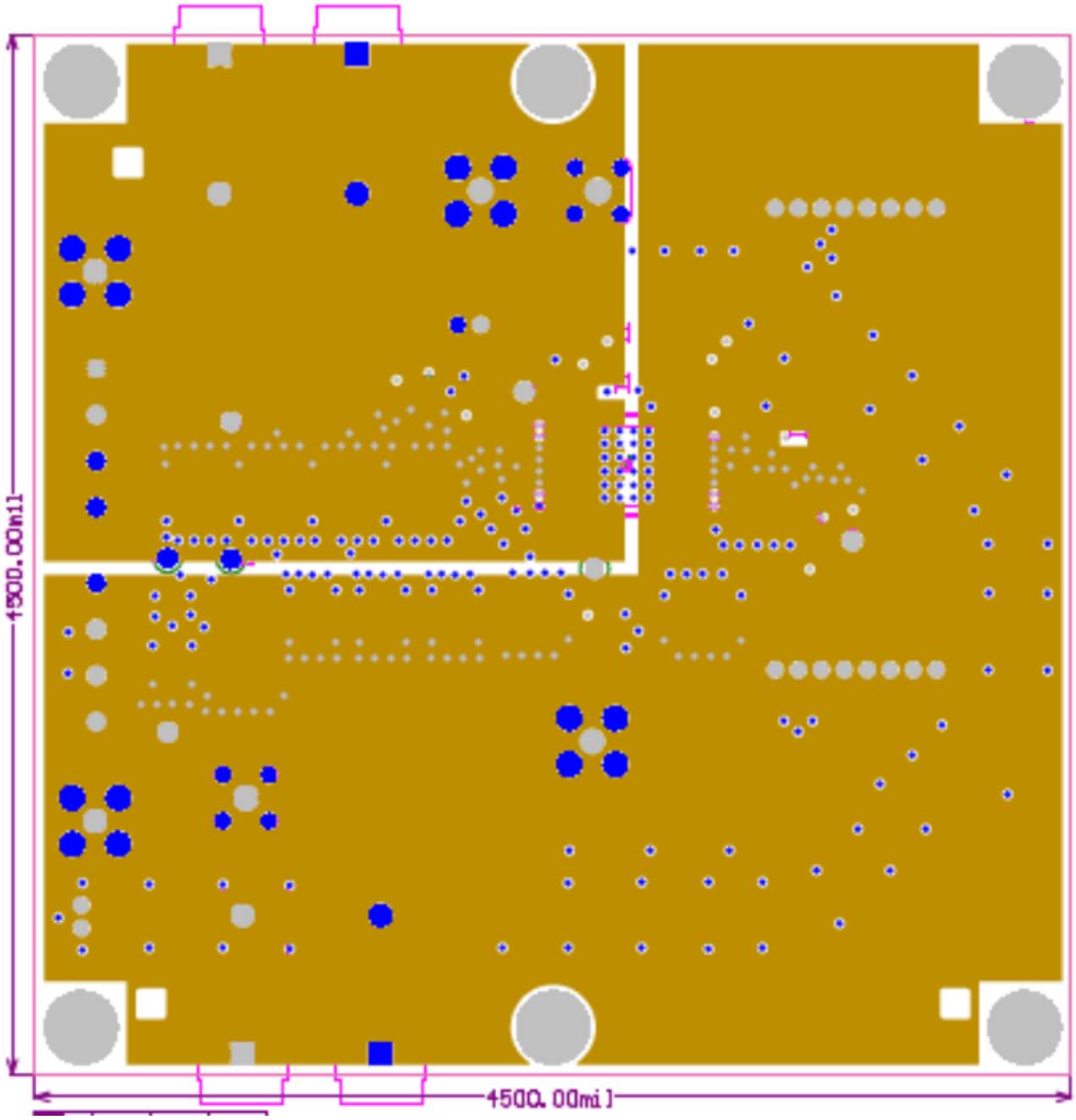

Figure 4-4. Board Layout - Second Layer (Mid Layer 1)

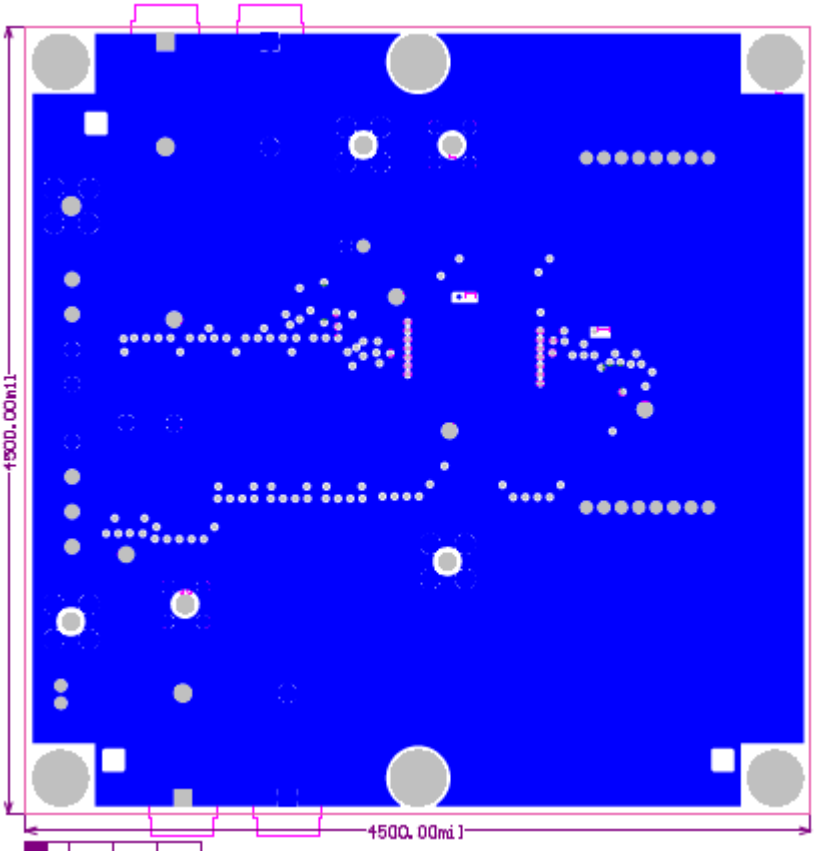

Figure 4-5. Board Layout - Third Layer (Mid Layer 2)

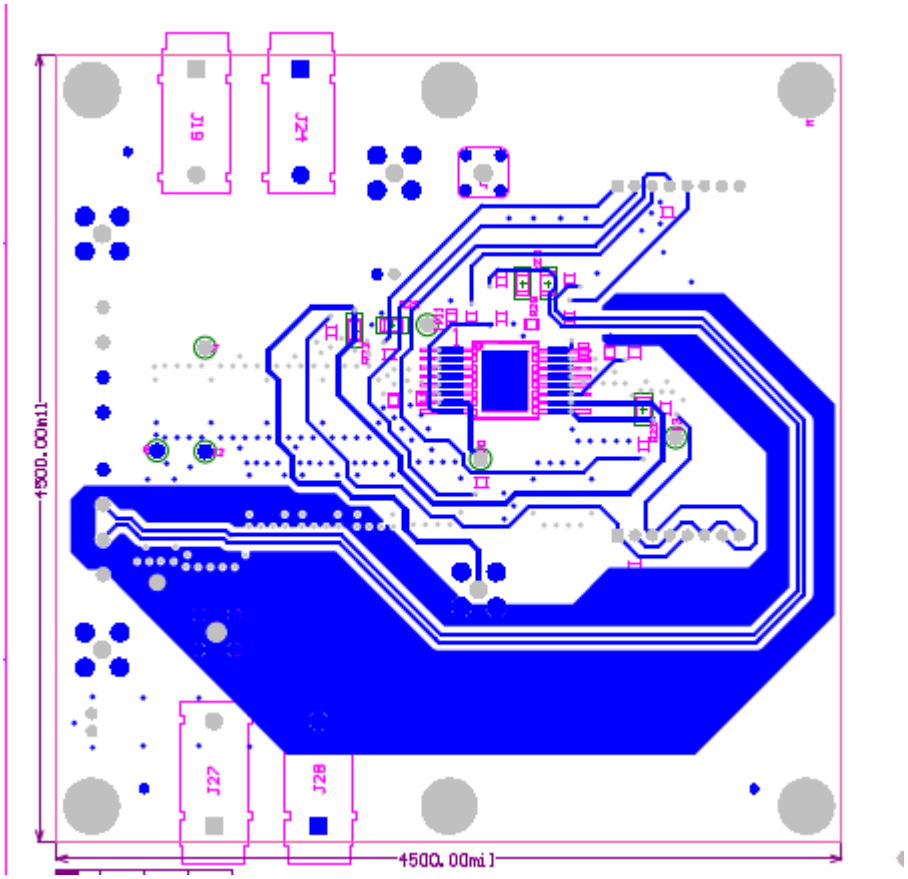

Figure 4-6. Board Layout - Fourth Layer (Bottom Layer)

5 Schematic and Bill of Materials

The following pages contain the TPS7H1101HTEVM schematic and bill of materials.

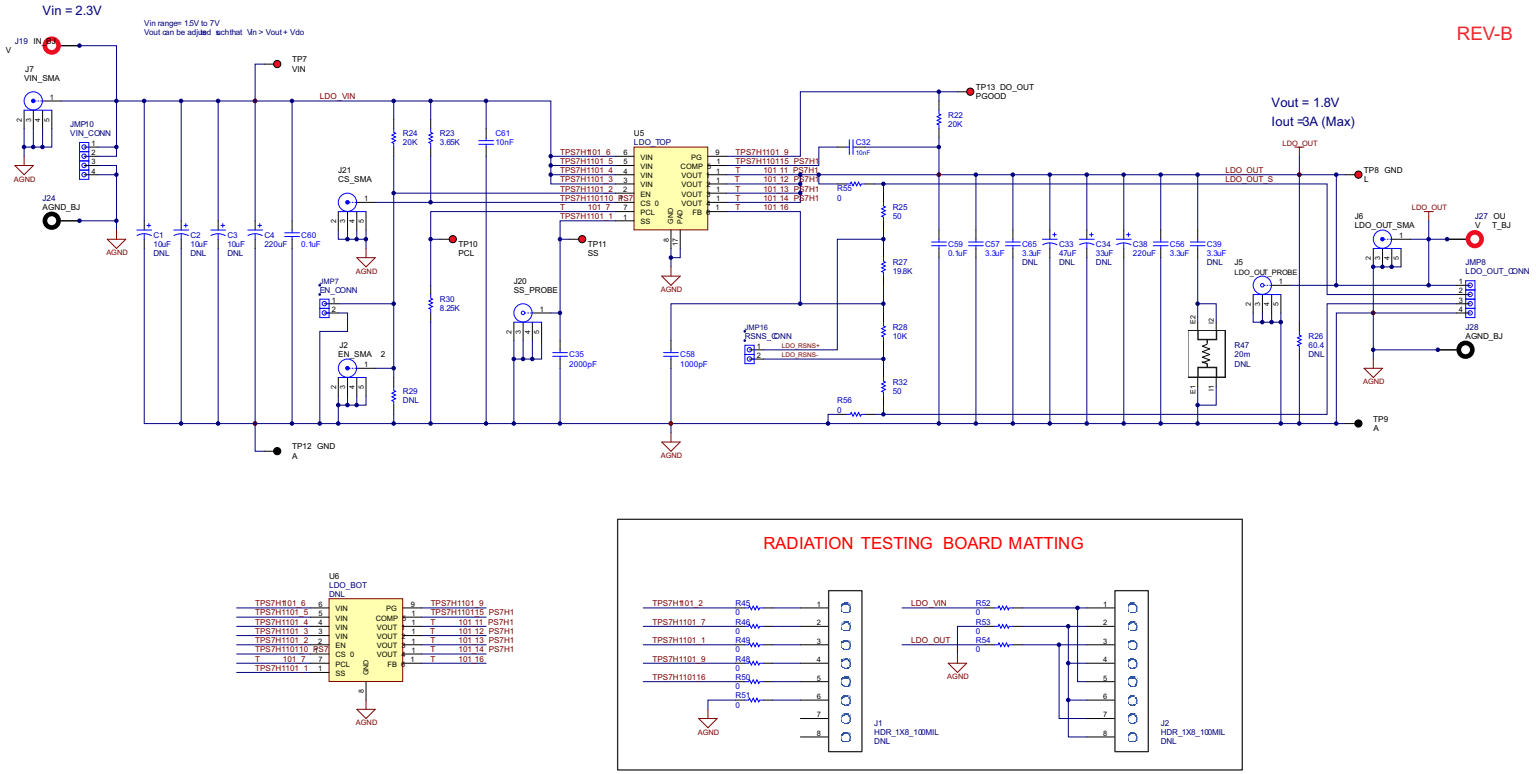

Figure 5-1. TPS7H1101SPEVM Schematic

Table 5-1. TPS7H1101SPEVM Bill of Materials

ITEM NO.	QTY	DESIGNATOR	VALUE	FOOTPRINT	MANUFACTURER	PART NO.	DESCRIPTION
1	1	C4	220uF	7260-38	Kemet	T543X227M016ATE035	CAP TANT 220UF 16V 20% 2917
2	2	C32,C61	10nF	0805	Kemet	C0805C103K3RACTU	CAP CER 10000PF 25V 10% X7R 0805
3	1	C35	2000pF	0805	Kemet	C0805C202J3GACTU	CAP CER 2000PF 25V 5% NP0 0805
4	1	C38	220uF	7260-38	Kemet	T543X227M016ATE035	CAP TANT 220UF 16V 20% 2917
5	2	C56,C57	3.3uF	2225	MURATA	GRM55DR71H335KA01L	CAP CER 3.3UF 50V 10% X7R 2220
6	1	C58	1000pF	0805	Kemet	C0805C102J3GACTU	CAP CER 1000PF 25V 5% NP0 0805
7	2	C59,C60	0.1uF	0805	Kemet	C0805C104K3RACTU	CAP CER 0.1UF 25V 10% X7R 0805
8	1	J5			Tektronix	131-5031-00	Compact Probe Tip Circuit Board Test Points, TH
9	1	J6			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
10	1	J7			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
11	1	J19			DEM Manufacturing	571-0500	Standard Banana Jack, insulated, 10A, red
12	1	J27			DEM Manufacturing	571-0500	Standard Banana Jack, insulated, 10A, red
13	1	J20			Tektronix	131-5031-00	Compact Probe Tip Circuit Board Test Points, TH
14	1	J21			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
15	1	J22			Emerson	142-0701-231	Connector, TH, SMA, 50 ohms
16	2	J24,J28			DEM Manufacturing	571-0100	Standard Banana Jack, insulated, 10A, black
17	1	JMP7		HDR_1X2_TSW	Samtec	TSW-102-07-G-S	CONN HEADER 2POS .100 SGL GOLD"
18	1	JMP8		HDR_1X4_39544	Molex	39544-3004	CONN TERMINAL BLOCK 4POS 5.08MM
19	1	JMP10		HDR_1X4_39544	Molex	39544-3004	CONN TERMINAL BLOCK 4POS 5.08MM
20	1	JMP16		HDR_1X2_TSW	Samtec	TSW-102-07-G-S	CONN HEADER 2POS .100 SGL GOLD"
21	1	R22	20kΩ	1206	Stackpole	RNCP1206FTD20K0	RES 20K OHM 1/2W 1% 1206 SMD
22	1	R23	3.65kΩ	1206	Panasonic	ERJ-8ENF3651V	RES 3.65k, 1/4W, 1%, 100ppm/C 1206
23	1	R24	20kΩ	0805	Stackpole	RNCP0805FTD20K0	RES 20K OHM 1/4W 1% 0805 SMD
24	2	R25,R32	50Ω	0603	Panasonic	ERJ-3EKF49R9V	RES 49.9 OHM 1/10W 1% 0603 SMD
25	1	R27	19.8kΩ	1206	Stackpole	RNCF1206BTE19K8	RES 19.8K OHM 1/8W 0.1% 1206
26	1	R28	10kΩ	1206	Stackpole	RNCS1206BKE10K0	RES 1/8W 10K OHM 0.1% 1206
27	1	R30	49.9kΩ	0805	Stackpole	RMCF0805FT49K9	RES 49.9K OHM 1/8W 1% 0805 SMD
28	11	R45,R46,R48,R49,R50,R51,R52,R53,R54,R55,R56	0Ω	0603	Panasonic	ERJ-3GEY0R00V	RES 0.0 OHM 1/10W 0603 SMD
29	1	TP7			Keystone	5000	Test Point, TH, Miniature, Red
30	1	TP8			Keystone	5000	Test Point, TH, Miniature, Red
31	2	TP9,TP12			Keystone	5001	Test Point, TH, Miniature, Black
32	1	TP10			Keystone	5000	Test Point, TH, Miniature, Red
33	1	TP11			Keystone	5000	Test Point, TH, Miniature, Red
34	1	TP13			Keystone	5000	Test Point, TH, Miniature, Red
35	1	U6		CFP (HKS)	Texas Instruments	TPS7H1201SHKS	IC installed as lid down at the back of the board

Table 5-1. TPS7H1101SPEVM Bill of Materials (continued)

ITEM NO.	QTY	DESIGNATOR	VALUE	FOOTPRINT	MANUFACTURER	PART NO.	DESCRIPTION
36	4				Keystone	2029K-ND	Standoffs
37	4				Pencom	4-40X1/4PH-PN-MS-SS	Screws for standoffs
38	1		HREL008		Any	HREL008	PCB
39	1				Brady	THT-13-457-10	Label on the EVM under TI logo = TPS7H1201HTEVM
							HREL008-001
40	0	C1,C2,C3	10uF	7260-38_1	Vishay	T95R106K050LSAL	CAP TANT 10UF 50V 10% 2824
41	0	C33	47uF	7260-38	Kemet	T491X476M035AT	CAP TANT 47UF 35V 20% 2917
42	0	C34	33uF	7260-38	Kemet	T491X336K035AT	CAP TANT 33UF 35V 10% 2917
43	0	C39,C65	3.3uF	2225	MURATA	GRM55DR71H335KA01L	CAP CER 3.3UF 50V 10% X7R 2220
44	0	J1,J2	HDR_1X8_100MIL	HDR_1X8_BCS	SAMTEC	BCS-108-F-S-TE	SKT 8 POS 2.54mm Solder ST Thru-Hole
45	0	R29	DNL	1206	TBD	TBD	TBD
46	0	R26	60.4Ω	2010	Rohm	MCR50JZHF60R4	RES 60.4 OHM 1/2W 1% 2010 SMD
47	0	R47	20mΩ	RES_Y14870R02000B0R	VISHAY	Y14870R02000B0R	Current sensing chip resistor, 20m OHM, 0.1%
48	0	U5		CFP (HKR)	Texas Instruments	TPS7H1101SHKR	IC installed as lid up at the top of the board

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2015) to Revision B (October 2020)	Page
• Updated to include TPS7H1101A version (throughout document)	2
• Updated to restructure document layout consistency	2
• Updated Power-Up information	4
• Updated Rpcl equation	4
• Updated plots and description for V_{CS}	5

Changes from Revision * (September 2013) to Revision A (October 2015)	Page
• Corrected the y-axis scale in the image	5

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265