Radiation Report

CDCM7005-SP Single-Event Effects Report

ABSTRACT

Single-Events Effects (SEE) testing was performed by HIREX Engineering, an Alter Technology Company. The testing did not detect any incidence of Single-Event Latchup (SEL) or Single-Event Functional Interrupt (SEF) up to a linear energy transfer (LET) of 60 MeV-cm ^{2} /mg (Xenon ions at normal incidence), the highest LET tested. Five types of Single-Event Upsets (SEU) were detected. The report is attached in Appendix A.

In the report, Type I SEUs were reported as the DUT output phase never recovered its original state unless re-synchronization was done. The failure mode being non-recoverable was being investigated further by TI during a June 2013 test trip to Texas A&M (TAMU). It was found that the phase could also be recovered by scrubbing (rewriting) the registers.

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Trademarks

1 Test Setup

Attempts were made to duplicate the HIREX test at TAMU on June 27, 2013. The test setup is shown in Figure 1-1. The ion specie used in the test was Cu in the 15MeV cocktail with an LET of 20.5MeV-cm^2/mg. The DUT was running at 80Mhz with divide-by-16 and LVCMOS on output Y0. The DUT was mounted on an evaluation board. A spare board was used as a control unit.

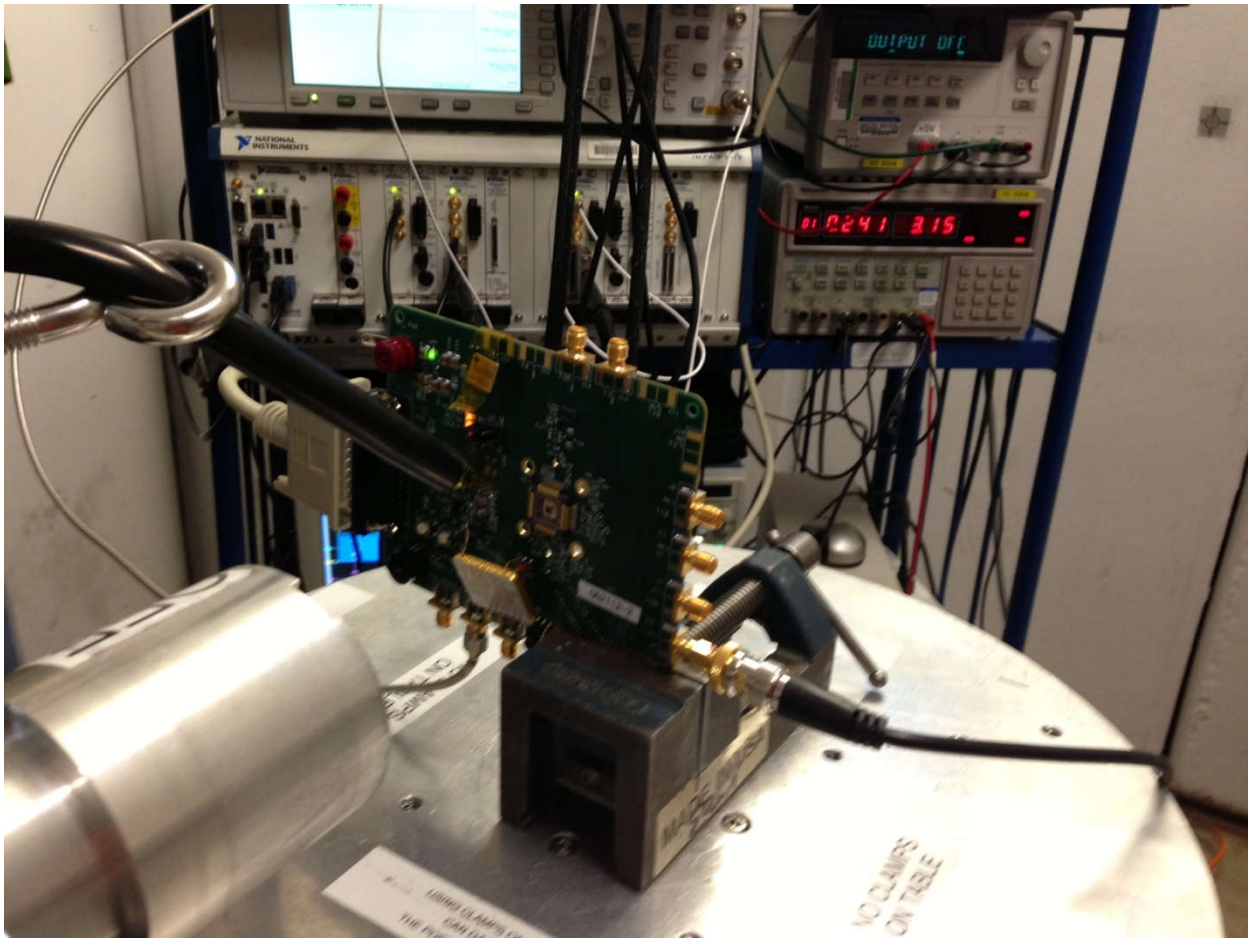

Figure 1-1. Test setup at TAMU

All supplies were set at 3.15V and the DUT board was at ambient temperature.

An RF clock source was used to supply 79.9942Mhz clock to an Agilent 8133A external trigger input. The 8133A was set to divide-by-16 on trigger, and the output being a square wave with about 2.5v signal swing. This signal drove the primary ref clock input of CDCM7005.

The CDCM7005 was programmed with all defaults except feedback mux to the phase detector was set to divide-by-16 and Y0 set to LVCMOS outputs. With proper input frequency, this configuration allows the CDCM7005 to lock. A square jitter-eye mask was programmed into the scope. Any waveform deviated from the square wave output by more than about 500ps to 1ns would be detected.

The Y0 output was connected to a Tektronix DPO7104 oscilloscope. The output waveform had mask set to include the area under the rising pulse of the output. Any deviation of the rising pulse will cross the mask, and the scope will indicate this by several means: 1) a pixel will be drawn in the mask, and 2) a failing waveform count (a count indicates an SEU) will index for each pass that the signal is in the mask. The scope screen was manually observed along with position of the signal within the mask. For example, the 180 phase shift might not cause the waveform to fail, but it was visually seen and recorded.

Note, this experimentation was not an attempt to recreated a full SEE test and create cross sections, but primarily to reclassify the type 1 SEU noted in the HIREX report.

2 Results

The results of the 4 ion runs are shown in Table 2-1.

Table 2-1. Ion Runs

Run	Time	Flux (ions/cm^2-s)	Fluence (ions/cm^2)	Notes/Work Needed
1	8:33	1 x 10^3	1 x 10^5	No SEU, 98 seconds
2	8:40	1 x 10^4	1 x 10^6	mulitple SEU, saw phase shifts, and locked in 180 phase shift.
3	8:45	5 x 10^3	1 x 10^6	1-2ns phase shifts, scrubbed fixed it (3x), several were self fixing,
4	8:54	1 x 10^4	1.7 x 10^6	lost the signal scrub fixed it, several 1-2ns shifts, scrubs fixed it, recovered at end of run

During the first run at 1x10^3 ions/cm^2-s, no errors were detected to a fluence of 1 x 10^5 ions/cm^2.

The flux was increased to 1 x10^4 ions/cm^2-s and ran to a fluence of 1 x10^6 ions/cm^2, and multiple upsets were detected. There were two type of upsets detected. One was a 180° phase shift, and the other a small phase shift on the order of approximately 1ns. Counting the number of upsets was difficult due to slow lock time recovery and manual scrubbing. In every case, the device was manually scrubbed (registers rewritten) and passing waveform resumed. This was slightly difficult to tell for certain, as a new SEU would occur before it would stabilize out.

The flux was lowered to 5 x 10^3 ions/cm^2-s and an ion run was done to 1 x10^6 ions/cm^2, the results of both 180° phase shifts and small phase offsets were confirmed. Several errors self-recovered without scrubbing.

In final run, the flux was set at 1 x10^4 ions/cm^2-s and run to a fluence of 1.7 x 10^6 ions/cm^2. In one case, the Y output became static. Scrubbing restored proper operation.

3 Conclusion

Some SEUs recovered to normal operation without any intervention. Type 1 SEUs as described in the attached HIREX report can be recovered by scrubbing the registers. Software to trigger periodic scrubbing of the registers of the CDCM7005 is determined to be the mitigation technique of choice.

4 Appendix A HIREX CDCM7005-SP Single Event Effects Report

HIREL EXPERTISE
HIREX ENGINEERING
a company of Alter Technology

ALTER TECHNOLOGY
Member of TÜV NORD

SINGLE EVENT EFFECTS

Test report

Test Type:	Heavy ions
Part Types:	CDCM7005-SP
Part Description:	3.3V High Performance Rad Tolerant Class V, Clock Synchronizer and Jitter Cleaner
Package:	CQFP-52
Part Manufacturer:	Texas Instruments
Test facility:	RADEF, University of Jyväskylä, Jyväskylä, Finland
Test Date:	November 2011

Hirex reference :	HRX/SEE/0376	Issue : 01	Date: November 30th, 2011
Written by:	M. Grandjean	Test Engineer	
Authorized by:	F.X. Guerre	Study Manager	

RESULTS SUMMARY

Test facility: RADEF, University of Jyväskylä, Jyväskylä, Finland
Test date: November 2011
Device description:

Part type:	CDCM7005-SP
Part description:	3.3V high performance Rad tolerant class V, clock synchronizer and jitter cleaner.
Package:	CQFP-52
Date code:	0831
Die dimension:	2.5 mm x 2.5 mm

SEL

One SEL was recorded on the core supply of the sample SN 5 during the run 71 with a fluence of 1E7 ions.cm² a LET of 120 MeV.cm²/mg (Xenon ion with 60 ° tilt angle) a core and IO voltage supplies of 3.5 V a charge pump supply of 3.0 V and a temperature of 125 °C.

SEFI

No SEFI was detected up to a LET of 60 MeV.cm²/mg.

SEU

SEUs were detected and recorded during the test. During the data analysis process 5 types of SEUs were defined and SEUs were classified. The Figure 1 summarizes the SEU cross-sections per device of the 5 types of SEU.

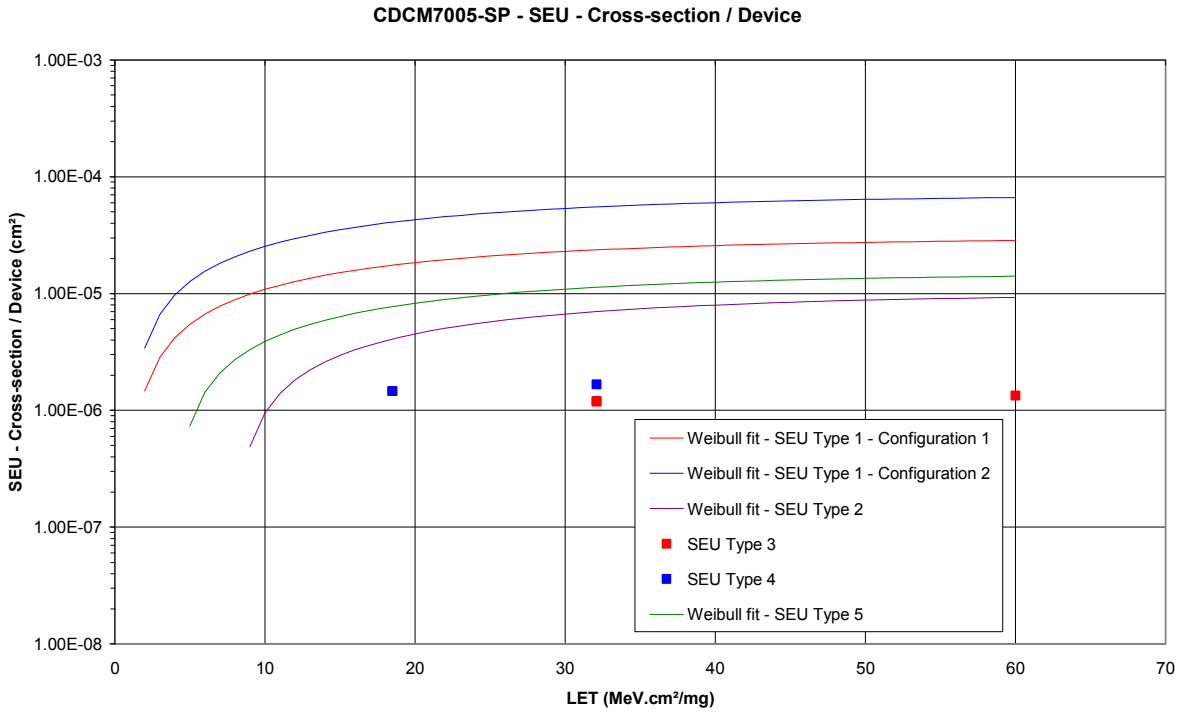

Figure 1 - SEU cross-section per device

SET

SET were detected and recorded on Vbb channel (bias voltage output). The Vbb SET saturation cross-section is about 3E-5 cm² and the LET threshold around 10 MeV.cm²/mg. The sensitivity of Vcp channel (charge pump output) to SET could not be reliably estimated due to a bad functionality of the channel of the digitizer. No SET was detected on Y0 channel (DUT output 0 configured to be LVPECL). Y2B channel (DUT output 2 configured to be LVCMOS) is supposed to be equivalent to Y0 channel because large noise spikes prevent the detection of eventual SET.

DOCUMENTATION CHANGE NOTICE

Issue	Date	Page	Change Item	
01	30/11/2011	All	Original issue	

Contributors to this work:

Michael Grandjean — Hirex Engineering
Volker Lahr — Tesat

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1 Introduction

This report presents the results of heavy ion irradiation characterization carried out on the CDCM7005-SP. This device is a 3.3V high performance Rad tolerant class V, clock synchronizer and jitter cleaner from Texas Instruments.

6 samples were tested at RADEF, University of Jyväskylä, Jyväskylä, Finland on November 2011 under HIREX Engineering responsibility.

2 Applicable and Reference Documents

2.1 Applicable Documents

AD-1. Hirex proposal HRX/PRO/3247 issue 1 dated May 10th, 2011.
AD-2. CDCM7005-SP datasheet, SGLS390C - JULY 2009 - REVISED APRIL 2010

2.2 Reference Documents

RD-1. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100

3 Device information

3.1 Device procurement

7 samples were delivered to HIREX. 6 of those samples were soldered, opened and prepared for irradiation test. The left over sample was kept as spare. All prepared samples were verified fully functional before the test campaign.

3.2 Device description

Part type:	CDCM7005-SP
Part description:	3.3V high performance Rad tolerant class V, clock synchronizer and jitter cleaner.
Package:	CQFP-52
Marking:	5962-0723001VXC CDCM7005MHFG-V THA 8A-R 0831A Q
Marking numbers:	116 – 119 – 040 – 221 – 042 – 149 – 029
Serial numbers:	Serialized from SN 1 to SN 7
Date code:	0831
Die dimension:	2.5 mm x 2.5 mm

3.3 Device identification

Photo 1 - Top marking

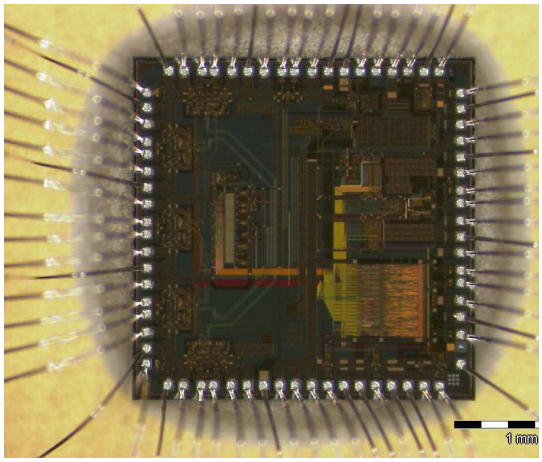

Photo 2 - Die view

Photo 3 - Die marking

Figure 2 - Device identification

3.4 Samples identification

The following Table 1 makes the correspondence between the marking number written on the top of the device cover and the serial number arbitrarily taken on the serialization process of the samples.

Serial Number	Marking number
1	040
2	042
3	119
4	149
5	221
6	029
7	116

Table 1 - Samples identification

4 RADEF Facility

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.

The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multi-cusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula,

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

4.1 Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm. The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.

The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-through can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.

A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

4.2 Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis. A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.

4.3 Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different sizes and shapes are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.

At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

4.4 Used ions

The following Table 2 summarizes the used ions during the test campaign.

Ion	Beam energy (MeV)	Range (Si) (µm)	LET* (MeV.cm^2/mg)
20 Ne+6	186	146	3.6
40 Ar+12	372	118	10.1
56 Fe+15	523	97	18.5
82 Kr+22	768	94	32.1
131 Xe+35	1217	89	60

*: measured LET at surface

Table 2 - Used ions

5 Test set-up

The test system is based on a Virtex-5 FPGA from XILINX. It has 168 I/O including 44 LVDS channels. The set of test board includes a DUT power supplies controller which manages the DUT power supplies up to 24 independent channels. A temperature control and regulation system is added to heat the DUT whenever needed. Ambient temperature is used otherwise. The communication between the under vacuum test system and the computer running the controlling GUI software is made using a 100 MBit/s Ethernet link. The Figure 3 displays the principle of the test system used for heavy ion tests.

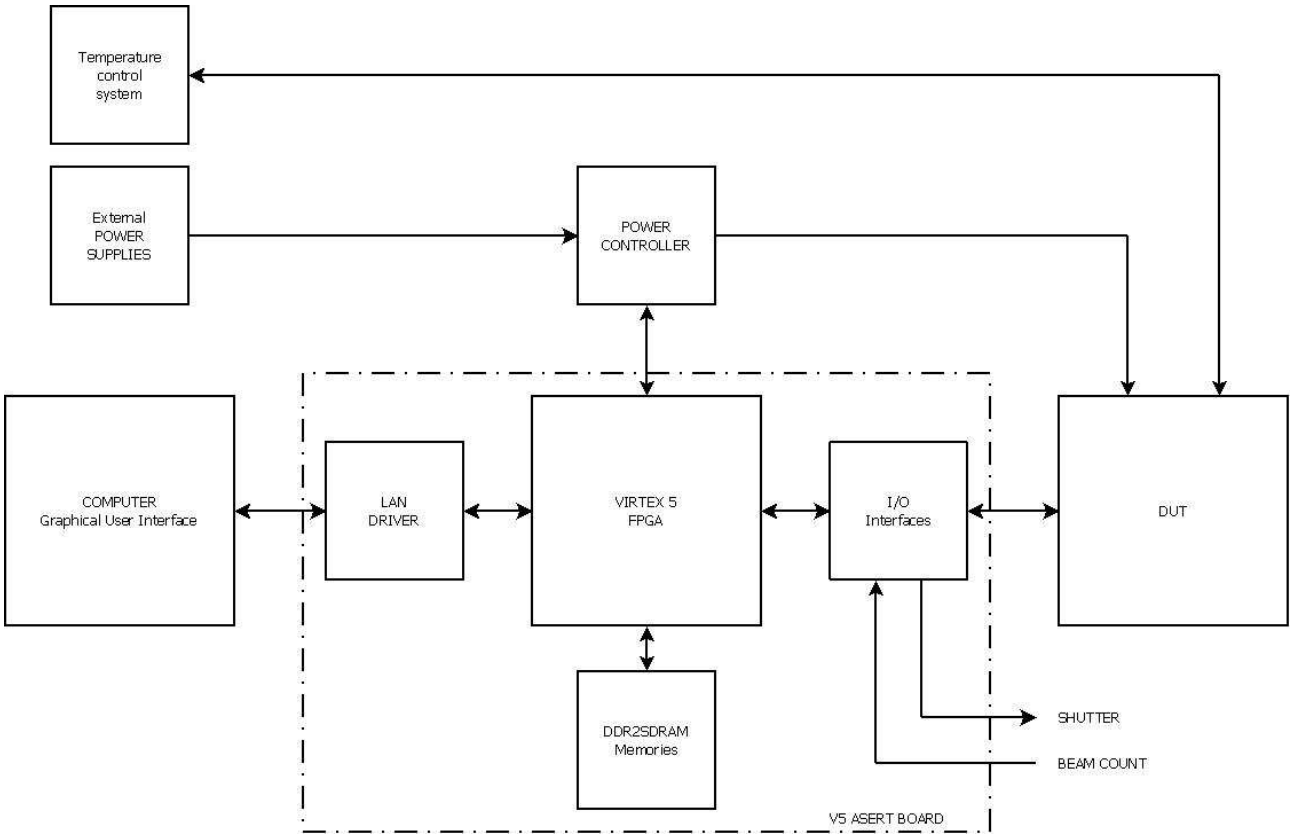

Figure 3 - Heavy ion test set-up

The DUT side of the tester is composed of one board called Device Interface Board (DIB) as shown on the Figure 4. This DIB receives on top in the middle a sample directly soldered and connects directly on the tester. It implements all the necessary bias components, power supply connectors and decoupling capacitors. A thermal path is integrated to the PCB to allow the access of the thermal pad of the device from the bottom of the PCB. A temperature sensor was placed in close contact to the package of the sample using thermal compound.

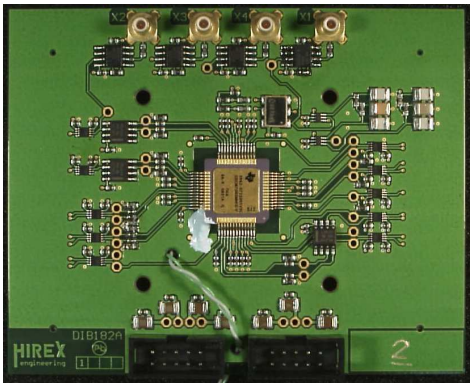

Figure 4- Device Interface Board

5.1 Test and device configurations

The Figure 5 highlights the bias principle used during the tests and the Figure 6 details the schematic of the bias. The device was clocked with an input frequency (Fin) of 100 MHz. The used VCXO was a 100 MHz VCXO referred FVCXO-PC73B-100.00 from Fox Electronics.

The configuration of the device was made through the SPI interface.

Two different configurations of the device, having each a different set of 3rd order passive loop filter characteristics, were used. The configuration values as well as the 3rd order passive loop filter characteristics were given by TESAT. The Table 3 details the parameters of both configurations. All parameters here below unspecified were kept at the default values (specified in AD-2). The 3rd order passive loop filter used was the same as the one on the typical application diagram of AD-2.

Both configurations result in:

- DUT Y output clocks synchronized to Fin with a frequency of 6.25 MHz.
- PLL lock, VCXO status and REF status at a static high logic level.

Parameter	Configuration 1	Configuration 2
Y0	LVPECL	LVPECL
Y1	LVPECL	LVPECL
Y2	LVCMOS	LVCMOS
Y3	LVCMOS	LVCMOS
Y4	LVPECL	LVPECL
M Divider	1	1024
N Divider	1	1024
Fb Divider	1	1
Yx Divider	16	16
M & N Delays	0	+ 1750 ps
Charge Pump	0.2 mA	3 mA
ADLOCK	0	0
LOCKW [1:0]	00	00
LOCKC [1:0]	00	00
R1 (KΩ)	30	330
R2 (KΩ)	3	1
C1 (pF)	10	2.7
C2 (nF)	100	100
C3 (pF)	100	100

Table 3 - Device configurations

SEEs were detected and recorded by supervising the DUT outputs as summarized on the Table 4:

DUT Output	SEU Monitored	SET Monitored
PLL Lock	✓	
VCXO Status	✓	
REF Status	✓	
Y0	✓	✓
Y1	✓	
Y2	✓	✓
Y3	✓	
Y4	✓	
3rd order passive loop filter		✓
Vbb		✓

Table 4 - DUT outputs monitors

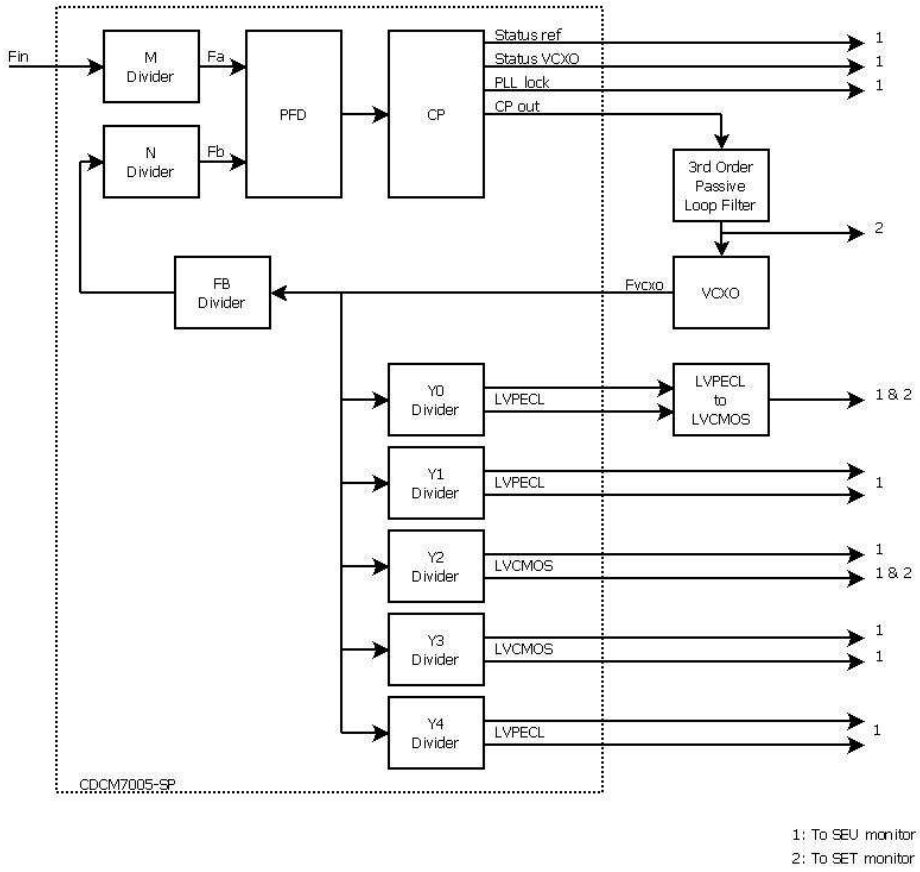

Figure 5 - Bias diagram

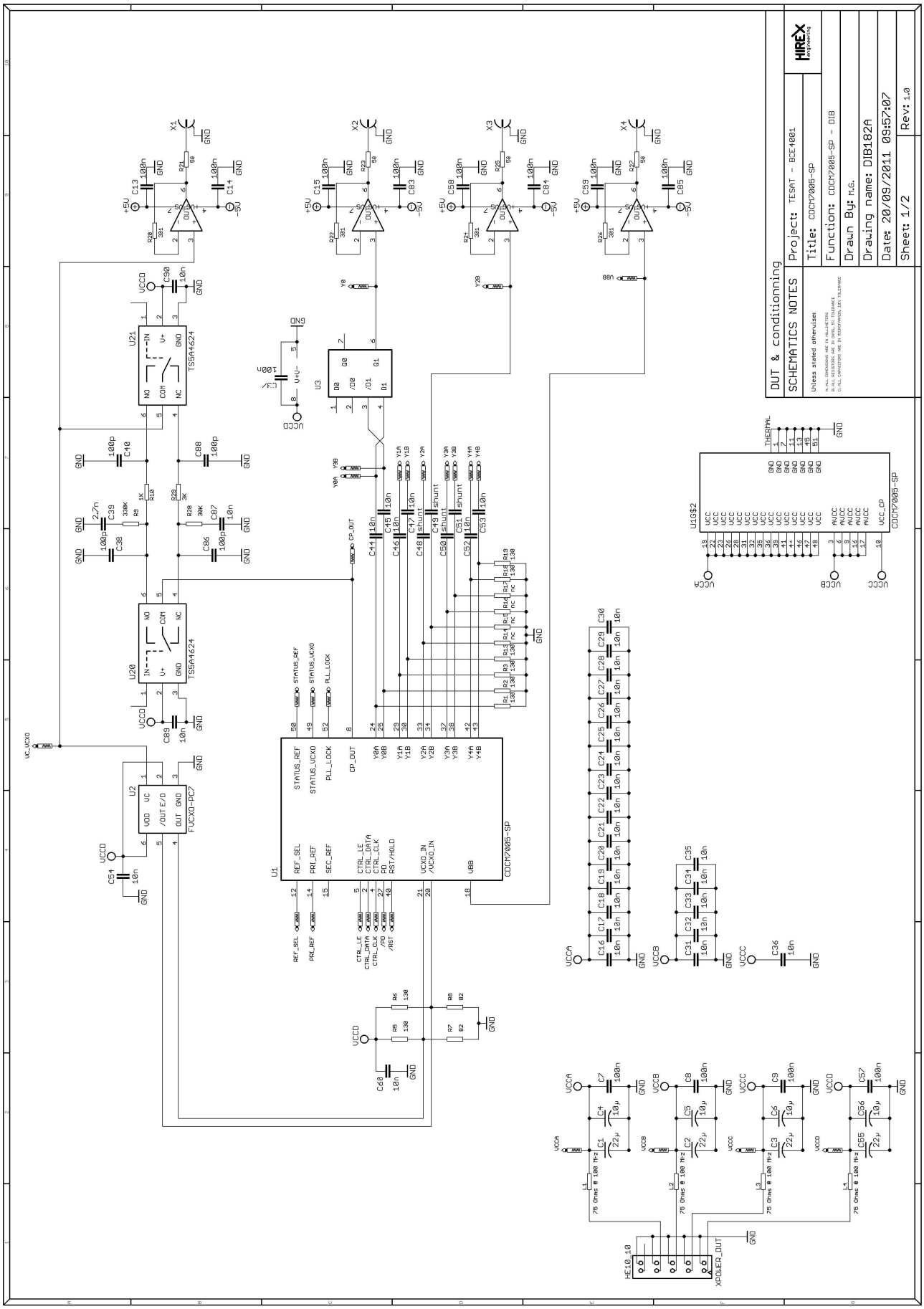

Figure 6 - Bias schematic

5.2 Test sequences

The SEFI, SEU and SET test sequence was:

Power on
Configure device
Loop
    Test (for a specified time)
End loop

Each time a SEFI was flagged a SEFI process was triggered. The SEFI process performed the device power cycle followed by a device configuration.

In the goal to keep the device powered on during the SEL test, the SEFI system was inhibited and the sequence modified to include repetitive re-configuration of device to keep as much as possible the device in nominal mode. The SEL test sequence was as follow:

Power on
Loop
    Configure device
    Test (for a specified time)
End loop

5.3 SEU Test principle

Right after powering-up the device, it is configured through the SPI interface using one of the two different configurations. When the configuration is effective (device outputs are stable), a model pattern is synchronized to the DUT output clocks (Ys) by a synchronization process. The synchronization process uses a 6.25 MHz reference clock signal inputting shift registers made of 8 registers clocked with a frequency of 50 MHz. Compared to the DUT output clock, the best phase aligned register output is then selected using a multiplexer over the 8 register outputs. Each model pattern of the DUT Y outputs is independent. The PLL lock, VCXO status and REF status patterns are static to the high logic level.

During the test, the DUT Y outputs are compared (using XOR gates) to the synchronized model pattern. All difference between the DUT Y outputs and the synchronized model pattern trig an error flag.

The error vector is computed using a time stamp, pattern values, DUT output values, XOR flags and 2 other flags indicating a synchronization trouble and a data loss. The error vector is recorded or not depending on some conditions like:

- Error counts lower than LE (Large Error) threshold.
- Error counts lower than SEFI threshold.

5.4 Power supplies - Test conditions

Two different power supplies conditions were used: one for SEFI, SEU and SET test and one for SEL test. The Table 5 details both test conditions.

Parameters	SEU / SET test condition	SEL test condition
Vcc (V)	3.1	3.5
Icc nom (mA)	190	200
Icc threshold (mA)	400	400
Vio (V)	3.1	3.5
Iio nom (mA)	6	8
Iio threshold (mA)	50	50
Vcp (V)	3.0	3.0
Icp nom (mA)	0.6	1
Icp threshold (mA)	50	50

Table 5 - Power supplies - test conditions

6 Test Results

6.1 SEL

One SEL was recorded on the core supply of the sample SN 5 during the run 71 with a fluence of 1E7 ions.cm² a LET of 120 MeV.cm²/mg (Xenon with 60 ° tilt angle) a core and IO voltage supplies of 3.5 V a charge pump supply of 3.0 V and a temperature of 125 °C.

As detailed on the Table 5 the core current nominal consumption was about 200 mA. A threshold of 400 mA was set to trigger SEL.

The SEL is visible on the Figure 7 showing the full chronogram from the run 71 of the core supply and flux vs. time. Several phenomena can be seen from this figure:

- The SEL occurring at 9507 seconds (abscissa reference) where the core current is measured at 750 mA.
- One long step of high current consumption from 9275 seconds to the SEL where the average core current is measured at 360 mA.
- Several steps with zero current consumption looking like “power down” steps.
- Several lower current consumption steps where the core current is measure around 170 mA.

It has to be remembered than during SEL test the device configuration was added to the test sequence. The “power down” steps and lower current consumption phenomena were corrected by the device re-configuration. On the other way the long step of high current consumption was not corrected by the re-configuration.

No event was recorded on IO and charge pump supplies as it can be seen from Figure 8 and Figure 9.

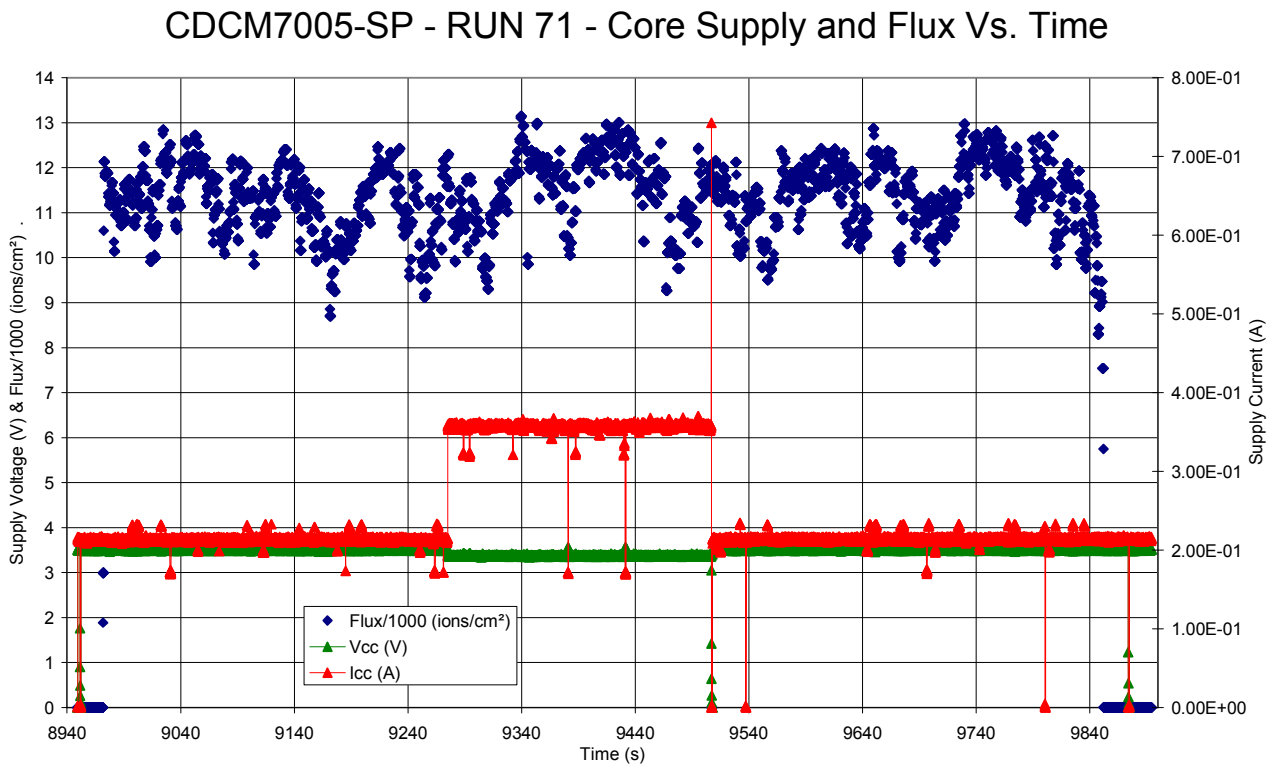

Figure 7 - RUN 71 - Core supply and Flux vs. Time

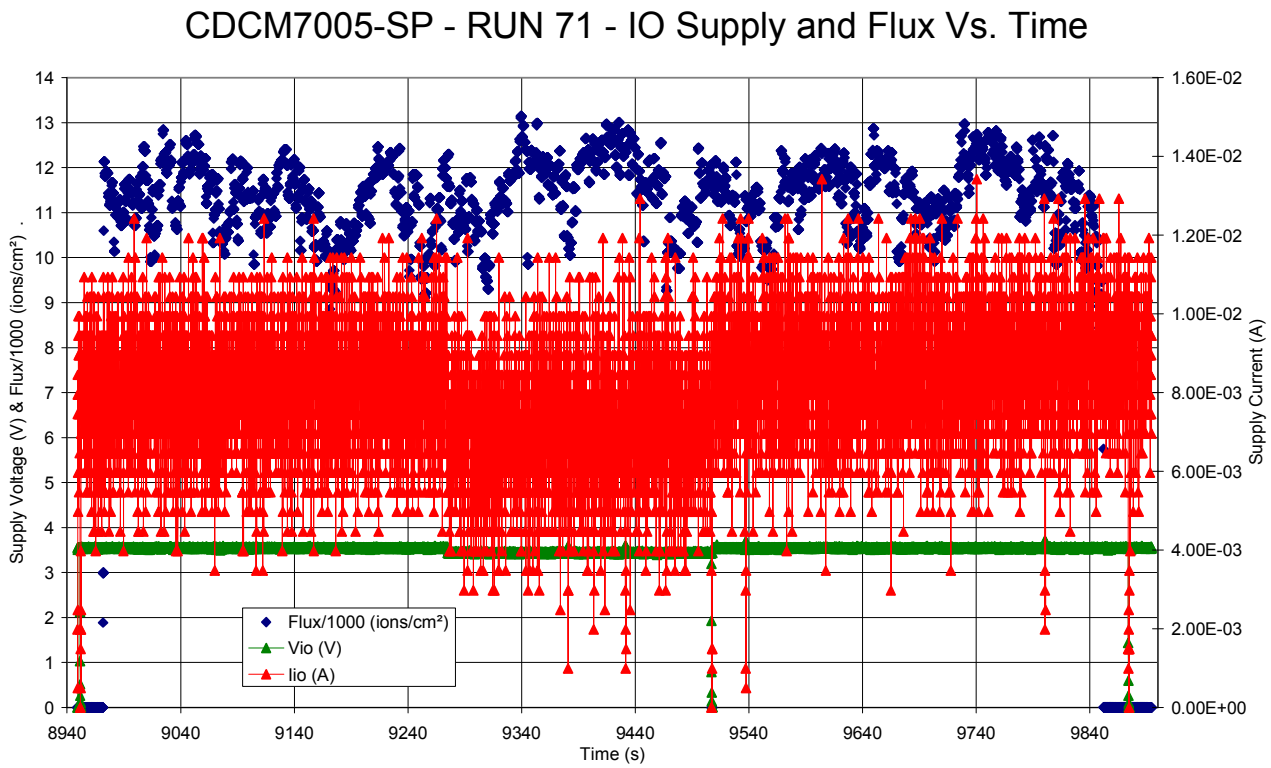

Figure 8 - RUN 71 - IO supply and Flux vs. Time

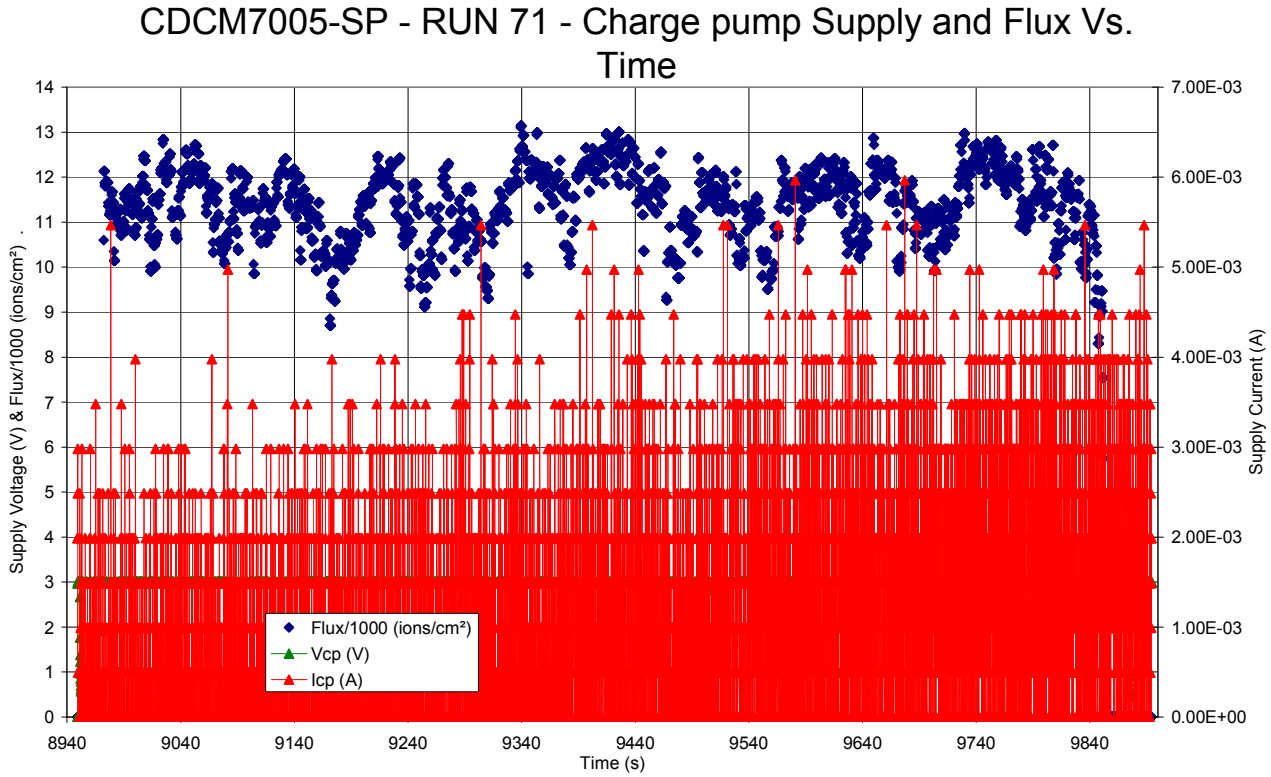

Figure 9 - RUN 71 - Charge pump supply and Flux vs. Time

6.2 SEFI

No SEFI was detected up to a LET of 60 MeV.cm²/mg.

6.3 SEU

SEUs were detected and recorded. During the data analysis process, 5 types of SEUs were defined (see here below) and all SEUs were classified:

Type 1: Out of phase / an event creating a delay between the DUT output and the synchronized model pattern. The DUT output phase did never recover its original state. The only way to recover from the error was to re-synchronize the model pattern. This type of error created a very large amount of recorded events triggering the SEFI flag during the test. However, the device being still functional (PLL locked and generating synchronized clocks) this type of error was classified as SEU of type 1 during the data analysis process.

Type 2: PLL lock / each time an event created the PLL lock signal to clear, for any reason one SEU of type 2 was counted.

Type 3: VCXO status / each time an event created the VCXO status to clear, for any reason one SEU of type 3 was counted.

Type 4: REF status / each time an event created the REF status to clear, for any reason one SEU of type 4 was counted.

Type 5: All other kinds of SEU recorded:
- SEU on a single Y output
- SEU on several Y outputs
- Combination of SEUs

The synchronization flag was never rose meaning the model pattern could always be synchronized properly with the DUT Y outputs. On the other way the data loss flag was recorded rose meaning error vectors were lost before being recorded. This data loss was due to the very large amount of error to be recorded.

The Figure 10 summarizes the SEU cross-sections per device of the 5 types of SEU.

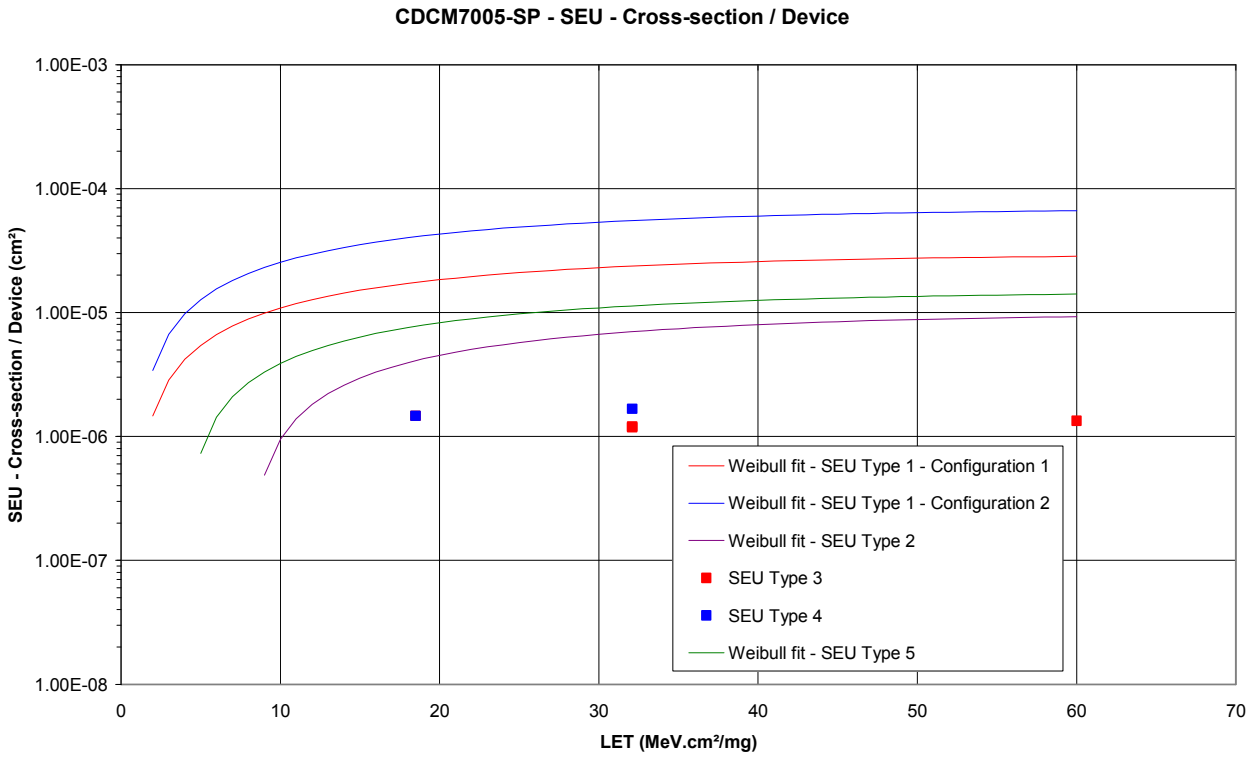

Figure 10 - SEU cross-sections per device

6.3.1 SEU Type 1

The SEU type 1 cross-section per device is plotted on the Figure 11. For the first configuration, the saturation cross-section is about 3E-5 cm² with a LET threshold below 3.6 MeV.cm²/mg. For the second configuration, the saturation cross-section is about 7E-5 cm² with a LET threshold below 3.6 MeV.cm²/mg.

Two Weibull fit curves were estimated from the measured points and added to the graph. The estimated Weibull fit curves are computed from the following equation of the cumulative distribution function:

$$\sigma = CSsat\left(1 - e^{-(x/\lambda)K}\right)$$

The parameters values of the estimated Weibull fit curves of the SEU of type 1 are visible on the Table 6.

Parameters	Configuration 1	Configuration 2
K	1	1
λ	20	20
X_0 (Mev.cm²/mg)	1	1
CSsat (cm²)	3E-5	7E-5

Table 6 - SEU Type 1 - Weibull fit curve parameter values

The phase delay distribution of the SEU of type 1 is plotted on the Figure 12. It can be seen than:
- The majority of out of phase errors present a phase delay of one clock cycle (20 ns).
- All recorded out of phase errors present a phase delay lower than 6 clock cycles (120 ns).

It should be remembered than the DUT Y outputs have a period of 160 ns (frequency of 6.25 MHz).

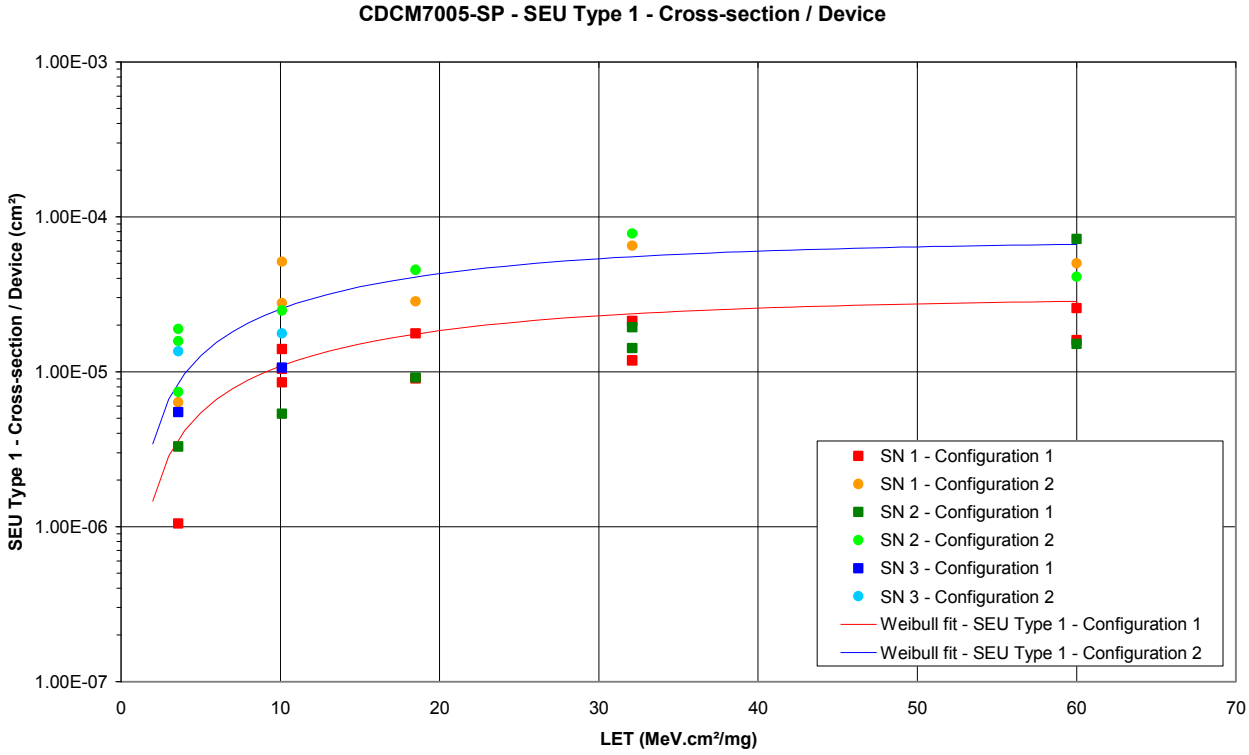

Figure 11 - SEU Type 1 cross-section per device

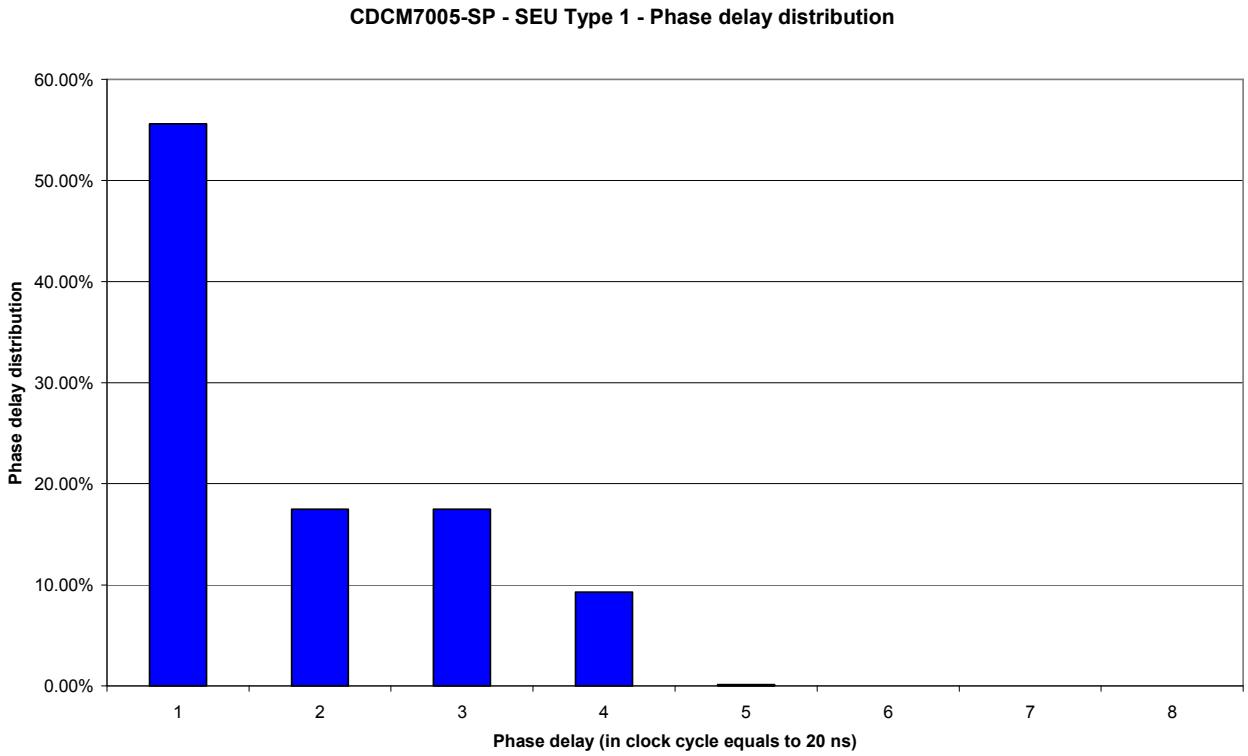

Figure 12 - SEU Type 1 - Phase delay distribution

6.3.2 SEU Type 2

The SEU type 2 cross-section per device is plotted on the Figure 13. The saturation cross-section is about 1E-5 cm² with a LET threshold below 10 MeV.cm²/mg.

An estimated Weibull fit curve having the following parameters is added to the graph:

K = 1
λ = 20
X_0 = 8 MeV.cm²/mg
CSsat = 1E-5 cm²

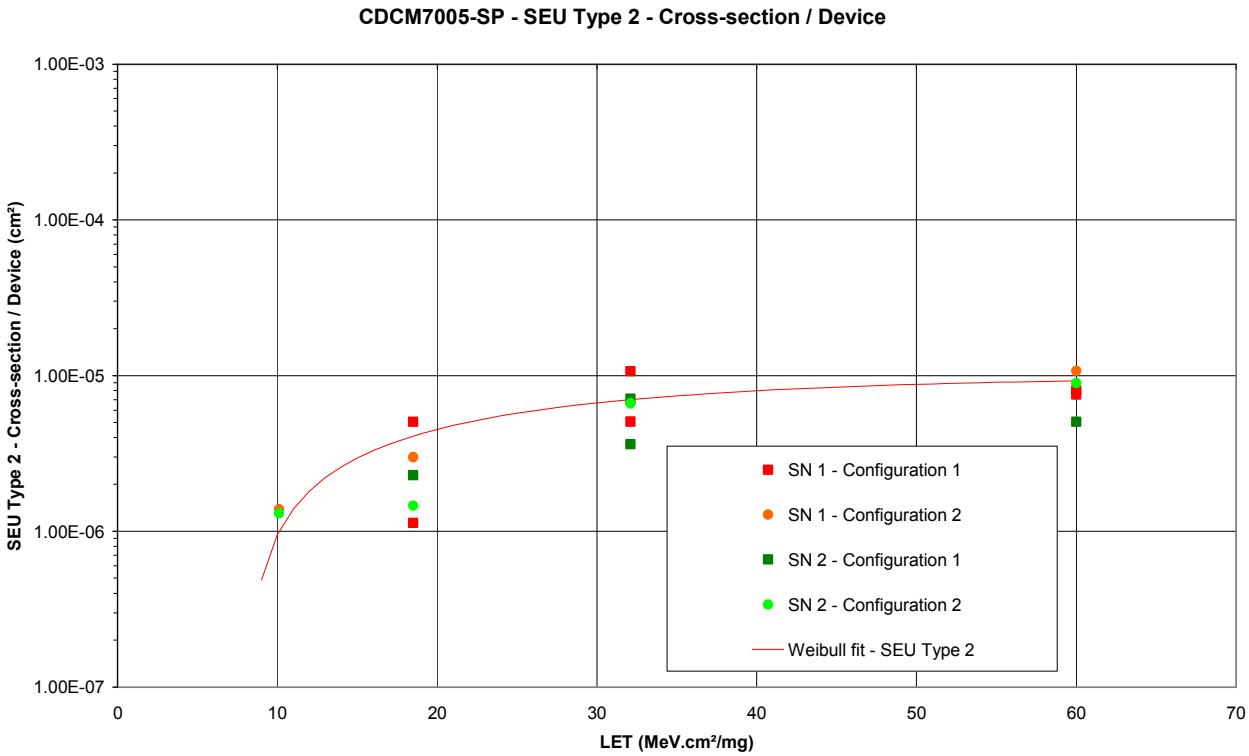

Figure 13 - SEU Type 2 cross-section per device

6.3.3 SEU Type 3

The SEU type 3 cross-section per device is plotted on the Figure 14. The saturation cross-section is about 1.6E-6 cm² with a LET threshold below 18 MeV.cm²/mg.

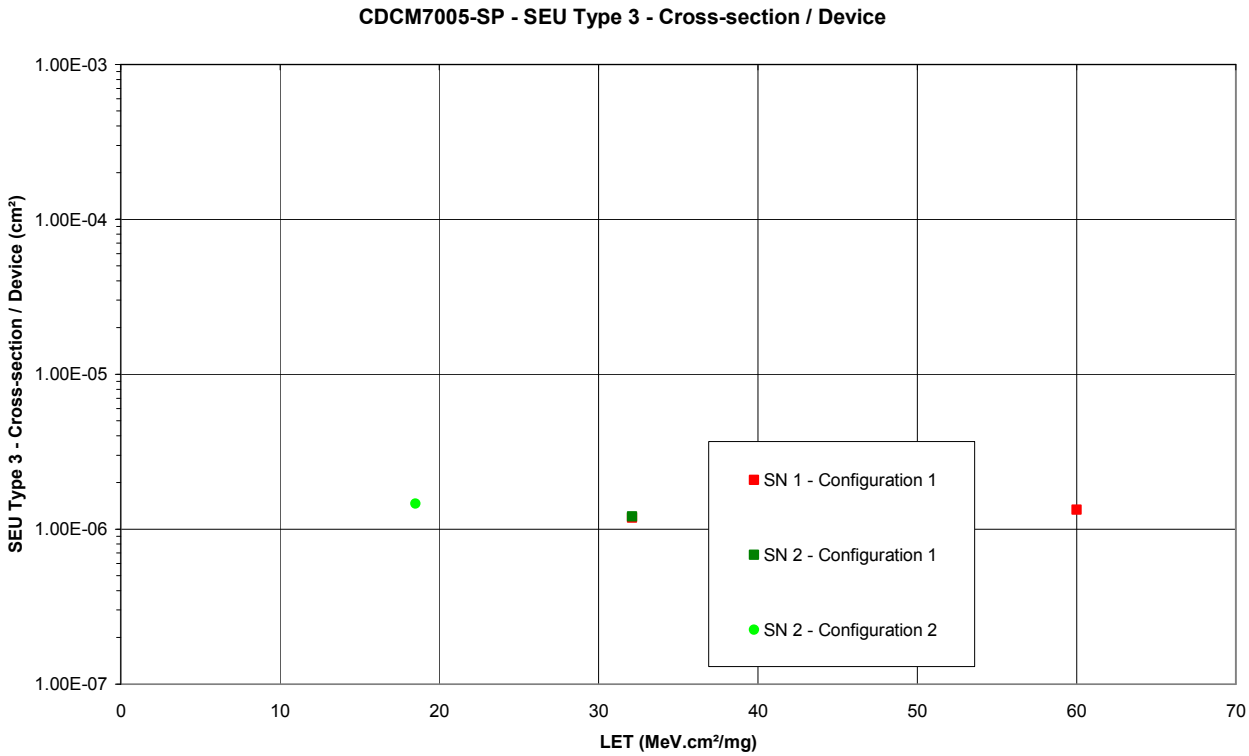

Figure 14 - SEU Type 3 cross-section per device

6.3.4 SEU Type 4

The SEU type 4 cross-section per device is plotted on the Figure 14. The saturation cross-section is about 1.7E-6 cm² with a LET threshold below 18 MeV.cm²/mg.

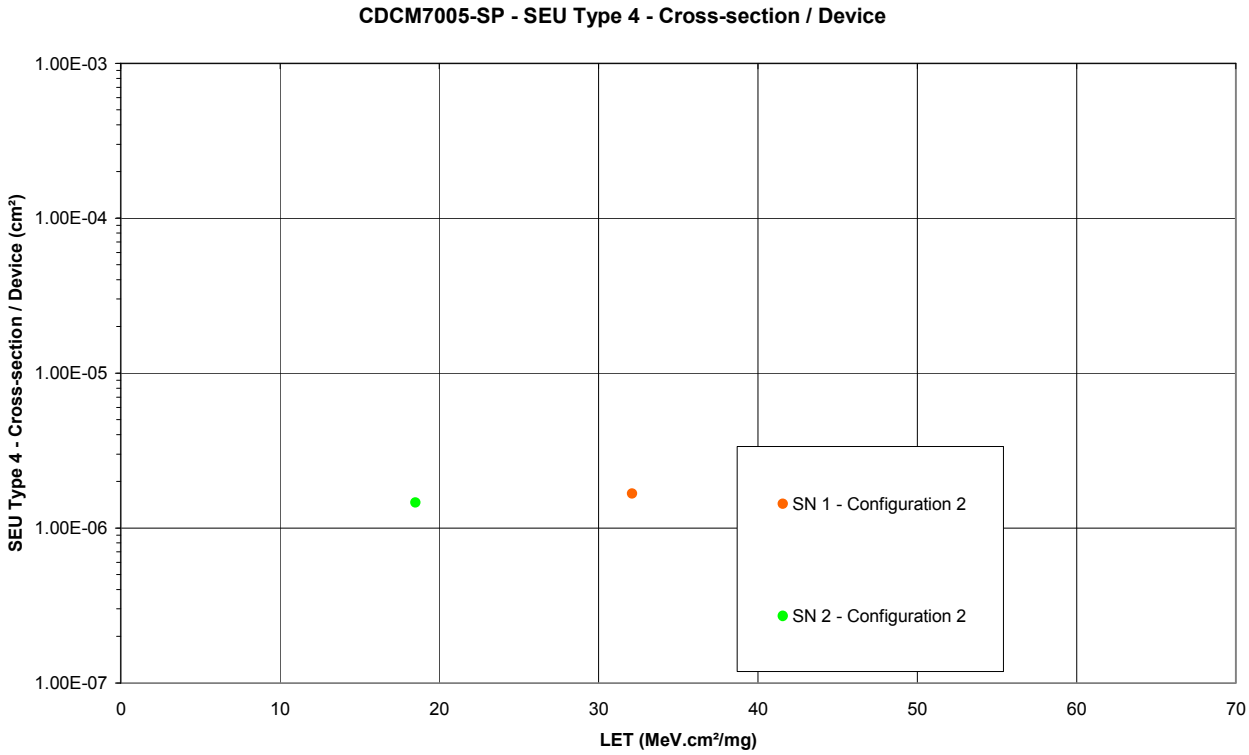

Figure 15 - SEU Type 4 cross-section per device

6.3.5 SEU Type 5

The SEU type 5 cross-section per device is plotted on the Figure 16. The saturation cross-section is about 1.5E-5 cm² with a LET threshold below 5 MeV.cm²/mg. An estimated Weibull fit curve having the following parameters is added to the graph:

K = 1
λ = 20
X_0 = 4 MeV.cm²/mg
CSsat = 1.5E-5 cm²

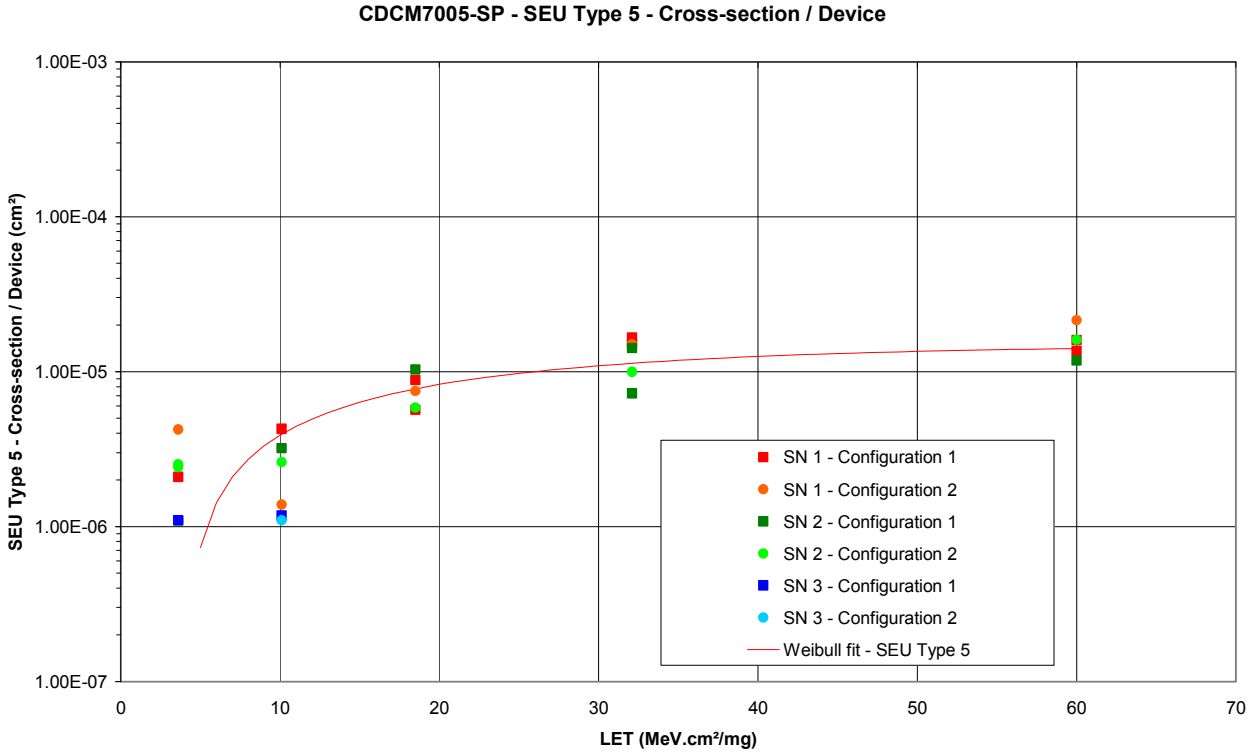

Figure 16 - SEU Type 5 cross-section per device

6.4 SET

SETs here reported are SETs that cannot be linked to any other event (SEL, SEFI, and SEU). All SETs that were the consequence of SEL or SEFI or SEU where removed from the SET log during the data analysis process.

6.4.1 SET on Vbb

The SET cross-section per device of the Vbb bias voltage output is plotted on the Figure 18. The Vbb SET saturation cross-section is about 3E-5 cm² with a LET threshold around 10 MeV.cm²/mg. Two examples of SET chronograms from the RUN056 are plotted on the Figure 17.

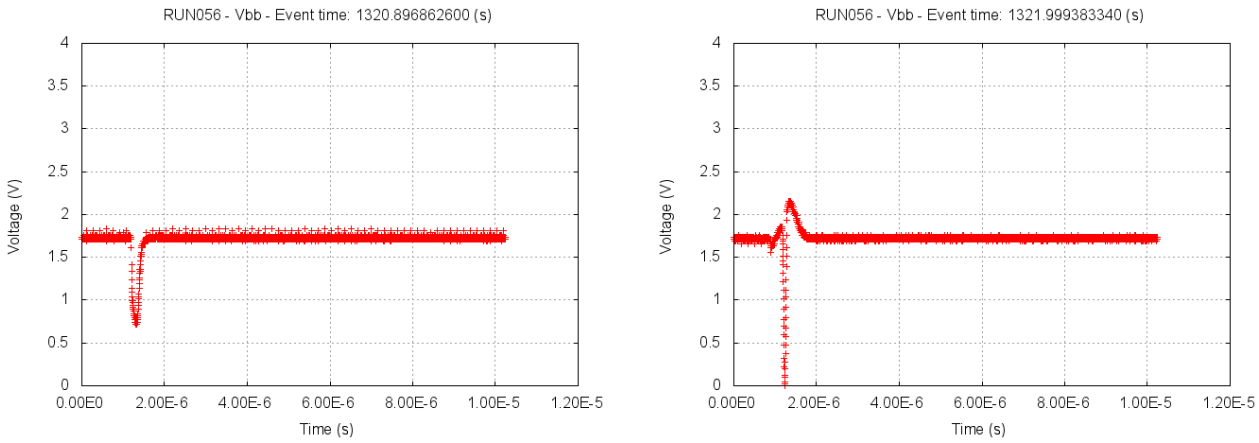

Figure 17 - Vbb - SET Chronogram examples from RUN056

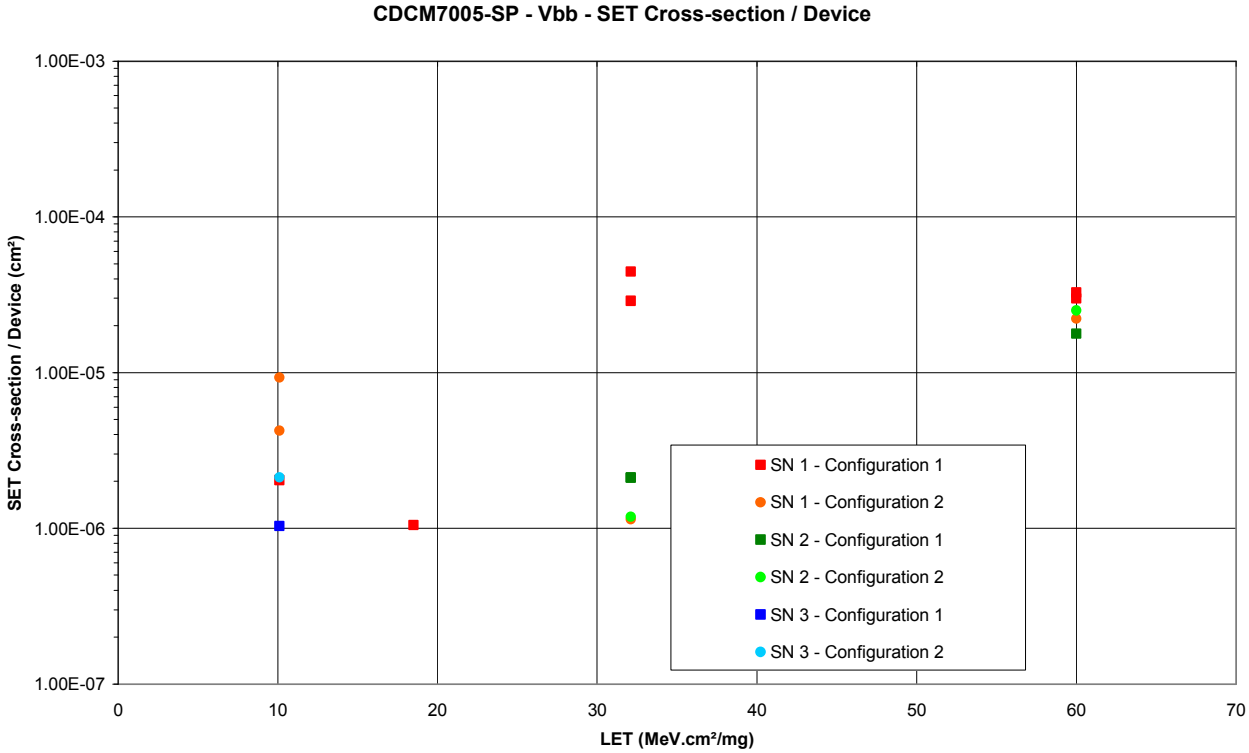

Figure 18 - Vbb - SET cross-section per device

6.4.2 SET on Vcp

Due to bad functionality of the channel of the digitizer, the result of the Vcp channel (charge pump output) cannot be reliably presented or counted.

6.4.3 SET on Y0

No SET were recorded on the Y0 channel (DUT output 0 configured to be LVPECL) up to a LET of 60 MEV.cm²/mg.

6.4.4 SET on Y2B

The Y2B channel (DUT output 2 configured to be LVCMOS) was noisy and many events due large noise spikes were detected without beam. The SET log presents a very large amount of data due to those noise spikes and small SET (if exist) cannot be separated. However this channel can be supposed to be similar to the Y0 channel.

7 Conclusion

This report presents the results of heavy ion irradiation characterization carried out on the CDCM7005-SP. This device is a 3.3V high performance Rad tolerant class V, clock synchronizer and itter cleaner from Texas Instruments.

6 samples were tested at RADEF, University of Jyväskylä, Jyväskylä , Finland on November 2011 under HIREX Engineering responsibility.

One SEL event was recorded on the core supply of the sample SN 5 during the run 71 with a fluence of 1E7 ions.cm² a LET of 120 MeV.cm²/mg (Xenon with 60 ° tilt angle) a core and IO voltage supplies of 3.5 V a charge pump supply of 3.0 V and a temperature of 125 °C.

No SEFI was detected up to a LET of 60 MeV.cm²/mg.

SEUs were detected and recorded during the test. During the data analysis process 5 types of SEUs were defined and SEUs were classified.

SEU of type 1: For the first configuration the saturation cross-section is about 3E-5 cm² with a LET threshold below 3.6 MeV.cm²/mg. For the second configuration, the saturation cross-section is about 7E-5 cm² with a LET threshold below 3.6 MeV.cm²/mg.

SEU of type 2: The saturation cross-section is about 1E-5 cm² with a LET threshold below 10 MeV.cm²/mg.

SEU of type 3: The saturation cross-section is about 1.6E-6 cm² with a LET threshold below 18 MeV.cm²/mg.

SEU of type 4: The saturation cross-section is about 1.7E-6 cm² with a LET threshold below 18 MeV.cm²/mg.

SEU of type 5: The saturation cross-section is about 1.5E-5 cm² with a LET threshold below 5 MeV.cm²/mg.

SET were detected and recorded on Vbb channel (bias voltage output). The Vbb SET saturation cross-section is about 3E-5 cm² and the LET threshold around 10 MeV.cm²/mg. The sensitivity of Vcp channel (charge pump output) to SET could not be reliably estimated due to a bad functionality of the channel of the digitizer. No SET was detected on Y0 channel (DUT output 0 configured to be LVPECL). Y2B channel (DUT output 2 configured to be LVCMOS) is supposed to be equivalent to Y0 channel because large noise spikes prevent the detection of eventual SET.

8 Glossary

Most of the definitions here below are from JEDEC standard JESD89A

DUT: Device under test.

Fluence (of particle radiation incident on a surface): The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface.
In this document, Fluence is expressed in ions per cm2.

Flux: The time rate of flow of particle radiant energy incident on a surface, divided by the area of that surface.
In this document, Flux is expressed in ions per cm2*s.

Single-Event Effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike.
Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL.

Single-Event Transient (SET): A soft error caused by the transient signal induced by a single energetic particle strike.

Single-Event Latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.
Single-Event Latch-up (SEL) cross-section: the number of events per unit fluence. For chip SEL cross-section, the dimensions are cm2 per chip.

Error cross-section: the number of errors per unit fluence. For device error cross-section, the dimensions are cm2 per device. For bit error cross-section, the dimensions are cm2 per bit.

Tilt angle: tilt angle, rotation axis of the DUT board is perpendicular to the beam axis; roll angle, board rotation axis is parallel to the beam axis

9 Run tables

9.1 Beam conditions, DUT conditions and SEL results

RUN					BEAM												DUT						SEL		
Line	Date	Hirex run #	Facility run #	Start time	Ion specie	Energy (MeV)	Range (Si) (µm)	LET (MeV.cm²/mg)	Tilt (°)	Roll (°)	LETeff. (MeV.cm²/mg)	Fluence (p/cm²)	Run duration (s)	Mean flux (p/(cm².s))	Run dose (Rad)	SN	Total dose (Rad)	Temperature (°)	Vcc, Vio (V)	Vcp (V)	Configuration	Count	Fluence (p/cm²)	Cross-section/device (cm²)
3	11/07/2011	3	1	12:13	40Ar+12	372	118	10.1	0	0	10.1	3.41E+05	6.82E+01	5.00E+03	5.51E+01	1	5.51E+01	Room	3.1	3	1	0	9.36E+05	-
4	11/07/2011	4	2	12:20	40Ar+12	372	118	10.1	0	0	10.1	1.00E+06	2.00E+02	5.00E+03	1.62E+02	1	2.17E+02	Room	3.1	3	1	0	8.59E+05	-
6	11/07/2011	6	3	12:31	40Ar+12	372	118	10.1	0	0	10.1	1.00E+06	2.00E+02	5.00E+03	1.62E+02	1	3.78E+02	Room	3.1	3	2	0	7.80E+04	-
9	11/07/2011	9	4	12:57	40Ar+12	372	118	10.1	0	0	10.1	1.00E+06	2.00E+02	5.00E+03	1.62E+02	1	5.40E+02	Room	3.1	3	2	0	7.21E+05	-
10	11/07/2011	10	5	13:02	40Ar+12	372	118	10.1	0	0	10.1	1.00E+06	2.00E+02	5.00E+03	1.62E+02	1	7.02E+02	Room	3.1	3	1	0	8.65E+05	-
13	11/07/2011	13	6	13:24	40Ar+12	372	118	10.1	0	0	10.1	1.00E+06	2.00E+02	5.00E+03	1.62E+02	2	1.62E+02	Room	3.1	3	1	0	9.36E+05	-
14	11/07/2011	14	7	13:30	40Ar+12	372	118	10.1	0	0	10.1	1.00E+06	2.00E+02	5.00E+03	1.62E+02	2	3.23E+02	Room	3.1	3	2	0	7.66E+05	-
17	11/07/2011	17	8	13:50	40Ar+12	372	118	10.1	0	0	10.1	1.00E+06	2.00E+02	5.00E+03	1.62E+02	3	1.62E+02	Room	3.1	3	2	0	7.92E+05	-
18	11/07/2011	18	9	13:56	40Ar+12	372	118	10.1	0	0	10.1	1.00E+06	2.00E+02	5.00E+03	1.62E+02	3	3.23E+02	Room	3.1	3	1	0	8.48E+05	-
19	11/07/2011	19	10	14:37	20Ne+6	186	146	3.6	0	0	3.6	1.00E+06	2.00E+02	5.00E+03	5.76E+01	3	3.81E+02	Room	3.1	3	1	0	9.12E+05	-
20	11/07/2011	20	11	14:42	20Ne+6	186	146	3.6	0	0	3.6	1.00E+06	2.00E+02	5.00E+03	5.76E+01	3	4.38E+02	Room	3.1	3	2	0	8.12E+05	-
24	11/07/2011	24	12	15:06	20Ne+6	186	146	3.6	0	0	3.6	1.00E+06	2.00E+02	5.00E+03	5.76E+01	2	3.81E+02	Room	3.1	3	2	0	7.94E+05	-
25	11/07/2011	25	13	15:12	20Ne+6	186	146	3.6	0	0	3.6	9.02E+05	1.80E+02	5.00E+03	5.20E+01	2	4.33E+02	Room	3.1	3	2	0	2.70E+05	-
26	11/07/2011	26	14	15:17	20Ne+6	186	146	3.6	0	0	3.6	1.00E+06	2.00E+02	5.00E+03	5.76E+01	2	4.90E+02	Room	3.1	3	2	0	8.25E+05	-
27	11/07/2011	27	15	15:21	20Ne+6	186	146	3.6	0	0	3.6	1.00E+06	2.00E+02	5.00E+03	5.76E+01	2	5.48E+02	Room	3.1	3	1	0	9.13E+05	-
29	11/07/2011	29	16	15:37	20Ne+6	186	146	3.6	0	0	3.6	1.00E+06	2.00E+02	5.00E+03	5.76E+01	1	7.59E+02	Room	3.1	3	2	0	9.44E+05	-
30	11/07/2011	30	17	15:42	20Ne+6	186	146	3.6	0	0	3.6	1.00E+06	2.00E+02	5.00E+03	5.76E+01	1	8.17E+02	Room	3.1	3	1	0	9.55E+05	-
31	11/07/2011	31	18	17:01	56Fe+15	523	97	18.5	0	0	18.5	1.00E+06	2.00E+02	5.00E+03	2.96E+02	1	1.11E+03	Room	3.1	3	1	0	8.84E+05	-
32	11/07/2011	32	19	17:05	56Fe+15	523	97	18.5	0	0	18.5	1.00E+06	2.00E+02	5.00E+03	2.96E+02	1	1.41E+03	Room	3.1	3	1	0	7.91E+05	-
33	11/07/2011	33	20	17:11	56Fe+15	523	97	18.5	0	0	18.5	1.00E+06	2.00E+02	5.00E+03	2.96E+02	1	1.70E+03	Room	3.1	3	2	0	6.67E+05	-
35	11/07/2011	35	21	17:30	56Fe+15	523	97	18.5	0	0	18.5	1.00E+06	2.00E+02	5.00E+03	2.96E+02	2	8.44E+02	Room	3.1	3	2	0	6.83E+05	-
36	11/07/2011	36	22	17:34	56Fe+15	523	97	18.5	0	0	18.5	1.00E+06	2.00E+02	5.00E+03	2.96E+02	2	1.14E+03	Room	3.1	3	1	0	8.73E+05	-
38	11/07/2011	38	23	18:05	82Kr+22	768	94	32.1	0	0	32.1	1.00E+06	2.00E+02	5.00E+03	5.14E+02	2	1.65E+03	Room	3.1	3	1	0	8.45E+05	-
39	11/07/2011	39	24	18:12	82Kr+22	768	94	32.1	0	0	32.1	1.00E+06	2.00E+02	5.00E+03	5.14E+02	2	2.17E+03	Room	3.1	3	1	0	8.28E+05	-
40	11/07/2011	40	25	18:18	82Kr+22	768	94	32.1	0	0	32.1	1.00E+06	2.00E+02	5.00E+03	5.14E+02	2	2.68E+03	Room	3.1	3	2	0	6.02E+05	-
45	11/07/2011	45	26	18:49	82Kr+22	768	94	32.1	0	0	32.1	1.00E+06	2.00E+02	5.00E+03	5.14E+02	1	2.22E+03	Room	3.1	3	2	0	5.99E+05	-
46	11/07/2011	46	27	18:57	82Kr+22	768	94	32.1	0	0	32.1	1.00E+06	2.00E+02	5.00E+03	5.14E+02	1	2.73E+03	Room	3.1	3	1	0	5.92E+05	-
47	11/07/2011	47	28	19:05	82Kr+22	768	94	32.1	0	0	32.1	1.00E+06	2.00E+02	5.00E+03	5.14E+02	1	3.25E+03	Room	3.1	3	1	0	8.44E+05	-
50	11/07/2011	50	29	19:33	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	1	4.21E+03	Room	3.1	3	1	0	6.61E+05	-
51	11/07/2011	51	30	19:36	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	1	5.17E+03	Room	3.1	3	1	0	7.49E+05	-
52	11/07/2011	52	31	19:41	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	1	6.13E+03	Room	3.1	3	2	0	5.59E+05	-
54	11/07/2011	54	32	20:01	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	2	3.64E+03	Room	3.1	3	2	0	5.60E+05	-
55	11/07/2011	55	33	20:06	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	2	4.60E+03	Room	3.1	3	1	0	2.78E+04	-
56	11/07/2011	56	34	20:09	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	2	5.56E+03	Room	3.1	3	1	0	5.95E+05	-
59	11/07/2011	59	35	20:43	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	3	1.40E+03	80	3.1	3	1	0	8.81E+05	-
60	11/07/2011	60	36	20:46	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	3	2.36E+03	80	3.1	3	2	0	8.69E+05	-
61	11/07/2011	61	37	20:57	131Xe+35	1217	89	60	0	0	60	1.00E+07	5.00E+02	2.00E+04	9.60E+03	3	1.20E+04	125	3.1	3	2	0	8.38E+06	-
62	11/07/2011	62	38	21:25	131Xe+35	1217	89	60	0	0	60	1.00E+07	5.00E+02	2.00E+04	9.60E+03	3	2.16E+04	125	3.1	3	1	0	8.26E+06	-
65	11/07/2011	65	39	21:59	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	4	9.60E+02	80	3.5	3	2	0	8.23E+05	-
66	11/07/2011	66	40	22:04	131Xe+35	1217	89	60	0	0	60	1.00E+06	2.00E+02	5.00E+03	9.60E+02	4	1.92E+03	80	3.5	3	1	0	8.61E+05	-
68	11/07/2011	68	41	22:12	131Xe+35	1217	89	60	0	0	60	1.00E+07	5.00E+02	2.00E+04	9.60E+03	4	1.15E+04	125	3.5	3	1	0	8.26E+06	-
69	11/07/2011	69	42	22:30	131Xe+35	1217	89	60	0	0	60	1.00E+07	5.00E+02	2.00E+04	9.60E+03	4	2.11E+04	125	3.5	3	2	0	8.25E+06	-
71	11/07/2011	71	43	22:56	131Xe+35	1217	89	60	60	0	120	1.00E+07	5.00E+02	2.00E+04	1.92E+04	5	1.92E+04	125	3.5	3	1	1	8.20E+06	1.22E-07
73	11/07/2011	73	44	23:30	131Xe+35	1217	89	60	60	0	120	1.00E+07	5.00E+02	2.00E+04	1.92E+04	6	1.92E+04	125	3.5	3	1	0	8.30E+06	-

9.2 SEU Type 1 results

RUN						SEU Type 1 (Delayed output)			SEU Type 1 - Delay values (clock cycle - 20 ns)								
Line	Date	Hirex run #	Facility run #	Start time	Synchronization Error	Count	Fluence (p/cm²)	Cross-section/device (cm²)	0	1	2	3	4	5	6	7	8
3	11/07/2011	3	1	12:13	No	8	9.36E+05	8.55E-06	0	4	0	3	4	0	0	0	0
4	11/07/2011	4	2	12:20	No	12	8.59E+05	1.40E-05	0	9	0	4	3	0	0	0	0
6	11/07/2011	6	3	12:31	No	4	7.80E+04	5.13E-05	0	9	6	1	1	0	0	0	0
9	11/07/2011	9	4	12:57	No	20	7.21E+05	2.77E-05	0	15	6	5	5	0	0	0	0
10	11/07/2011	10	5	13:02	No	9	8.65E+05	1.04E-05	0	7	2	1	2	0	0	0	0
13	11/07/2011	13	6	13:24	No	5	9.36E+05	5.34E-06	0	3	0	1	2	0	0	0	0
14	11/07/2011	14	7	13:30	No	19	7.66E+05	2.48E-05	0	24	8	8	3	0	0	0	0
17	11/07/2011	17	8	13:50	No	14	7.92E+05	1.77E-05	0	14	7	2	3	0	0	0	0
18	11/07/2011	18	9	13:56	No	9	8.48E+05	1.06E-05	0	7	3	1	2	0	0	0	0
19	11/07/2011	19	10	14:37	No	5	9.12E+05	5.48E-06	0	4	1	0	1	0	0	0	0
20	11/07/2011	20	11	14:42	No	11	8.12E+05	1.36E-05	0	8	4	1	7	0	0	0	0
24	11/07/2011	24	12	15:06	No	15	7.94E+05	1.89E-05	0	17	7	7	4	0	0	0	0
25	11/07/2011	25	13	15:12	No	2	2.70E+05	7.41E-06	0	2	0	1	1	0	0	0	0
26	11/07/2011	26	14	15:17	No	13	8.25E+05	1.58E-05	0	12	3	6	2	0	0	0	0
27	11/07/2011	27	15	15:21	No	3	9.13E+05	3.29E-06	0	2	0	0	1	0	0	0	0
29	11/07/2011	29	16	15:37	No	6	9.44E+05	6.35E-06	0	7	0	3	0	0	0	0	0
30	11/07/2011	30	17	15:42	No	1	9.55E+05	1.05E-06	0	0	0	0	1	0	0	0	0
31	11/07/2011	31	18	17:01	No	8	8.84E+05	9.05E-06	0	7	1	2	1	0	0	0	0
32	11/07/2011	32	19	17:05	No	14	7.91E+05	1.77E-05	0	13	3	3	2	0	0	0	0
33	11/07/2011	33	20	17:11	No	19	6.67E+05	2.85E-05	0	17	8	7	2	0	0	0	0
35	11/07/2011	35	21	17:30	No	31	6.83E+05	4.54E-05	0	26	9	7	5	0	0	0	0
36	11/07/2011	36	22	17:34	No	8	8.73E+05	9.16E-06	0	7	2	2	1	0	0	0	0
38	11/07/2011	38	23	18:05	No	12	8.45E+05	1.42E-05	0	11	4	4	3	0	0	0	0
39	11/07/2011	39	24	18:12	No	16	8.28E+05	1.93E-05	0	15	3	5	1	0	0	0	0
40	11/07/2011	40	25	18:18	No	47	6.02E+05	7.81E-05	0	46	18	15	3	0	0	0	0
45	11/07/2011	45	26	18:49	No	39	5.99E+05	6.51E-05	0	38	15	15	5	0	0	0	0
46	11/07/2011	46	27	18:57	No	7	5.92E+05	1.18E-05	0	7	0	2	1	0	0	0	0
47	11/07/2011	47	28	19:05	No	18	8.44E+05	2.13E-05	0	17	3	4	3	0	0	0	0
50	11/07/2011	50	29	19:33	No	17	6.61E+05	2.57E-05	0	17	2	2	0	0	0	0	0
51	11/07/2011	51	30	19:36	No	12	7.49E+05	1.60E-05	0	11	1	3	1	0	0	0	0
52	11/07/2011	52	31	19:41	No	28	5.59E+05	5.01E-05	0	27	5	12	2	0	0	0	0
54	11/07/2011	54	32	20:01	No	23	5.60E+05	4.11E-05	0	22	8	6	1	1	0	0	0
55	11/07/2011	55	33	20:06	No	2	2.78E+04	7.20E-05	0	3	1	0	0	0	0	0	0
56	11/07/2011	56	34	20:09	No	9	5.95E+05	1.51E-05	0	9	4	3	0	0	0	0	0
59	11/07/2011	59	35	20:43	No	99	-	-	-	-	-	-	-	-	-	-	-
60	11/07/2011	60	36	20:46	No	124	-	-	-	-	-	-	-	-	-	-	-
61	11/07/2011	61	37	20:57	No	979	-	-	-	-	-	-	-	-	-	-	-
62	11/07/2011	62	38	21:25	No	443	-	-	-	-	-	-	-	-	-	-	-
65	11/07/2011	65	39	21:59	No	143	-	-	-	-	-	-	-	-	-	-	-
66	11/07/2011	66	40	22:04	No	128	-	-	-	-	-	-	-	-	-	-	-
68	11/07/2011	68	41	22:12	No	629	-	-	-	-	-	-	-	-	-	-	-
69	11/07/2011	69	42	22:30	No	384	-	-	-	-	-	-	-	-	-	-	-
71	11/07/2011	71	43	22:56	No	626	-	-	-	-	-	-	-	-	-	-	-
73	11/07/2011	73	44	23:30	No	536	-	-	-	-	-	-	-	-	-	-	-

9.3 SEU Type 2, 3, 4 and 5 results

RUN					SEU Type 2 (PLL Lock Status)			SEU Type 3 (VCXO Status)			SEU Type 4 (REF Status)			SEU Type 5 (Other kind)		
Line	Date	Hirex run #	Facility run #	Start time	Count	Fluence (p/cm²)	Cross-section/device (cm²)	Count	Fluence (p/cm²)	Cross-section/device (cm²)	Count	Fluence (p/cm²)	Cross-section/device (cm²)	SEU	SEU Fluence (p/cm²)	SEU Cross-section (cm²)
3	11/07/2011	3	1	12:13	0	9.36E+05	-	0	9.36E+05	-	0	9.36E+05	-	4	9.36E+05	4.27E-06
4	11/07/2011	4	2	12:20	0	8.59E+05	-	0	8.59E+05	-	0	8.59E+05	-	0	8.59E+05	-
6	11/07/2011	6	3	12:31	0	7.80E+04	-	0	7.80E+04	-	0	7.80E+04	-	0	7.80E+04	-
9	11/07/2011	9	4	12:57	1	7.21E+05	1.39E-06	0	7.21E+05	-	0	7.21E+05	-	1	7.21E+05	1.39E-06
10	11/07/2011	10	5	13:02	0	8.65E+05	-	0	8.65E+05	-	0	8.65E+05	-	0	8.65E+05	-
13	11/07/2011	13	6	13:24	0	9.36E+05	-	0	9.36E+05	-	0	9.36E+05	-	3	9.36E+05	3.20E-06
14	11/07/2011	14	7	13:30	1	7.66E+05	1.31E-06	0	7.66E+05	-	0	7.66E+05	-	2	7.66E+05	2.61E-06
17	11/07/2011	17	8	13:50	0	7.92E+05	-	0	7.92E+05	-	0	7.92E+05	-	1	7.92E+05	1.26E-06
18	11/07/2011	18	9	13:56	0	8.48E+05	-	0	8.48E+05	-	0	8.48E+05	-	1	8.48E+05	1.18E-06
19	11/07/2011	19	10	14:37	0	9.12E+05	-	0	9.12E+05	-	0	9.12E+05	-	1	9.12E+05	1.10E-06
20	11/07/2011	20	11	14:42	0	8.12E+05	-	0	8.12E+05	-	0	8.12E+05	-	0	8.12E+05	-
24	11/07/2011	24	12	15:06	0	7.94E+05	-	0	7.94E+05	-	0	7.94E+05	-	2	7.94E+05	2.52E-06
25	11/07/2011	25	13	15:12	0	2.70E+05	-	0	2.70E+05	-	0	2.70E+05	-	0	2.70E+05	-
26	11/07/2011	26	14	15:17	0	8.25E+05	-	0	8.25E+05	-	0	8.25E+05	-	2	8.25E+05	2.43E-06
27	11/07/2011	27	15	15:21	0	9.13E+05	-	0	9.13E+05	-	0	9.13E+05	-	1	9.13E+05	1.10E-06
29	11/07/2011	29	16	15:37	0	9.44E+05	-	0	9.44E+05	-	0	9.44E+05	-	4	9.44E+05	4.24E-06
30	11/07/2011	30	17	15:42	0	9.55E+05	-	0	9.55E+05	-	0	9.55E+05	-	2	9.55E+05	2.09E-06
31	11/07/2011	31	18	17:01	1	8.84E+05	1.13E-06	0	8.84E+05	-	0	8.84E+05	-	5	8.84E+05	5.66E-06
32	11/07/2011	32	19	17:05	4	7.91E+05	5.05E-06	0	7.91E+05	-	0	7.91E+05	-	7	7.91E+05	8.84E-06
33	11/07/2011	33	20	17:11	2	6.67E+05	3.00E-06	0	6.67E+05	-	0	6.67E+05	-	5	6.67E+05	7.49E-06
35	11/07/2011	35	21	17:30	1	6.83E+05	1.46E-06	1	6.83E+05	1.46E-06	1	6.83E+05	1.46E-06	4	6.83E+05	5.86E-06
36	11/07/2011	36	22	17:34	2	8.73E+05	2.29E-06	0	8.73E+05	-	0	8.73E+05	-	9	8.73E+05	1.03E-05
38	11/07/2011	38	23	18:05	6	8.45E+05	7.10E-06	0	8.45E+05	-	0	8.45E+05	-	12	8.45E+05	1.42E-05
39	11/07/2011	39	24	18:12	3	8.28E+05	3.62E-06	1	8.28E+05	1.21E-06	0	8.28E+05	-	6	8.28E+05	7.25E-06
40	11/07/2011	40	25	18:18	4	6.02E+05	6.64E-06	0	6.02E+05	-	0	6.02E+05	-	6	6.02E+05	9.96E-06
45	11/07/2011	45	26	18:49	4	5.99E+05	6.68E-06	0	5.99E+05	-	1	5.99E+05	1.67E-06	9	5.99E+05	1.50E-05
46	11/07/2011	46	27	18:57	3	5.92E+05	5.07E-06	0	5.92E+05	-	0	5.92E+05	-	9	5.92E+05	1.52E-05
47	11/07/2011	47	28	19:05	9	8.44E+05	1.07E-05	1	8.44E+05	1.18E-06	0	8.44E+05	-	14	8.44E+05	1.66E-05
50	11/07/2011	50	29	19:33	5	6.61E+05	7.57E-06	0	6.61E+05	-	0	6.61E+05	-	9	6.61E+05	1.36E-05
51	11/07/2011	51	30	19:36	6	7.49E+05	8.01E-06	1	7.49E+05	1.34E-06	0	7.49E+05	-	12	7.49E+05	1.60E-05
52	11/07/2011	52	31	19:41	6	5.59E+05	1.07E-05	0	5.59E+05	-	0	5.59E+05	-	12	5.59E+05	2.15E-05
54	11/07/2011	54	32	20:01	5	5.60E+05	8.93E-06	0	5.60E+05	-	0	5.60E+05	-	9	5.60E+05	1.61E-05
55	11/07/2011	55	33	20:06	1	2.78E+04	3.60E-05	0	2.78E+04	-	0	2.78E+04	-	2	2.78E+04	7.20E-05
56	11/07/2011	56	34	20:09	3	5.95E+05	5.05E-06	0	5.95E+05	-	0	5.95E+05	-	7	5.95E+05	1.18E-05
59	11/07/2011	59	35	20:43	94	-	-	0	-	-	0	-	-	94	-	-
60	11/07/2011	60	36	20:46	116	-	-	0	-	-	0	-	-	116	-	-
61	11/07/2011	61	37	20:57	99	-	-	3	-	-	3	-	-	107	-	-
62	11/07/2011	62	38	21:25	6	-	-	0	-	-	0	-	-	17	-	-
65	11/07/2011	65	39	21:59	8	-	-	1	-	-	0	-	-	9	-	-
66	11/07/2011	66	40	22:04	0	-	-	0	-	-	0	-	-	2	-	-
68	11/07/2011	68	41	22:12	6	-	-	0	-	-	0	-	-	22	-	-
69	11/07/2011	69	42	22:30	52	-	-	1	-	-	0	-	-	58	-	-
71	11/07/2011	71	43	22:56	10	-	-	3	-	-	3	-	-	191	-	-
73	11/07/2011	73	44	23:30	26	-	-	9	-	-	10	-	-	50	-	-

9.4 SET results

RUN					Vbb			Vcp			Y0			Y2B		
Line	Date	Hirex run #	Facility run #	Start time	SET	SET Fluence (p/cm²)	SET Cross-section (cm²)	SET	SET Fluence (p/cm²)	SET Cross-section (cm²)	SET	SET Fluence (p/cm²)	SET Cross-section (cm²)	SET	SET Fluence (p/cm²)	SET Cross-section (cm²)
3	11/07/2011	3	1	12:13	0	9.77E+05	-		9.77E+05	-	0	9.77E+05	-		9.77E+05	-
4	11/07/2011	4	2	12:20	0	9.58E+05	-		9.58E+05	-	0	9.58E+05	-		9.58E+05	-
6	11/07/2011	6	3	12:31	3	3.22E+05	9.31E-06		3.22E+05	-	0	3.22E+05	-		3.22E+05	-
9	11/07/2011	9	4	12:57	4	9.44E+05	4.24E-06		9.44E+05	-	0	9.44E+05	-		9.44E+05	-
10	11/07/2011	10	5	13:02	2	9.79E+05	2.04E-06		9.79E+05	-	0	9.79E+05	-		9.79E+05	-
13	11/07/2011	13	6	13:24	0	9.79E+05	-		9.79E+05	-	0	9.79E+05	-		9.79E+05	-
14	11/07/2011	14	7	13:30	0	9.22E+05	-		9.22E+05	-	0	9.22E+05	-		9.22E+05	-
17	11/07/2011	17	8	13:50	2	9.42E+05	2.12E-06		9.42E+05	-	0	9.42E+05	-		9.42E+05	-
18	11/07/2011	18	9	13:56	1	9.67E+05	1.03E-06		9.67E+05	-	0	9.67E+05	-		9.67E+05	-
19	11/07/2011	19	10	14:37	0	9.84E+05	-		9.84E+05	-	0	9.84E+05	-		9.84E+05	-
20	11/07/2011	20	11	14:42	0	9.54E+05	-		9.54E+05	-	0	9.54E+05	-		9.54E+05	-
24	11/07/2011	24	12	15:06	0	9.50E+05	-		9.50E+05	-	0	9.50E+05	-		9.50E+05	-
25	11/07/2011	25	13	15:12	0	8.85E+05	-		8.85E+05	-	0	8.85E+05	-		8.85E+05	-
26	11/07/2011	26	14	15:17	0	9.32E+05	-		9.32E+05	-	0	9.32E+05	-		9.32E+05	-
27	11/07/2011	27	15	15:21	0	9.86E+05	-		9.86E+05	-	0	9.86E+05	-		9.86E+05	-
29	11/07/2011	29	16	15:37	0	9.80E+05	-		9.80E+05	-	0	9.80E+05	-		9.80E+05	-
30	11/07/2011	30	17	15:42	0	1.00E+06	-		1.00E+06	-	0	1.00E+06	-		1.00E+06	-
31	11/07/2011	31	18	17:01	1	9.53E+05	1.05E-06		9.53E+05	-	0	9.53E+05	-		9.53E+05	-
32	11/07/2011	32	19	17:05	0	9.31E+05	-		9.31E+05	-	0	9.31E+05	-		9.31E+05	-
33	11/07/2011	33	20	17:11	0	9.29E+05	-		9.29E+05	-	0	9.29E+05	-		9.29E+05	-
35	11/07/2011	35	21	17:30	0	8.85E+05	-		8.85E+05	-	0	8.85E+05	-		8.85E+05	-
36	11/07/2011	36	22	17:34	0	9.57E+05	-		9.57E+05	-	0	9.57E+05	-		9.57E+05	-
38	11/07/2011	38	23	18:05	2	9.46E+05	2.11E-06		9.46E+05	-	0	9.46E+05	-		9.46E+05	-
39	11/07/2011	39	24	18:12	2	9.43E+05	2.12E-06		9.43E+05	-	0	9.43E+05	-		9.43E+05	-
40	11/07/2011	40	25	18:18	1	8.43E+05	1.19E-06		8.43E+05	-	0	8.43E+05	-		8.43E+05	-
45	11/07/2011	45	26	18:49	1	8.75E+05	1.14E-06		8.75E+05	-	0	8.75E+05	-		8.75E+05	-
46	11/07/2011	46	27	18:57	28	9.70E+05	2.89E-05		9.70E+05	-	0	9.70E+05	-		9.70E+05	-
47	11/07/2011	47	28	19:05	42	9.41E+05	4.46E-05		9.41E+05	-	0	9.41E+05	-		9.41E+05	-
50	11/07/2011	50	29	19:33	28	8.58E+05	3.26E-05		8.58E+05	-	0	8.58E+05	-		8.58E+05	-
51	11/07/2011	51	30	19:36	27	9.02E+05	2.99E-05		9.02E+05	-	0	9.02E+05	-		9.02E+05	-
52	11/07/2011	52	31	19:41	18	8.12E+05	2.22E-05		8.12E+05	-	0	8.12E+05	-		8.12E+05	-
54	11/07/2011	54	32	20:01	21	8.36E+05	2.51E-05		8.36E+05	-	0	8.36E+05	-		8.36E+05	-
56	11/07/2011	56	34	20:09	16	8.98E+05	1.78E-05		8.98E+05	-	0	8.98E+05	-		8.98E+05	-
59	11/07/2011	59	35	20:43	-	-	-	-	-	-	-	-	-	-	-	-
60	11/07/2011	60	36	20:46	-	-	-	-	-	-	-	-	-	-	-	-
61	11/07/2011	61	37	20:57	-	-	-	-	-	-	-	-	-	-	-	-
62	11/07/2011	62	38	21:25	-	-	-	-	-	-	-	-	-	-	-	-
65	11/07/2011	65	39	21:59	-	-	-	-	-	-	-	-	-	-	-	-
66	11/07/2011	66	40	22:04	-	-	-	-	-	-	-	-	-	-	-	-
68	11/07/2011	68	41	22:12	-	-	-	-	-	-	-	-	-	-	-	-
69	11/07/2011	69	42	22:30	-	-	-	-	-	-	-	-	-	-	-	-
71	11/07/2011	71	43	22:56	-	-	-	-	-	-	-	-	-	-	-	-
73	11/07/2011	73	44	23:30	-	-	-	-	-	-	-	-	-	-	-	-

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