Application Note

Charging Capacitive Loads with Smart High-Side Switches

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ABSTRACT

TI's smart high-side switches (HSS) can be useful in charging capacitive loads due to the current limit feature which helps suppress inrush current. The current limit and thermal protection circuitry help make the system more reliable and robust by limiting overcurrent caused by the capacitive load. This application note summarizes how the current limit and junction temperature affect the ability of a switch to successfully charge a capacitor.

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1 Introduction

HSSs are used in many applications to power capacitive loads in parallel with resistive loads. Capacitors are also commonly placed on the output of systems to improve EMI performance, filter voltage transients, and so forth. Depending on the capacitance, significant inrush current can occur; this behavior can also be compared to a short to ground scenario. By setting a current limit using the current limit (CL) pin, this inrush current drawn by the capacitor can be reduced. By using Equation 1, users can predict the amount of inrush the system experiences, which is dependent on the capacitance of the load and the change in voltage over time.

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dT} \quad (1)$$

1.1 Capacitive Load Nature

A capacitor is considered fully charged when the output voltage reaches the supply voltage (VS) level. At the same time, the capacitor stops drawing current and the resistive load begins sinking current. Figure 1-1 shows that, during start-up, current takes the orange path until the capacitor is fully charged, and then the current takes the green path. On a waveform, when the capacitor is approximately charged to VS, the current stabilizes to the level the resistive load is expected to draw, I = VS/R_{LOAD}.

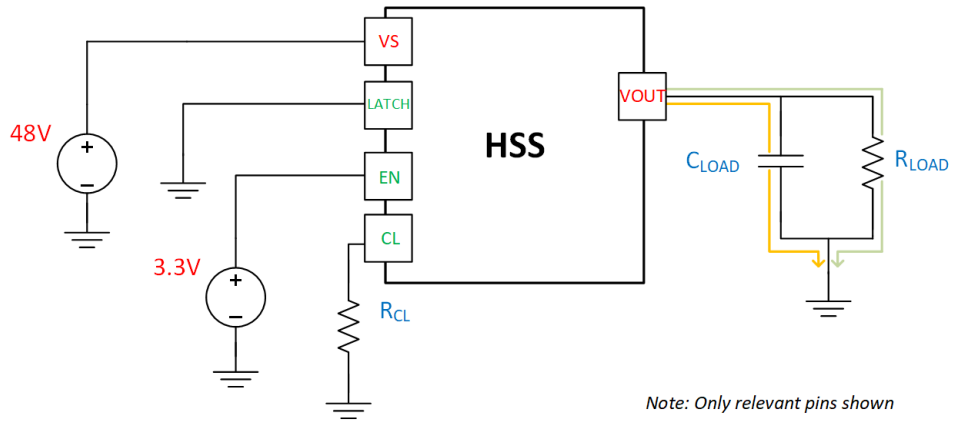


Figure 1-1. Concept Diagram

Based on the following points, the total charge time of the capacitive load also increases with capacitance and temperature:

- Ohm's Law, V = IR, the change in voltage is dependent upon current and resistance. As the junction temperature increases, the on-resistance of the switch also increases, further limiting current flow.
- RC (resistor - capacitor) time constant, τ = RC, where charging time is equal to the resistance times capacitance.

2 Current Limit and Thermal Protection

TI's smart HSSs include a high-accuracy adjustable current limit feature. Typically, the current limit loop takes a few µs to assert. Within the few µs, the inrush current can exceed the limit, but there is an additional internal fast trip level to limit the current for protection. The current limit pin can be configured in one of three ways (one externally and two internally):

1. Connect the CL pin through a resistor to ground to adjust the current limit within the range for the device. The equation or example on how to calculate this can be found in the *Application Information* section of every data sheet. Please make sure the resistor and the current limit is chosen within the stated range for the relevant device or else the current limit is considered *out of range*.
2. Leave the CL pin floating for the CL = open or out of range internal current limit.
3. Connect the CL pin directly to ground for the CL = GND internal current limit.

TI highly recommends that the current limit is set externally using a resistor. The internal limits are designed for fail-safe cases (for example, the external resistor gets damaged), so the device can protect itself and is considered a fault for the device. For methods two and three above, the internal current limits are stated in the *Electrical Characteristics* table of every data sheet.

Other available HSSs do not include this feature or allow the user to adjust the current limit based on application. Some of TI's HSSs also allow the user to dynamically change the current limit meaning set an initial limit for inrush control and change to another value during normal operation.

When the overcurrent threshold is reached, the device responds accordingly based on the device. For the 48V HTC devices, the device clamps the current at the current limit until thermal shutdown is reached. There are two types of thermal shutdown: relative, where the power FET temperature (T_{FET}) is rising much faster than the controller (T_{CON}), and absolute, where the device reaches the absolute reference temperature (T_{ABS}). When the device experiences thermal faults regardless of the type, the output turns off as a protective mechanism. Whether or not the device eventually turns back on after the device recovers from the fault depends on the latch pin configuration. If the latch pin is pulled low, then the device operates in auto-retry mode and if the latch pin is pulled high, then the device is in latch-off mode. The following is a short summary of the thermal faults.

- Relative thermal shutdown
  - $\Delta T = T_{FET} - T_{CON} > T_{REL}$
  - T_{REL}= relative thermal shutdown threshold
  - If latch = low, when t_{RETRY} time is up, then the device or output tries to start back up again.
  - If latch = high, then the output stays off until the latch or enable pin is toggled.
- Absolute thermal shutdown
  - Device reaches T_{ABS}
  - If latch = low, $T_J < T_{ABS} - T_{hys}$ must be true when the t_{RETRY} time is up for the device to try to start back up again.
  - T_{hys} = thermal shutdown hysteresis threshold
  - T_J = junction temperature
  - If latch = high, then the output stays off until the latch or enable pin is toggled.

3 Test Setup and Conditions

For the tests done below, a resistive load was placed in parallel with the capacitive load. The load current (I_{LOAD} = I_L) was set to half of the externally set current limit.

$$R_{LOAD} = \frac{VS}{I_{LOAD}}, \quad I_{LOAD} = \frac{I_{CL}}{2} \tag{2}$$

This experiment evaluates how the current limit (MIN – CL lower limit, TYP – CL midpoint, MAX – CL upper limit) and temperature (25°C, 85°C) affect the ability of the switch to successfully charge capacitive loads.

Equipment:

- TI EVMs – TPS1HTC30EVM & TPS1HTC100EVM
- E-load in constant resistance mode
- Function generator – 3.3V DC signal
- Power supply – 48V
- Electrolytic capacitors (rated 50V or higher)
- Temperature chamber (85°C)
- 0805 surface mount resistors (10kΩ, 16.7kΩ, 20kΩ, 50kΩ)

Note

51kΩ was used since 50kΩ was not readily available.

- Cables
- Voltage and current probes
- Safety box or enclosure (optional)

To eliminate any unwanted or abnormal behavior occurring with TI's HSSs, make sure to use the e-load in constant resistance mode. Constant current mode does not accurately depict the behavior of a purely resistive load because the load is always constantly drawing a preset current. Refer to (+) [FAQ] Why does my e-load cause my high side switch to shut down? - Power management forum - Power management - TI E2E support forums for more information.

When using an e-load, unless the resistive load is actively *on*, the device detects an open-load fault. For each test, the following were the sequence of steps followed:

1. Connect electrolytic capacitor on the output in parallel with the resistive load. The anode or positive (longer) lead was connected to power and cathode or negative (shorter) lead to ground.
2. Turn on the e-load after configuring the appropriate resistance for the current limit being tested.
3. Turn on the input power supply to be in a high and stable condition.
4. Trigger the 3.3V EN high signal using the function generator.
5. Note the results and turn off the power supplies.

3.1 Probe and Jumper Configuration

Refer to Figure 3-1 and Figure 3-2 for the jumper configuration (yellow), probe (red) locations, and an image of the test setup.

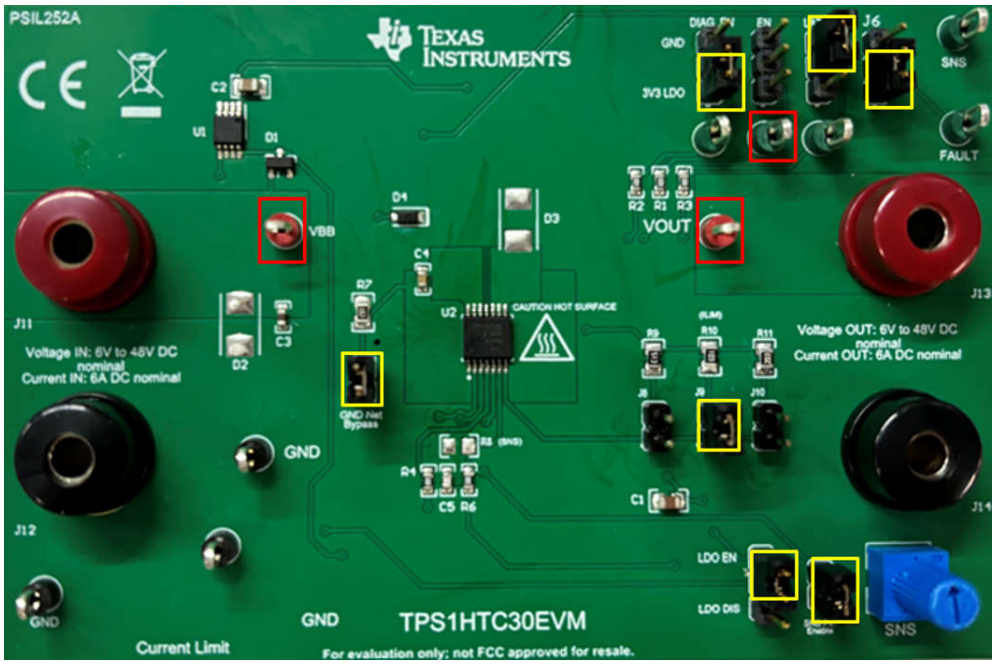


Figure 3-1. EVM Jumper and Probe Configuration

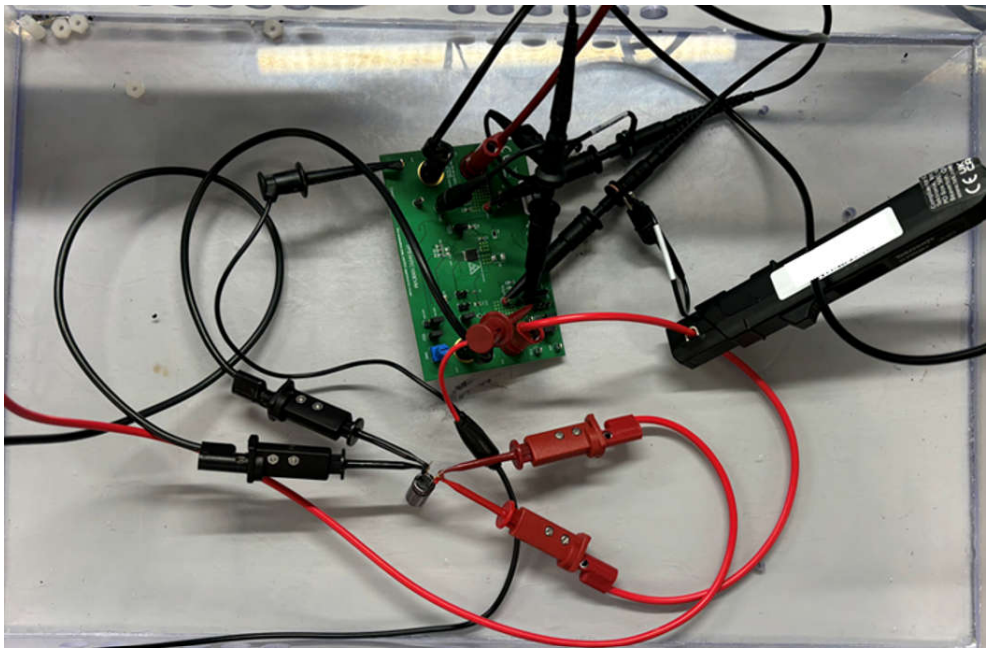


Figure 3-2. Setup

4 Results

The *x* in Table 4-1 and Table 4-2 indicates where the device begins to go into thermal shutdown. Capacitors higher than that can be fully charged but only after the device auto-retries several times. For some users, the output turning on and off multiple times before fully charging the capacitive load can be inefficient and timely for certain applications. Figure 4-1 shows an example waveform during normal operation where the capacitor is charged without encountering a thermal fault.

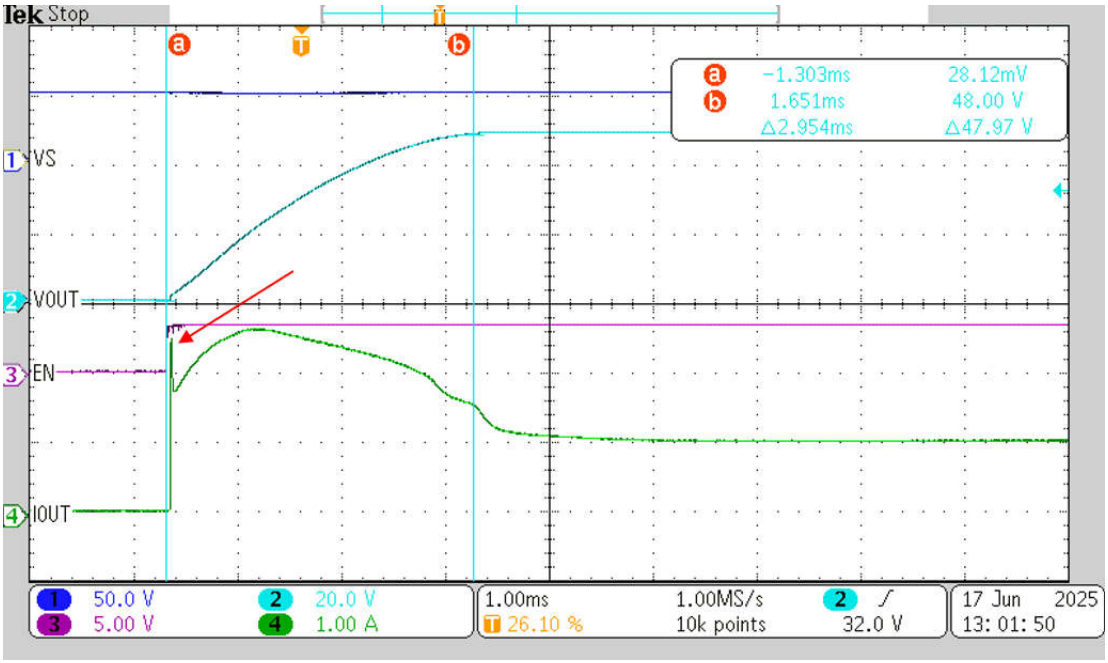
As the current limit decreases, the amount of capacitance that can be charged with the switch increases. In some cases, when charging large capacitors while utilizing a lower current limit where thermal shutdown occurs but the output is successfully charged, the VOUT curve looks more like a step function as shown in Figure 4-2. In other cases, where a higher current limit is utilized, the output voltage is not able to charge to VS as shown in Figure 4-3 regardless of the time period. The higher the inrush or load current, the more the power dissipation over the FET. The faster the device heats up, the more quickly the device reaches the thermal shutdown threshold. By configuring the device to a lower current limit, the device heats up less and recovers faster, slowly charging the large capacitor in small steps.

Be careful of slight inaccuracies due to minor voltage offsets with the measuring equipment, which also can affect the total charge time. Expect that large capacitors take more time to charge relative to small ones and that the time takes longer for those same capacitors to charge at higher temperatures. For these results, the capacitor was considered fully charged once the output voltage reached approximately 46-48V. This was based on where the output voltage stopped increasing. At the same voltage point, the current can also take slightly longer to stabilize at the load current level where only the resistive load is drawing current. The data tables show approximate charging times for the devices tested and can vary across process, voltage, and temperature (PVT) and with board layout (if not using an EVM). The key concept here is recognizing at which capacitance the device begins to experience a thermal fault.

At higher drain to source voltages, such as 48V and with higher inrush or load currents, the point where the device limits current can be higher than the target limit. This is because there is more power dissipation over the FET. The power FET heats up more relative to the current limit sense FET because there is much less current going through – I_{LOAD}/K_{CL} (current mirror mechanism). Eventually, due to mutual heating, the power FET causes the sense FET to start heating up so the two FETs get closer in temperature. Over time, the device is able to better regulate the current. This does not affect the reliability of the device.

4.1 Example Waveforms

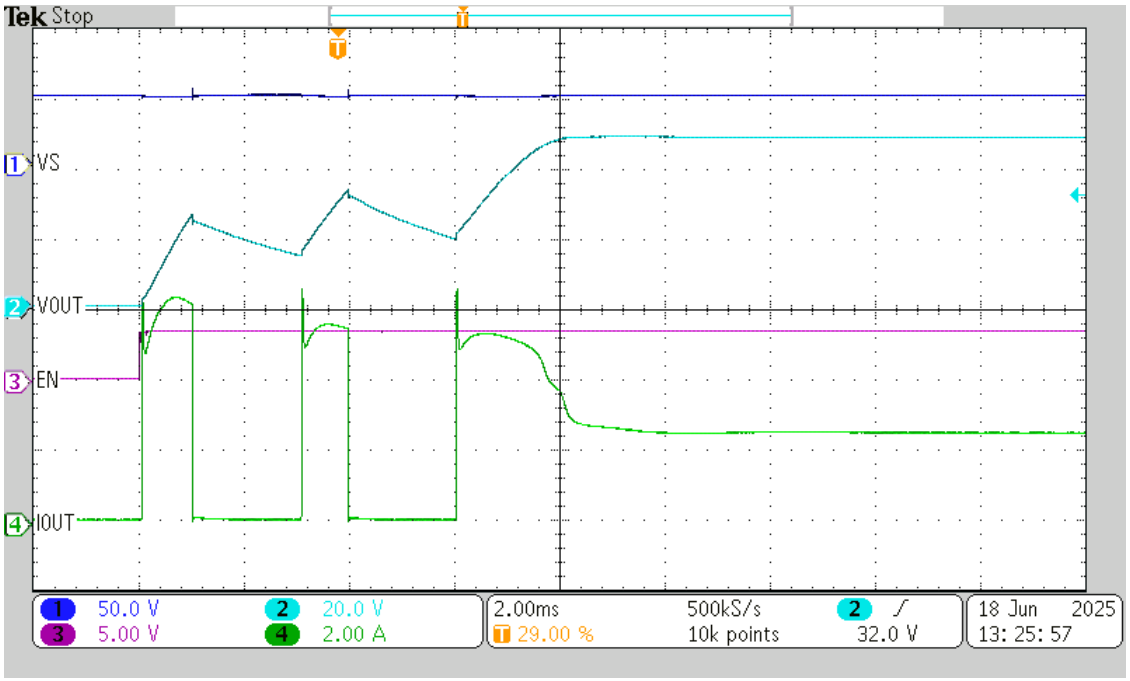
Cursor a - the switch is enabled. Cursor b - the capacitor is fully charged. The red arrow shows the inrush current that occurs before the current limit loop asserts.



A. TPS1HTC30-Q1, CL lower limit – 2A, 100 uF, 25°C

Figure 4-1. Capacitive Load Charging Behavior - No Thermal Fault

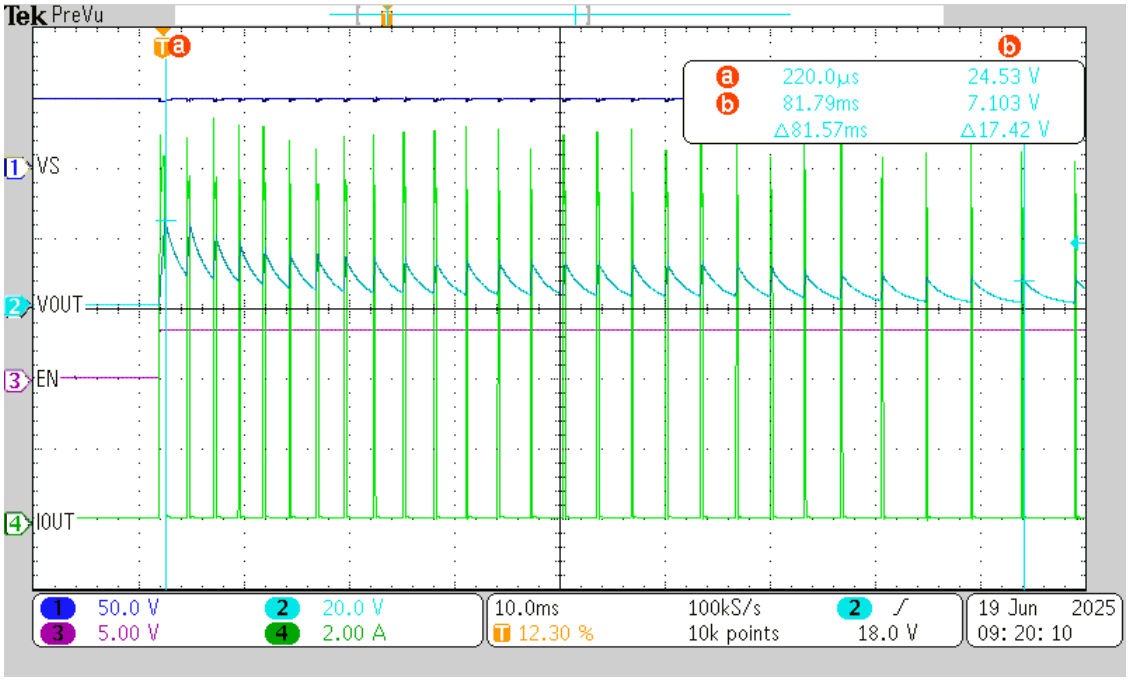
The device is eventually able to charge after turning on or off (auto-retry) several times.



A. TPS1HTC30-Q1, CL midpoint – 5A, 220 uF, 25°C

Figure 4-2. Capacitive Load Charging Behavior - Thermal Fault

The device is not able to charge the output to VS.



A. TPS1HTC30-Q1, CL upper limit – 10A, 180 uF, 25°C

Figure 4-3. Capacitive Load Charging Behavior - Fail Case

4.2 48V Application Devices

Table 4-1. TPS1HTC30-Q1 Capacitor Charging Times

TPS1HTC30Q1	Capacitor Charging Time (VS = 48V)					
	25°C			85°C		
	CL Lower Limit	CL Midpoint	CL Upper Limit	CL Lower Limit	CL Midpoint	CL Upper Limit
Capacitance (uF)	R_{CL}=50kΩ, I_{CL}=2A, R_L=48Ω, I_L=1A	R_{CL}=20kΩ, I_{CL}=5A, R_L=19.2Ω, I_L=2.5A	R_{CL}=10kΩ, I_{CL}=10A, R_L=9.6Ω, I_L=5A	R_{CL}=50kΩ, I_{CL}=2A, R_L=48Ω, I_L=1A	R_{CL}=20kΩ, I_{CL}=5A, R_L=19.2Ω, I_L=2.5A	R_{CL}=10kΩ, I_{CL}=10A, R_L=9.6Ω, I_L=5A
6.8	817.6us	748.0us	178.00us	810.8us	734.4us	179.2us
10	841.6us	772.8us	595.6us	868.8us	762.4us	631.2us
15	957.6us	816.8us	647.6us	978.8us	816.4us	649.2us
22	1.038ms	870.8us	667.6us	1.509ms	878.4us	693.2us
33	1.278ms	964.8us	731.6us	1.705ms	960.4us	741.2us
47	1.874ms	1.105ms	804.6us	1.994ms	1.096ms	805.2us
68	2.384ms	1.295ms	954.6us	2.537ms	1.314ms	1.001ms
75	2.404ms	1.311ms	972.6us	2.565ms	1.326ms	1.003ms
82	2.554ms	1.377ms	982.6us	2.728ms	1.398ms	1.037ms
100	2.954ms	1.533ms	1.061ms	3.156ms	1.634ms	1.105ms
180	4.291ms	2.162ms	X	4.706ms	2.370ms	X
220	5.302ms	X	-	5.792ms	X	-
330	X	-	-	X	-	-

Table 4-2. TPS1HTC100-Q1 Capacitor Charging Times

TPS1HTC100Q1	Capacitor Charging Time (VS = 48V)					
	25°C			85°C		
	CL Lower Limit	CL Midpoint	CL Upper Limit	CL Lower Limit	CL Midpoint	CL Upper Limit
Capacitance (uF)	R_{CL}=50kΩ, I_{CL}=0.92A, R_L=104.3Ω, I_L=0.46A	R_{CL}=16.7kΩ, I_{CL}=3A R_L=32Ω, I_L=1.5A	R_{CL}=10kΩ, I_{CL}=5.3A, R_L=18.1Ω, I_L=2.65A	R_{CL}=50kΩ, ICL=0.92A, R_L=104.3Ω, I_L=0.46A	R_{CL}=16.7kΩ, I_{CL}=3A, R_L=32Ω, I_L=1.5A	R_{CL}=10kΩ, I_{CL}=5.3A, R_L=18.1Ω, I_L=2.65A
6.8	911.4us	731.4us	699.6us	938.0us	745.0us	732.2us
10	991.4us	735.4us	713.6us	1.032us	757.0us	736.2us
15	1.143ms	751.4us	734.6us	1.196ms	770.5us	753.1us
22	1.323ms	771.4us	742.6us	1.380ms	779.5us	777.1us
33	1.583ms	829.4us	X	1.664ms	840.5us	X
47	1.929ms	X	-	2.065ms	X	-
68	X	-	-	X	-	-

5 Additional Information

The identification tables below help reference the waveform for each test. In place of the time to charge the capacitor, in Section 4, is a number that corresponds to the relevant figure number. All of the figures in this section are labeled as 5-#. The second number is the number from the key table. For example, to look at waveform 6 from the Table 5-1, please refer to Figure 5-6.

Table 5-1. TPS1HTC30-Q1 Capacitor Charging Times Key

TPS1HTC30-Q1	Capacitor Charging Time (VS = 48V)					
	25°C			85°C		
	CL Lower Limit	CL Midpoint	CL Upper Limit	CL Lower Limit	CL Midpoint	CL Upper Limit
Capacitance (uF)	R_{CL}=50kΩ, I_{CL}=2A, R_L=48Ω, I_L=1A	R_{CL}=20kΩ, I_{CL}=5A, R_L=19.2Ω, I_L=2.5A	R_{CL}=10kΩ, I_{CL}=10A, R_L=9.6Ω, I_L=5A	R_{CL}=50kΩ, I_{CL}=2A, R_L=48Ω, I_L=1A	R_{CL}=20kΩ, I_{CL}=5A, R_L=19.2Ω, I_L=2.5A	R_{CL}=10kΩ, I_{CL}=10A, R_L=9.6Ω, I_L=5A
6.8	1	14	26	37	50	62
10	2	15	27	38	51	63
15	3	16	28	39	52	64
22	4	17	29	40	53	65
33	5	18	30	41	54	66
47	6	19	31	42	55	67
68	7	20	32	43	56	68
75	8	21	33	44	57	69
82	9	22	34	45	58	70
100	10	23	35	46	59	71
180	11	24	36	47	60	72
220	12	25	-	48	61	-
330	13	-	-	49	-	-

Table 5-2. TPS1HTC100-Q1 Capacitor Charging Times Key

TPS1HTC100-Q1	Capacitor Charging Time (VS = 48V)					
	25°C			85°C		
	CL Lower Limit	CL Midpoint	CL Upper Limit	CL Lower Limit	CL Midpoint	CL Upper Limit
Capacitance (uF)	R_{CL}=50kΩ, I_{CL}=0.92A, R_L=104.3Ω, I_L=0.46A	R_{CL}=16.7kΩ, I_{CL}=3A, R_L=32Ω, I_L=1.5A	R_{CL}=10kΩ, I_{CL}=5.3A, R_L=18.1Ω, I_L=2.65A	R_{CL}=50kΩ, I_{CL}=0.92A, R_L=104.3Ω, I_L=0.46A	R_{CL}=16.7kΩ, I_{CL}=3A, R_L=32Ω, I_L=1.5A	R_{CL}=10kΩ, I_{CL}=5.3A, R_L=18.1Ω, I_L=2.65A
6.8	73	80	86	91	98	104
10	74	81	87	92	99	105
15	75	82	88	93	100	106
22	76	83	89	94	101	107
33	77	84	90	95	102	108
47	78	85	-	96	103	-
68	79	-	-	97	-	-

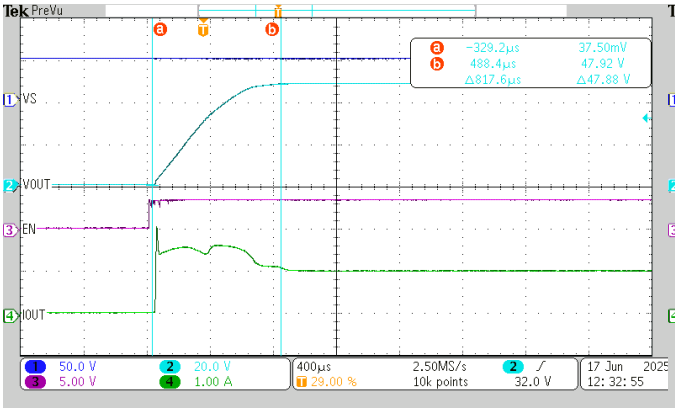


Figure 5-1. Test Condition 1

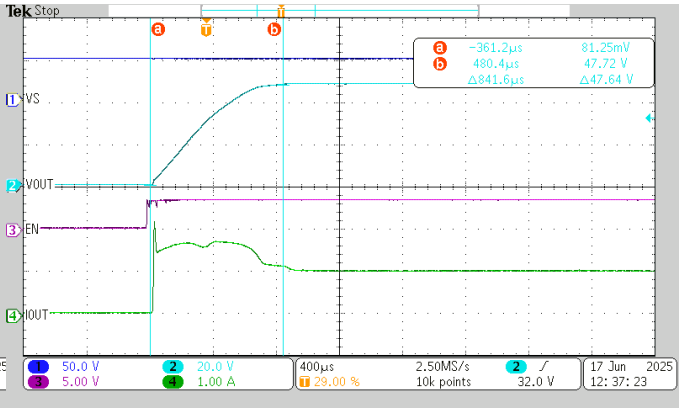


Figure 5-2. Test Condition 2

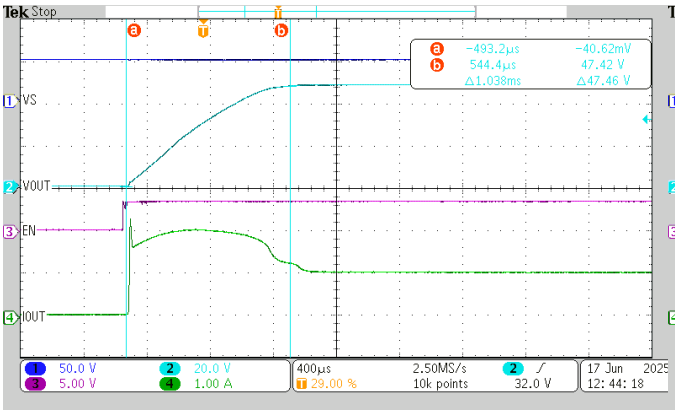


Figure 5-3. Test Condition 3

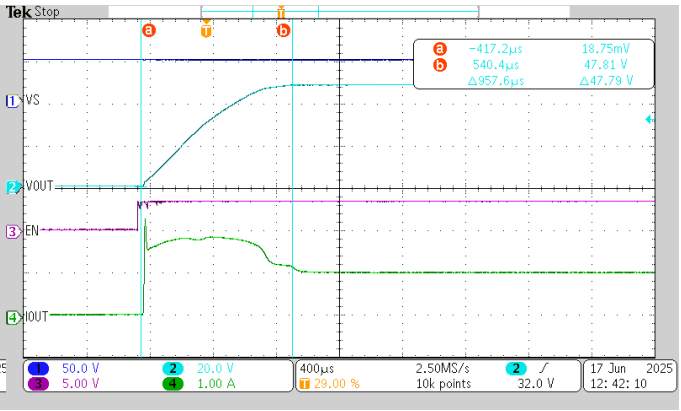


Figure 5-4. Test Condition 4

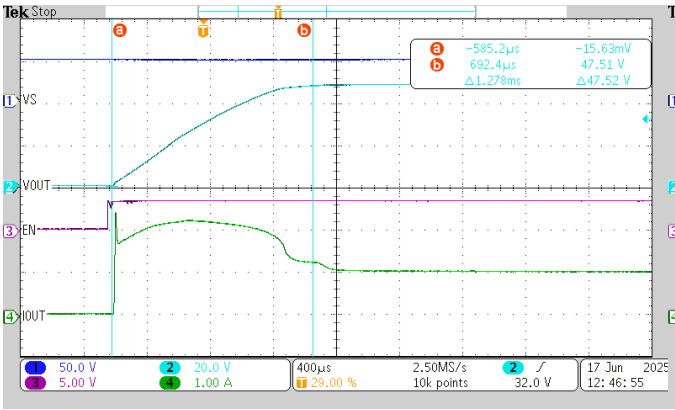


Figure 5-5. Test Condition 5

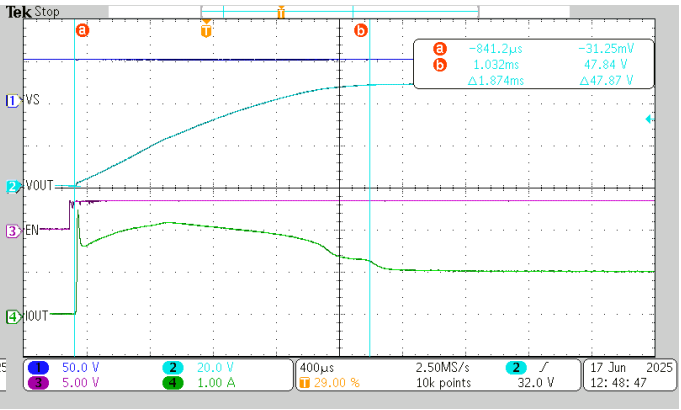


Figure 5-6. Test Condition 6

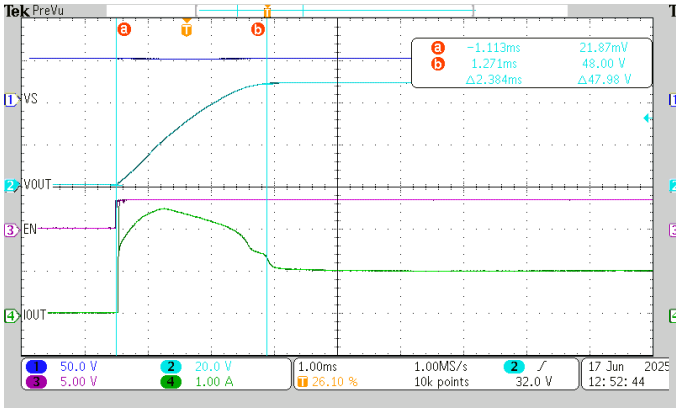


Figure 5-7. Test Condition 7

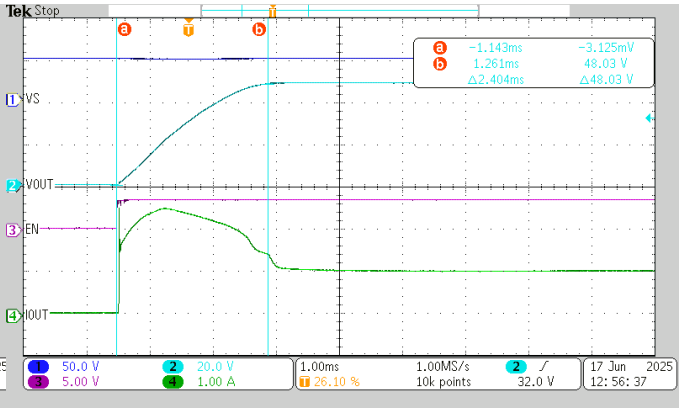


Figure 5-8. Test Condition 8

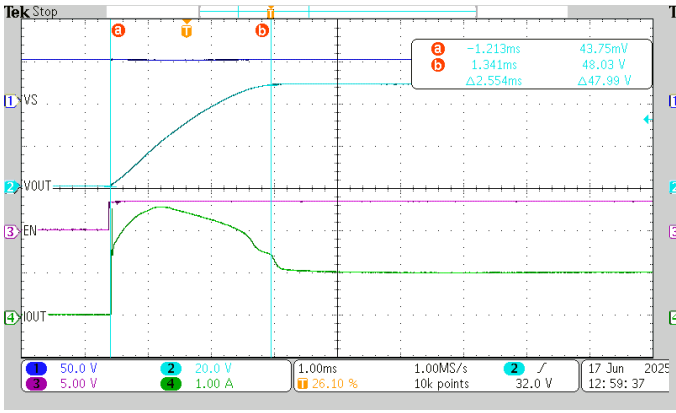


Figure 5-9. Test Condition 9

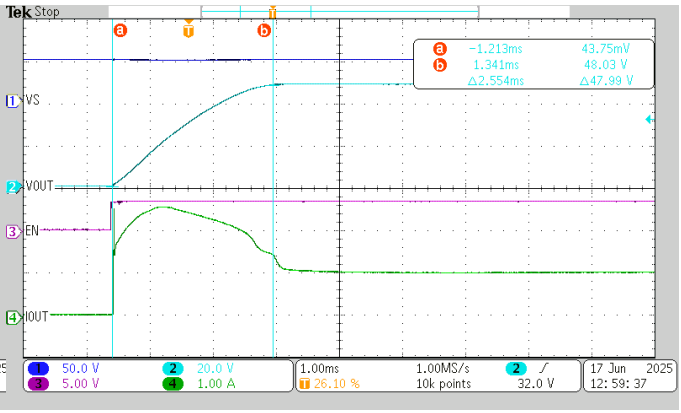


Figure 5-10. Test Condition 10

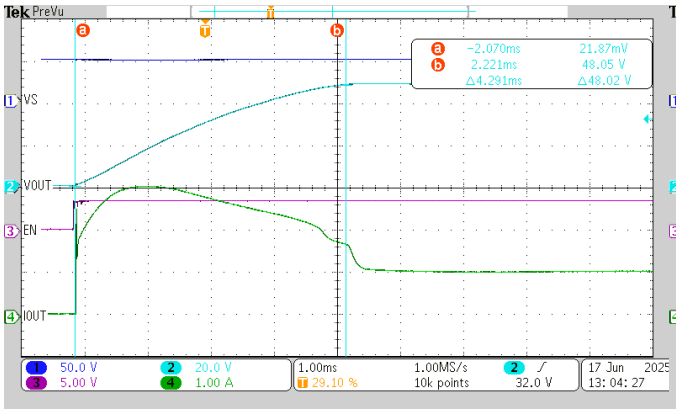


Figure 5-11. Test Condition 11

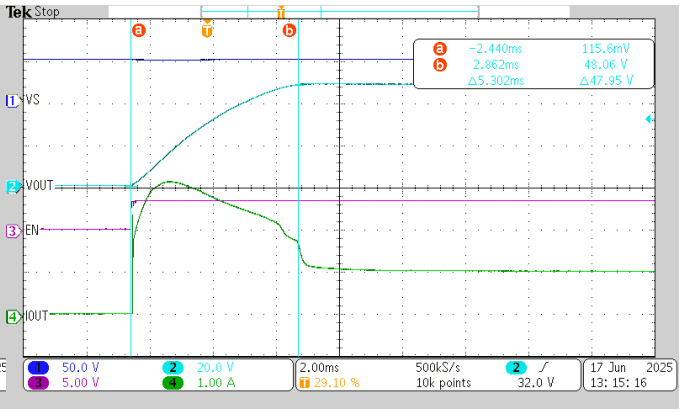


Figure 5-12. Test Condition 12

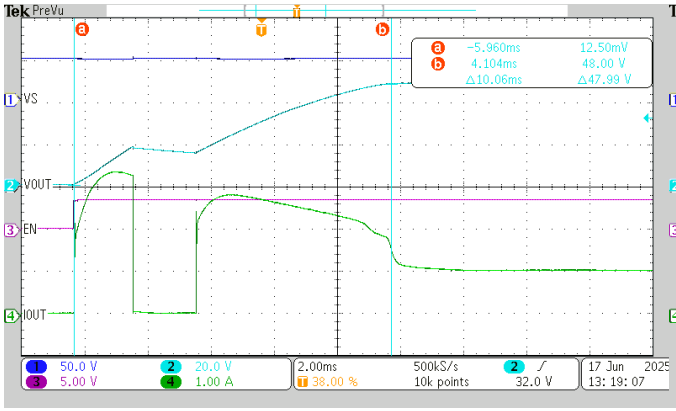


Figure 5-13. Test Condition 13

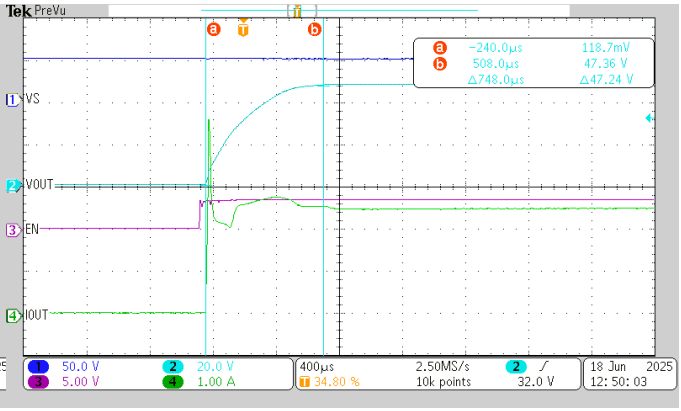


Figure 5-14. Test Condition 14

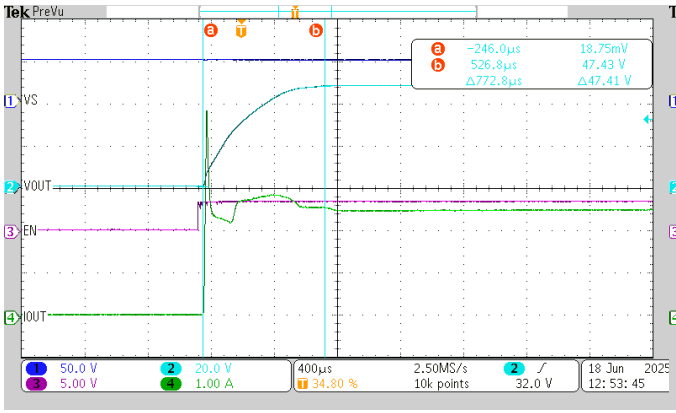


Figure 5-15. Test Condition 15

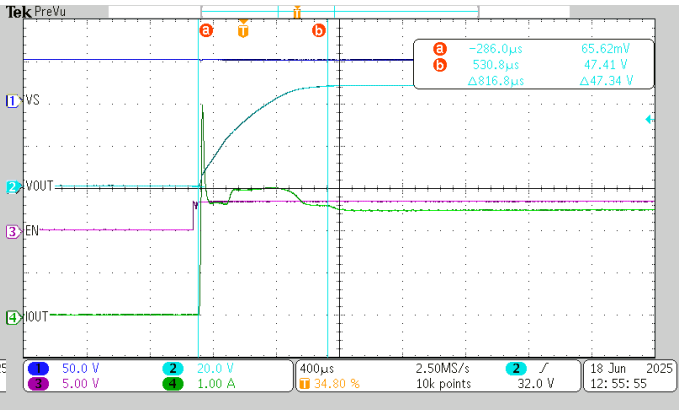


Figure 5-16. Test Condition 16

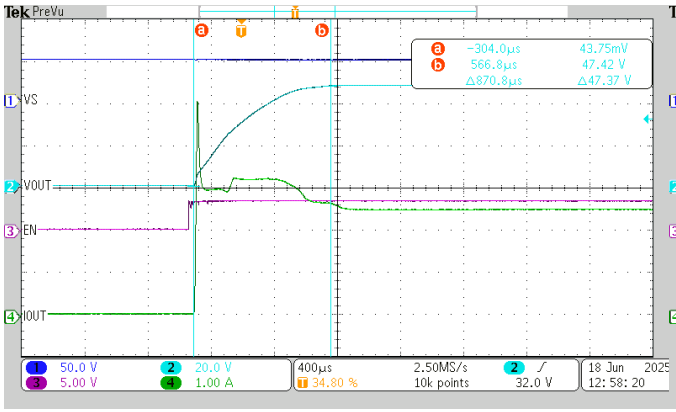


Figure 5-17. Test Condition 17

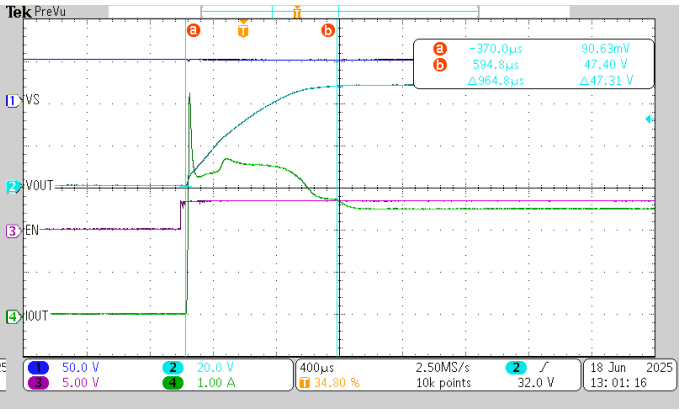


Figure 5-18. Test Condition 18

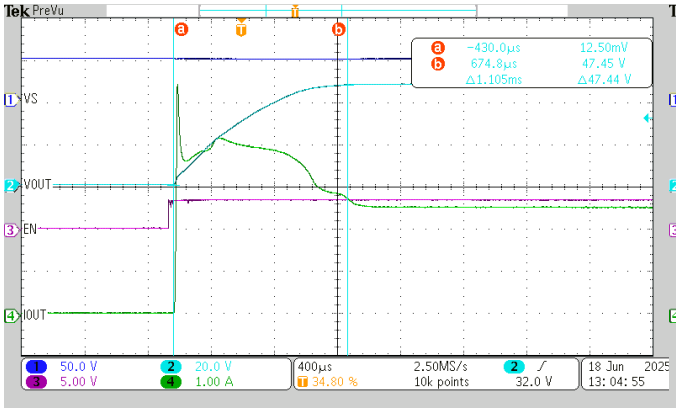


Figure 5-19. Test Condition 19

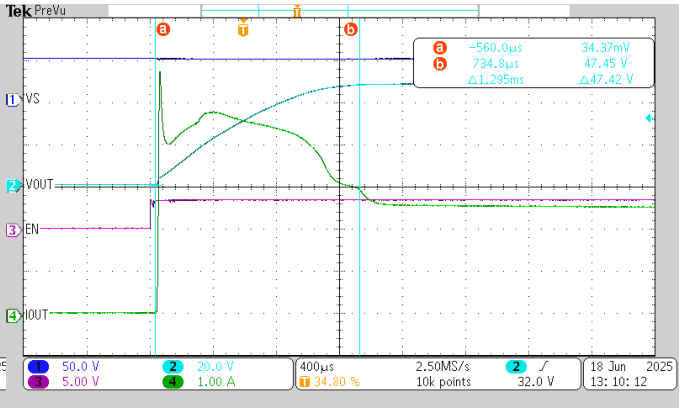


Figure 5-20. Test Condition 20

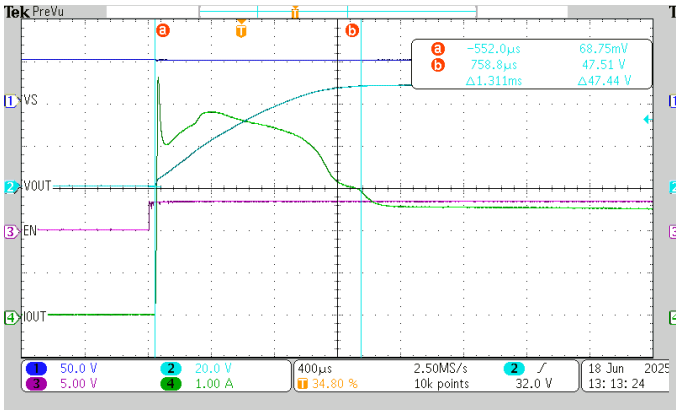
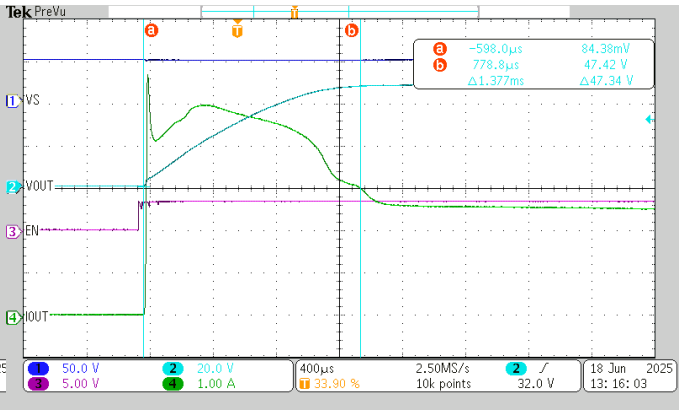


Figure 5-21. Test Condition 21



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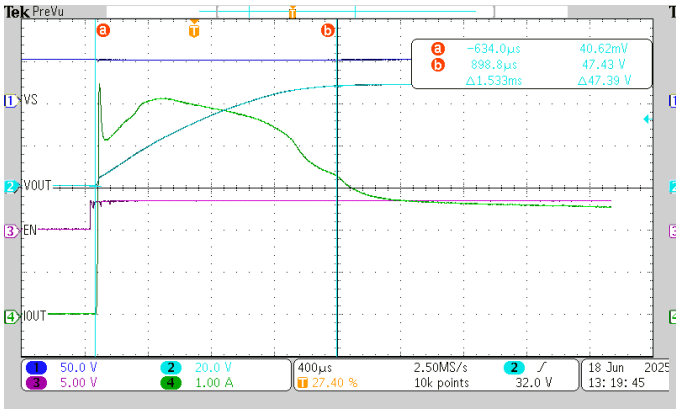

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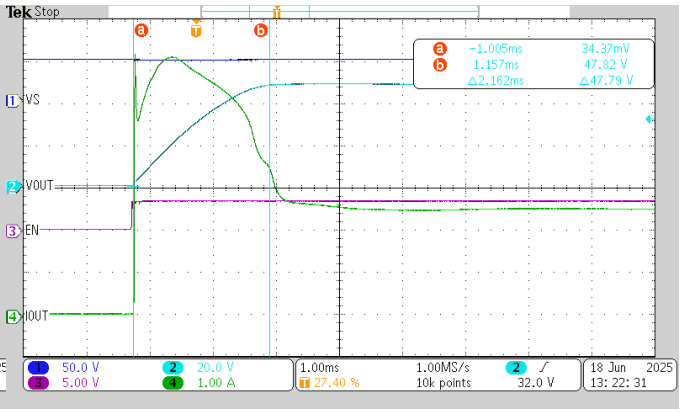
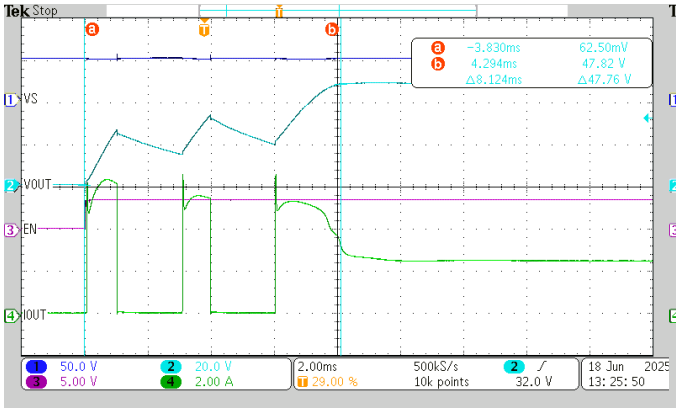


Figure 5-24. Test Condition 24



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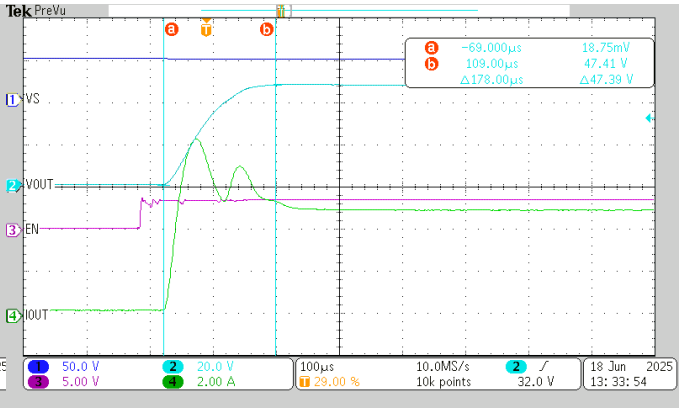


Figure 5-26. Test Condition 26

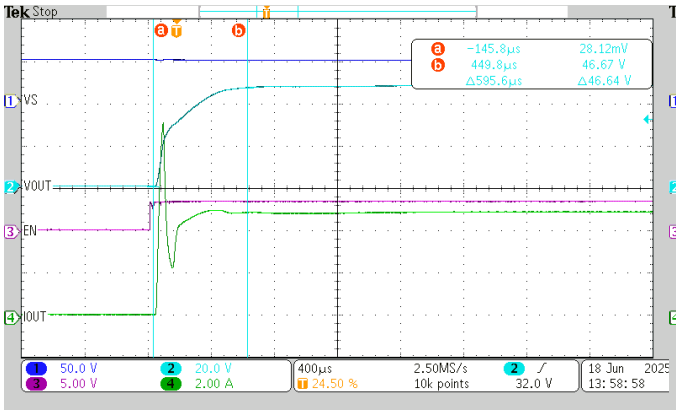


Figure 5-27. Test Condition 27

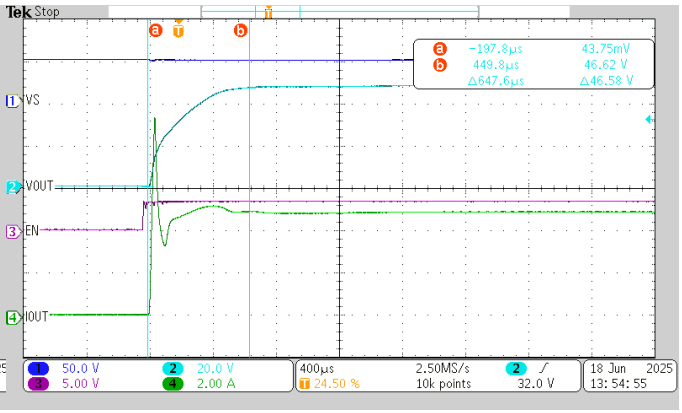
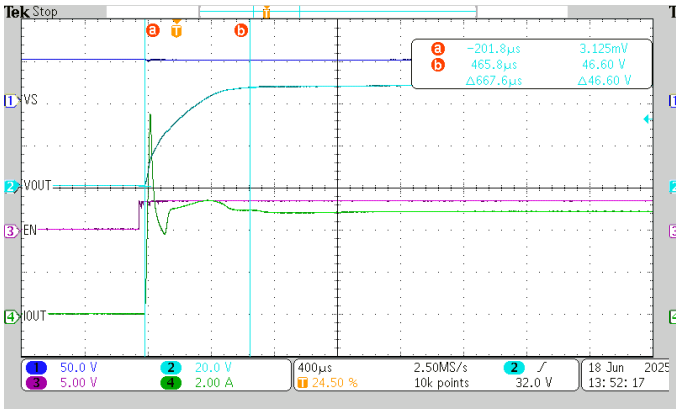


Figure 5-28. Test Condition 28



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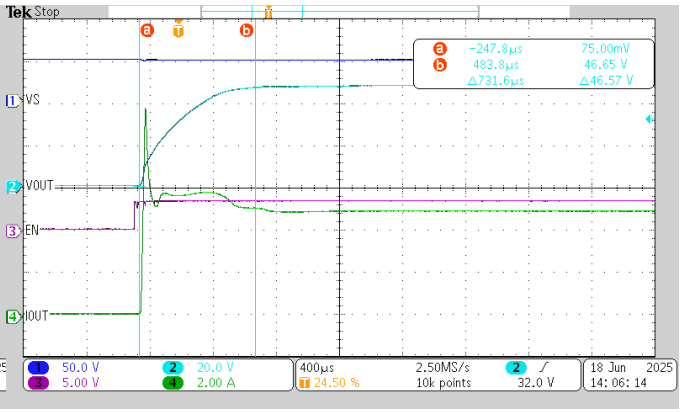

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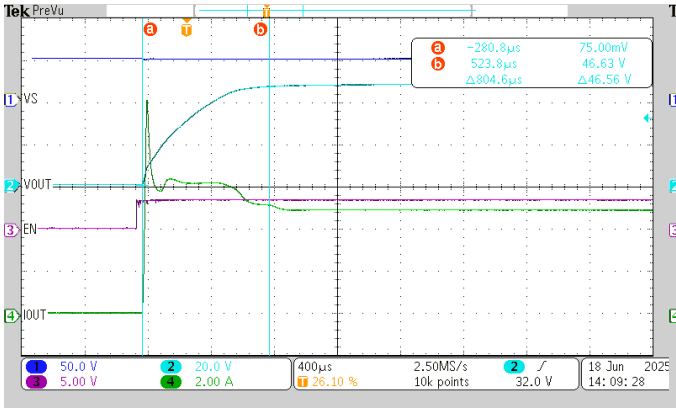

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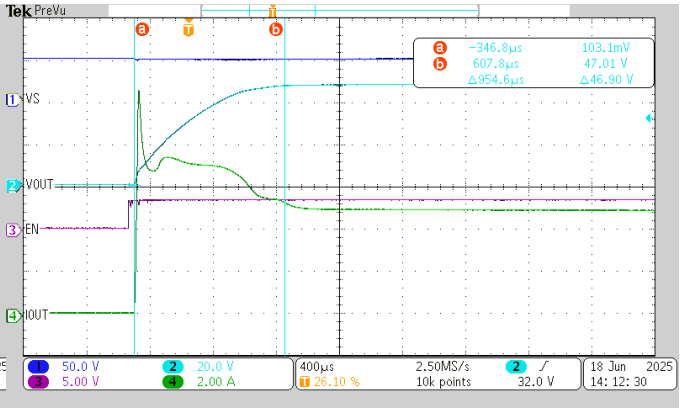


Figure 5-32. Test Condition 32

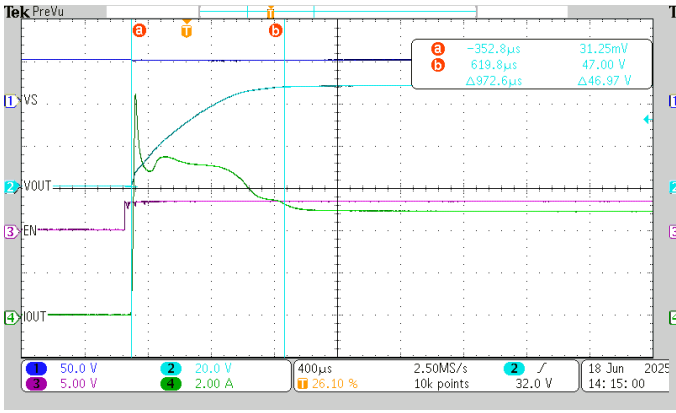


Figure 5-33. Test Condition 33

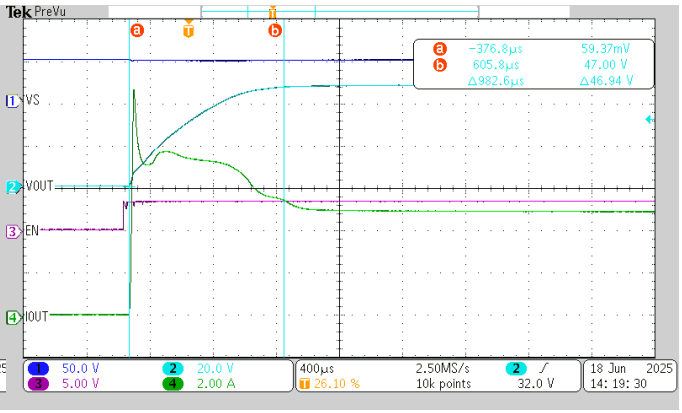
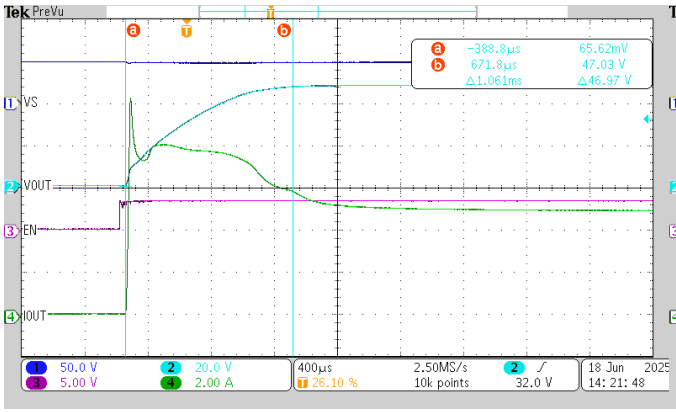


Figure 5-34. Test Condition 34



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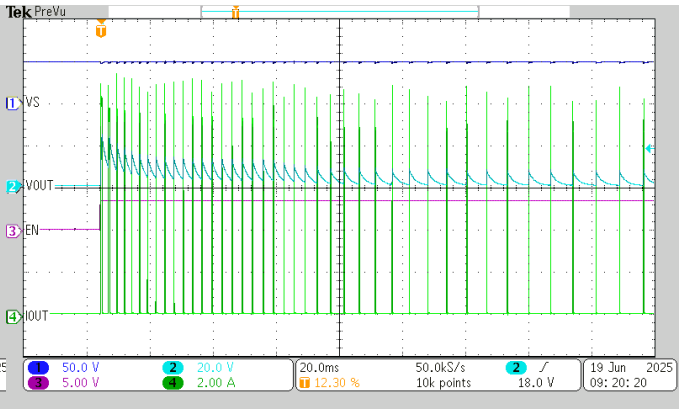


Figure 5-36. Test Condition 36

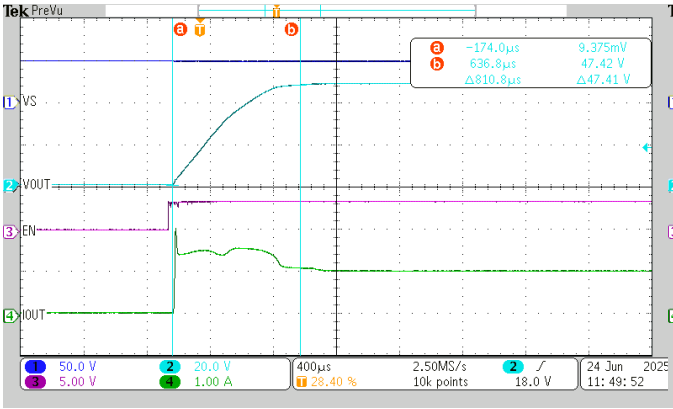


Figure 5-37. Test Condition 37

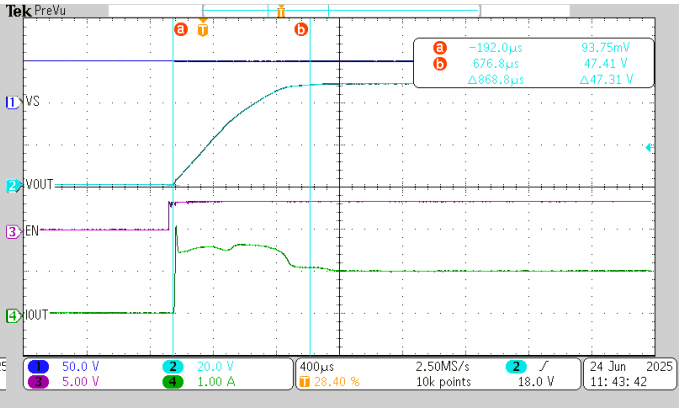


Figure 5-38. Test Condition 38

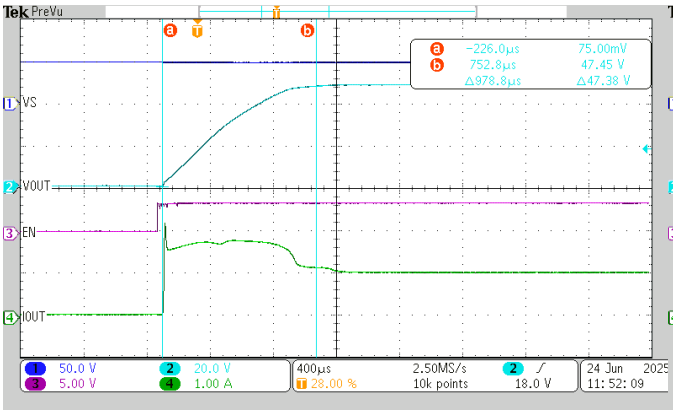


Figure 5-39. Test Condition 39

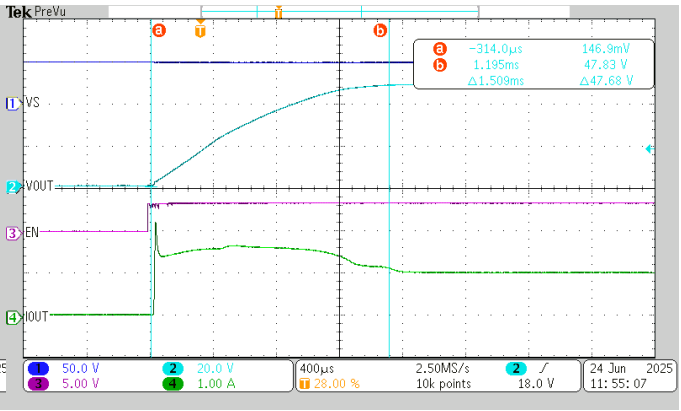


Figure 5-40. Test Condition 40

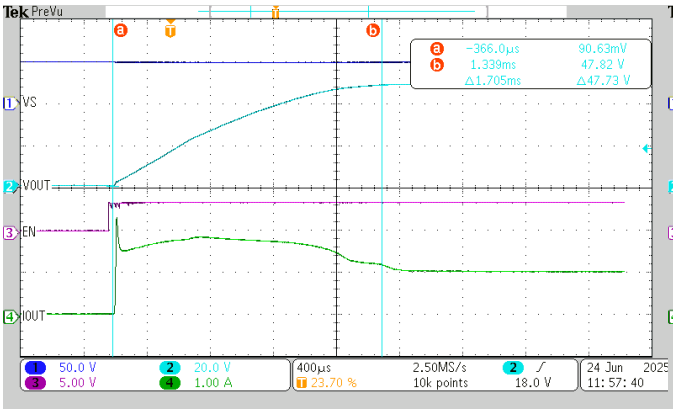


Figure 5-41. Test Condition 41

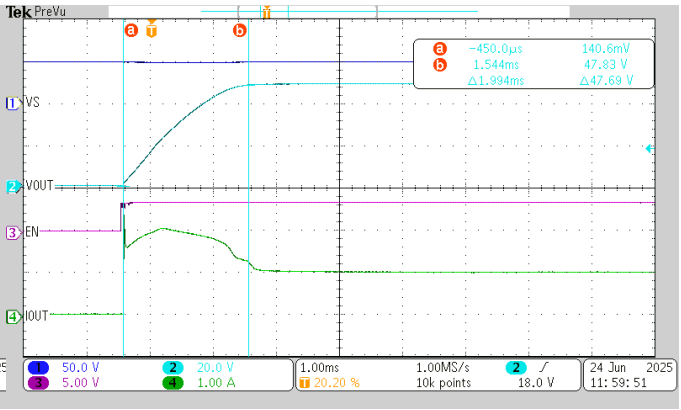


Figure 5-42. Test Condition 42

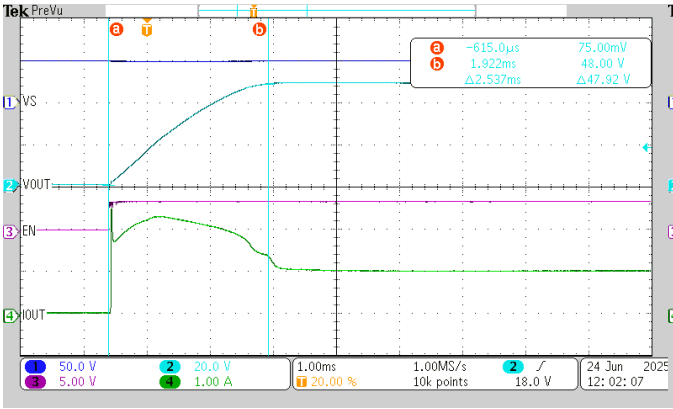


Figure 5-43. Test Condition 43

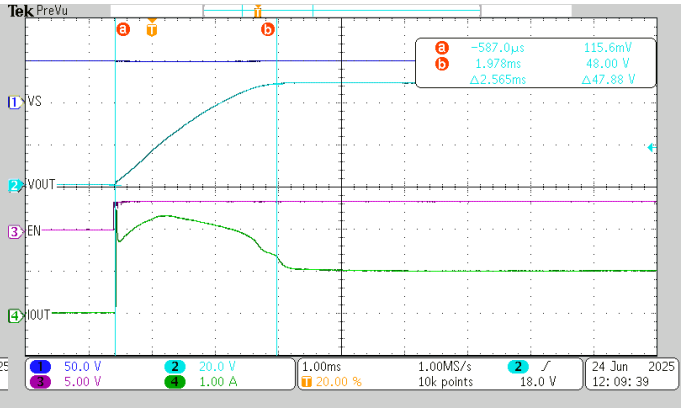


Figure 5-44. Test Condition 44

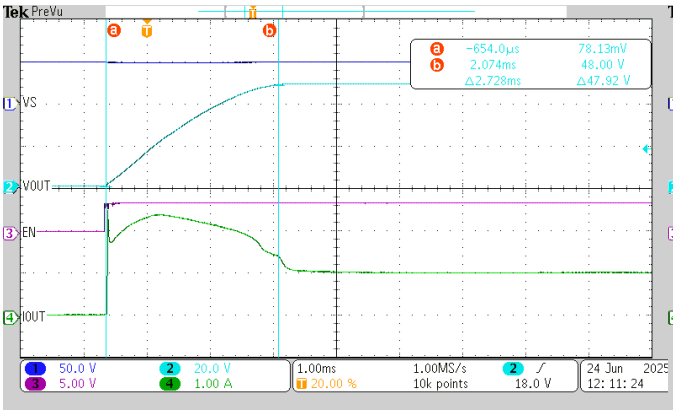


Figure 5-45. Test Condition 45

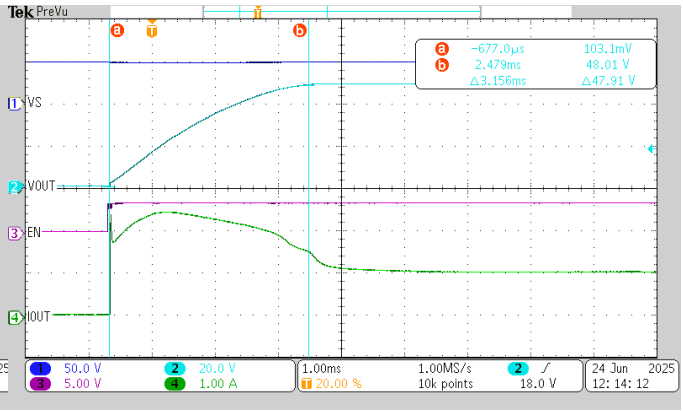
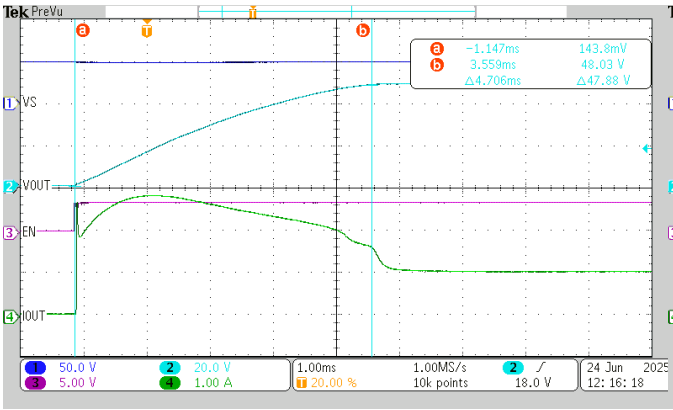


Figure 5-46. Test Condition 46



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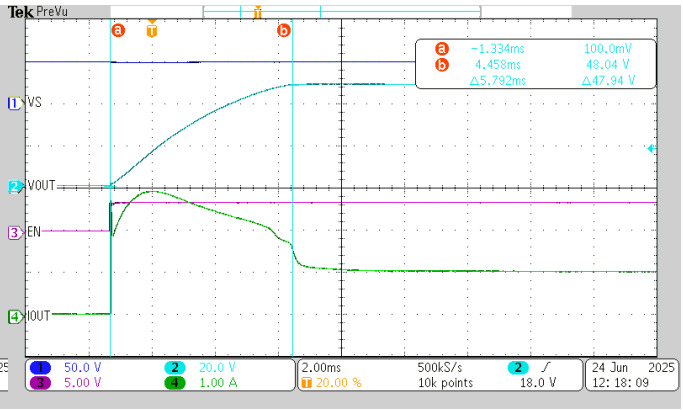


Figure 5-48. Test Condition 48

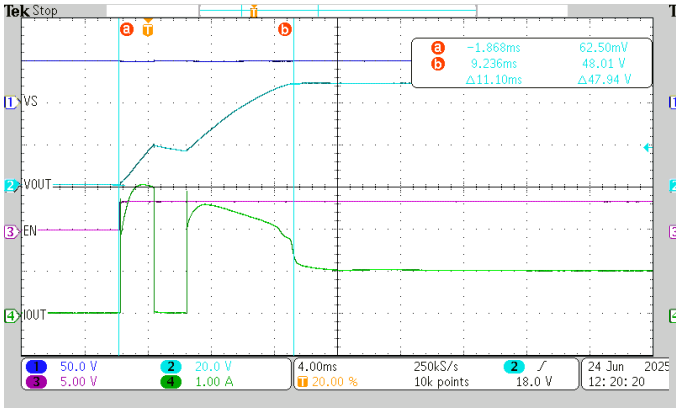


Figure 5-49. Test Condition 49

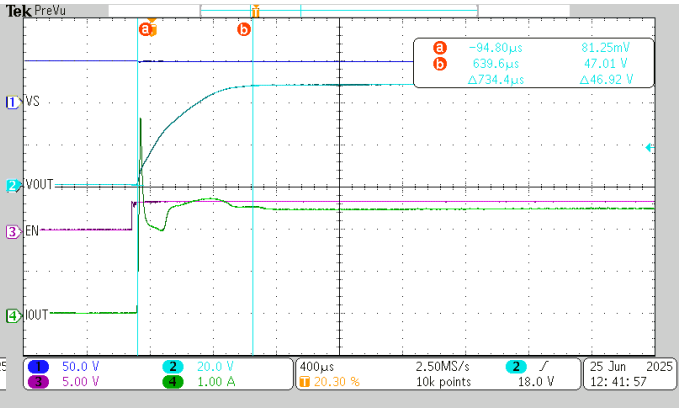


Figure 5-50. Test Condition 50

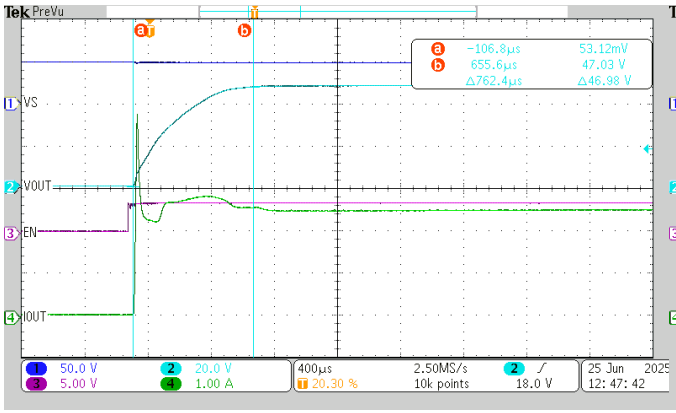


Figure 5-51. Test Condition 51

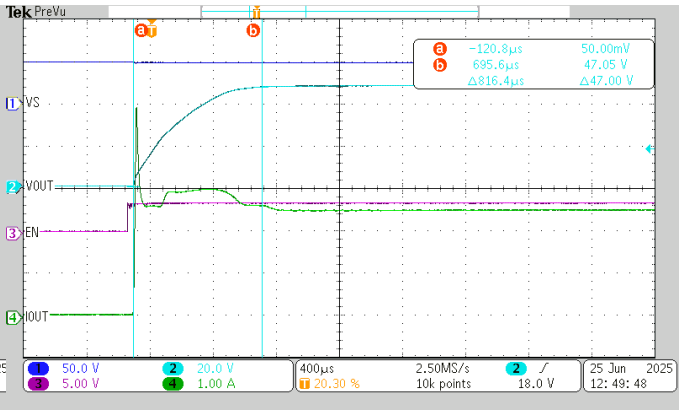


Figure 5-52. Test Condition 52

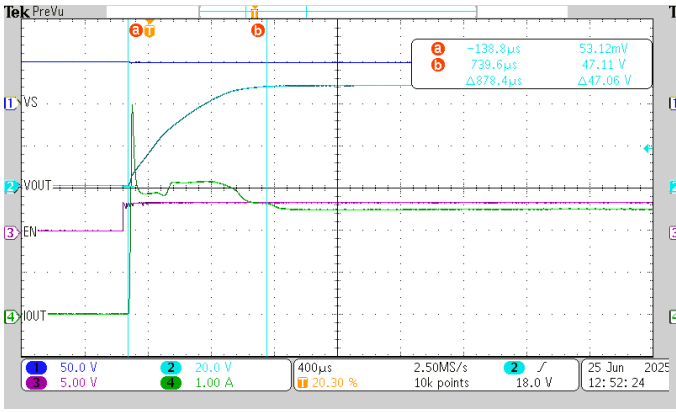


Figure 5-53. Test Condition 53

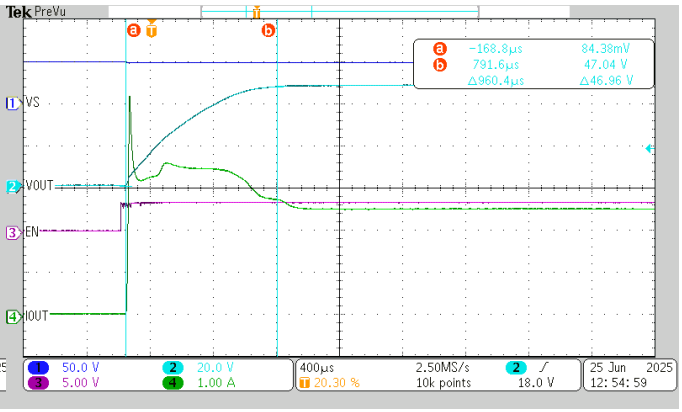


Figure 5-54. Test Condition 54

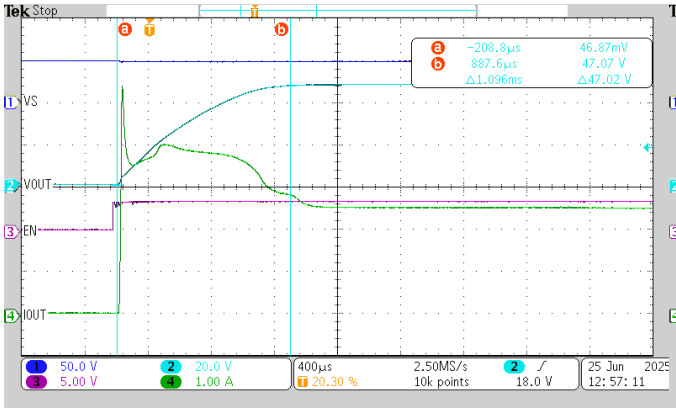


Figure 5-55. Test Condition 55

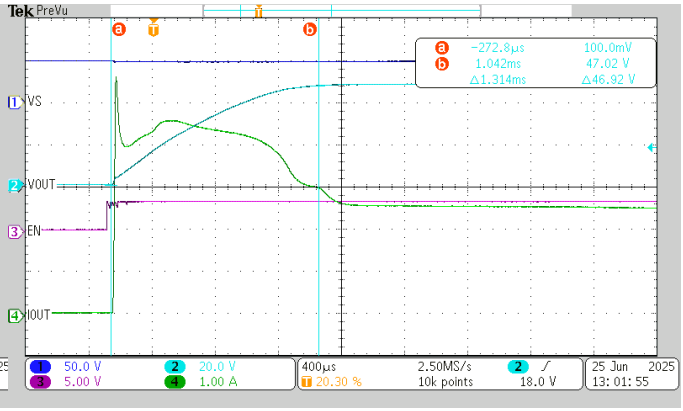


Figure 5-56. Test Condition 56

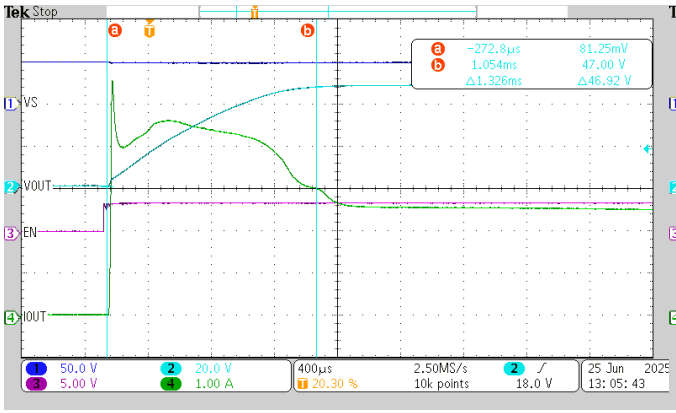


Figure 5-57. Test Condition 57

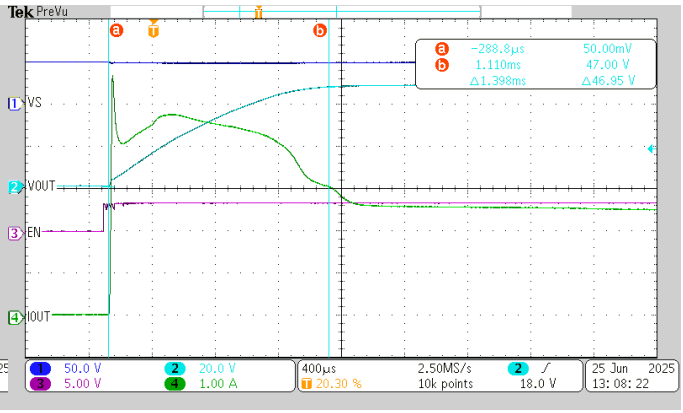


Figure 5-58. Test Condition 58

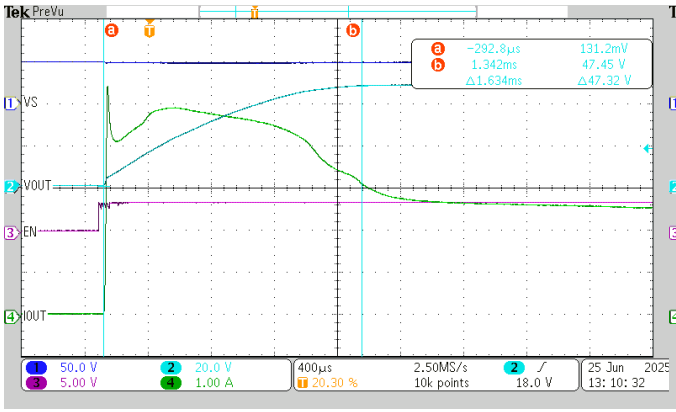


Figure 5-59. Test Condition 59

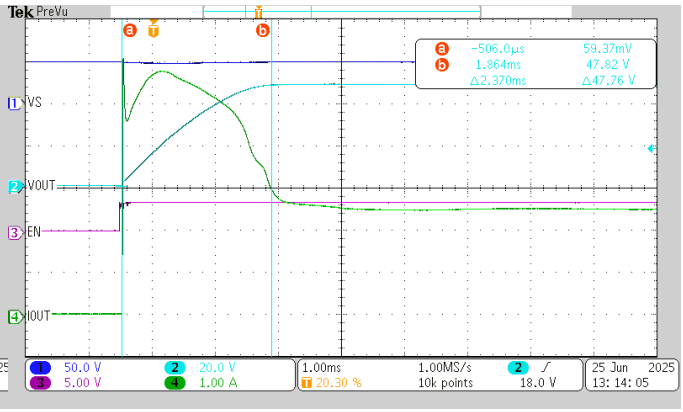


Figure 5-60. Test Condition 60

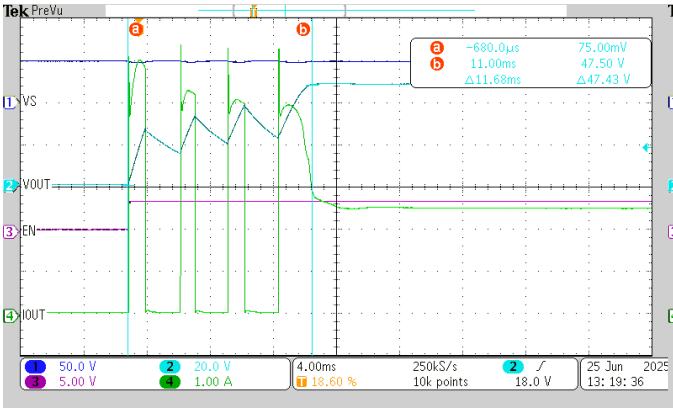


Figure 5-61. Test Condition 61

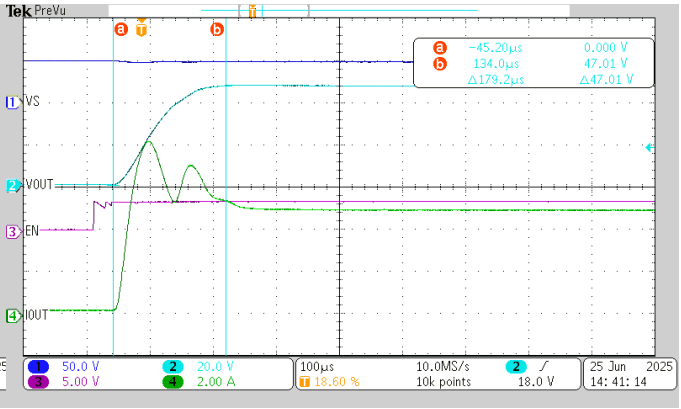


Figure 5-62. Test Condition 62

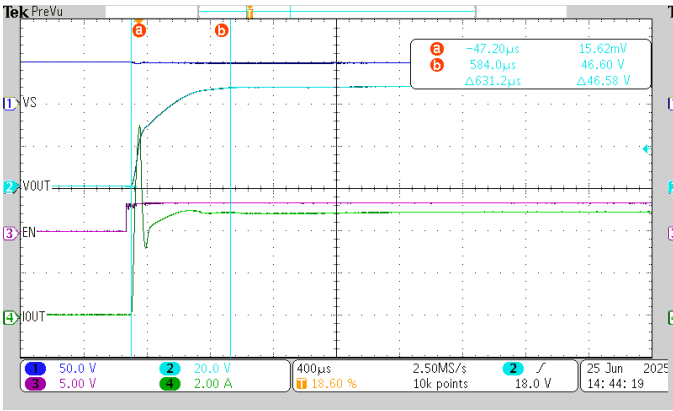


Figure 5-63. Test Condition 63

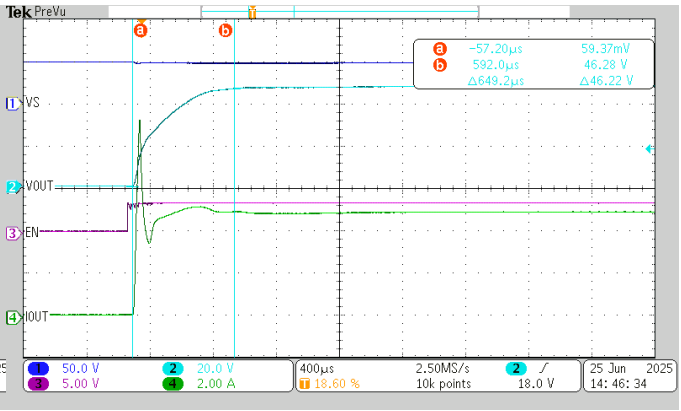


Figure 5-64. Test Condition 64

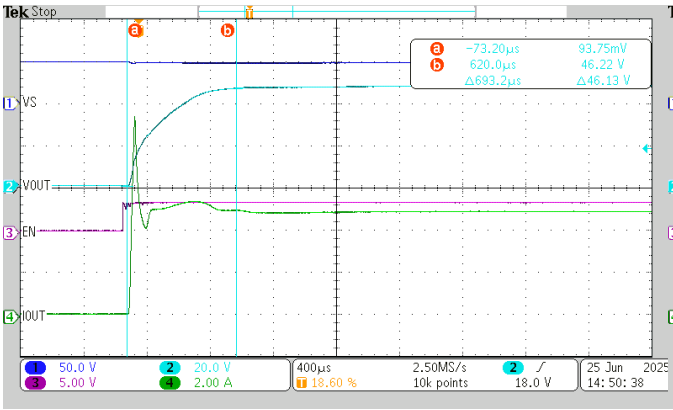


Figure 5-65. Test Condition 65

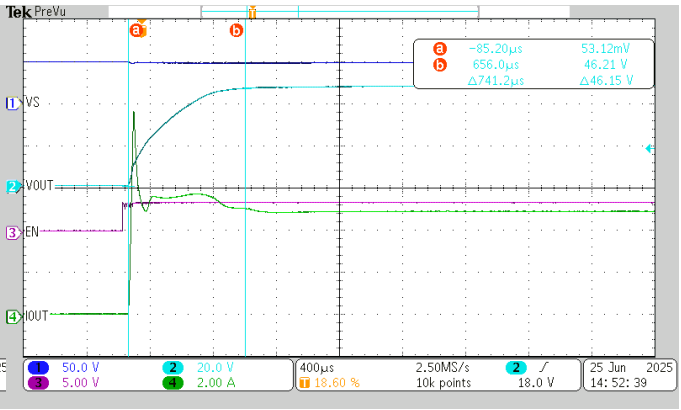


Figure 5-66. Test Condition 66

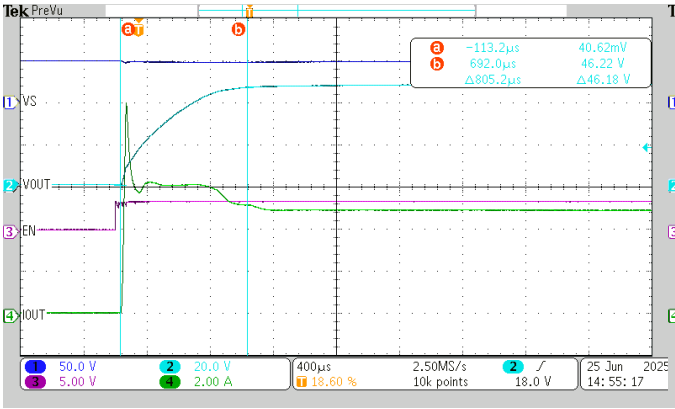


Figure 5-67. Test Condition 67

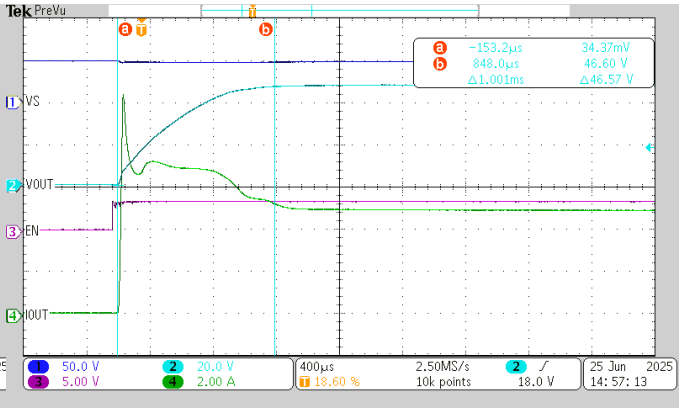


Figure 5-68. Test Condition 68

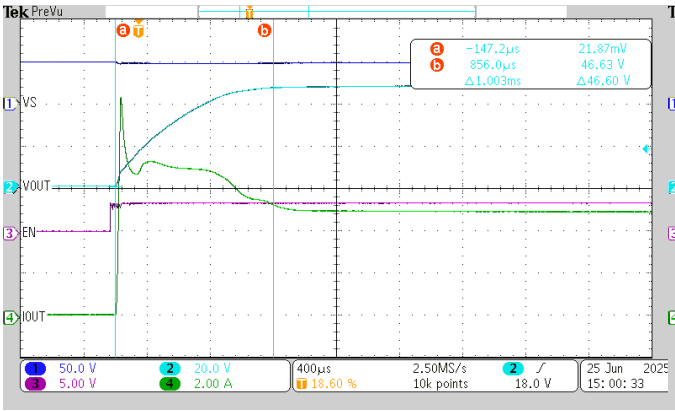


Figure 5-69. Test Condition 69

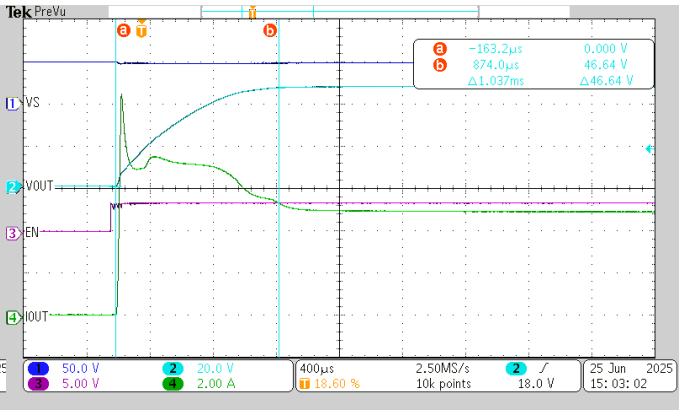


Figure 5-70. Test Condition 70

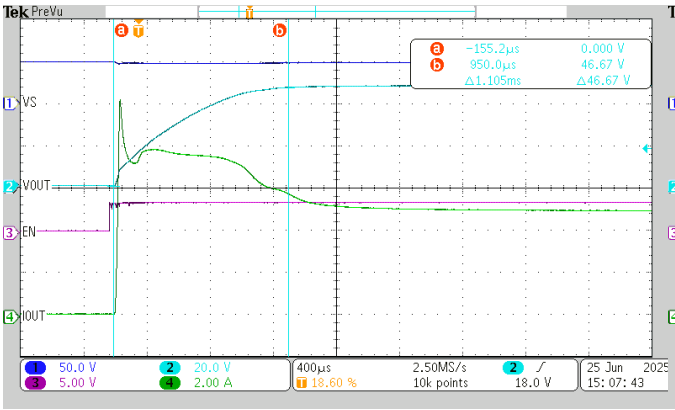


Figure 5-71. Test Condition 71

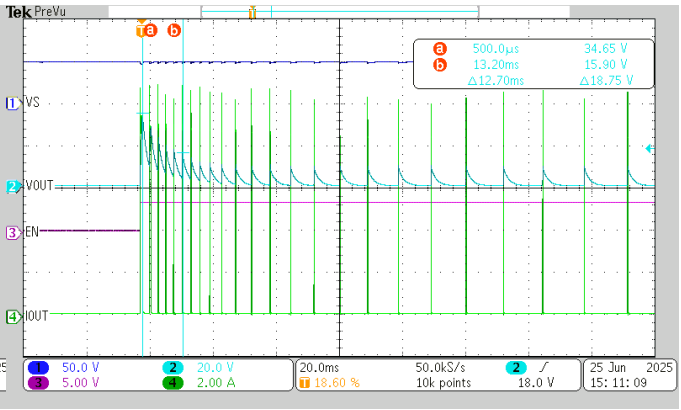


Figure 5-72. Test Condition 72

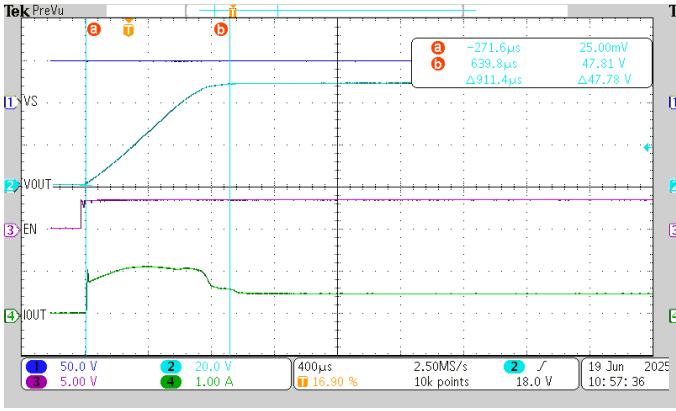


Figure 5-73. Test Condition 73

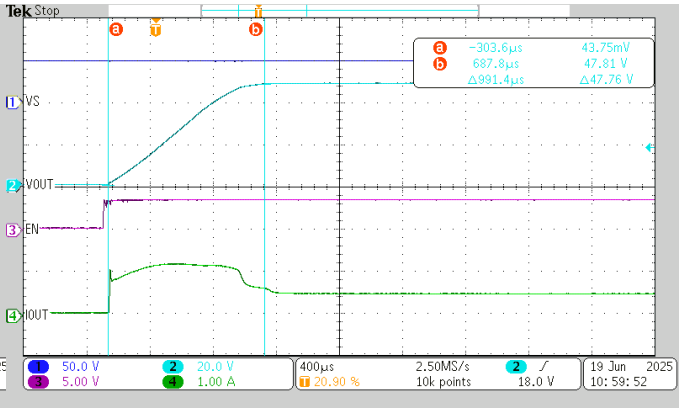
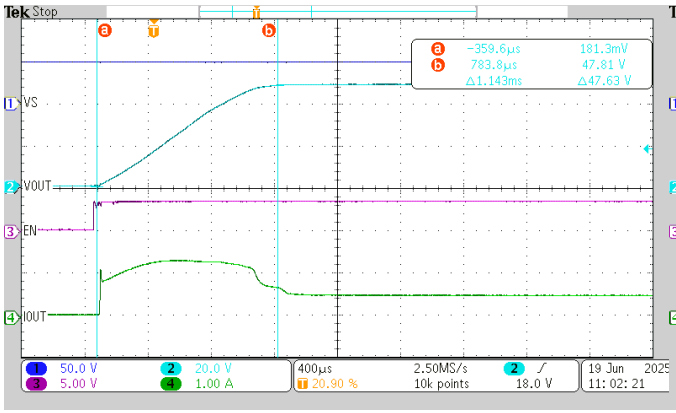


Figure 5-74. Test Condition 74



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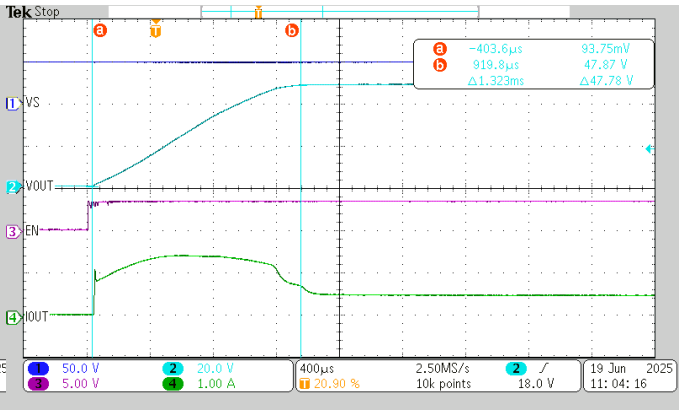

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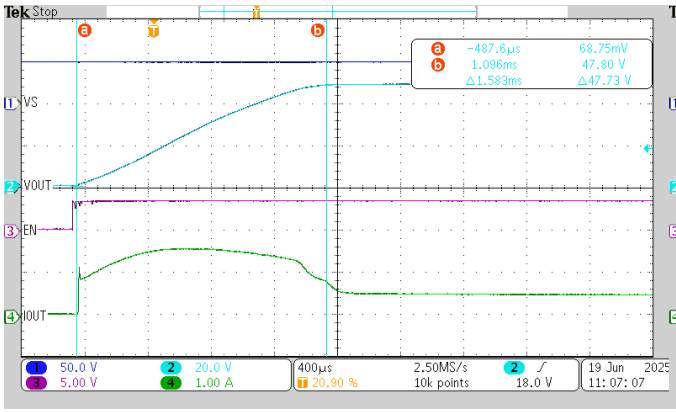

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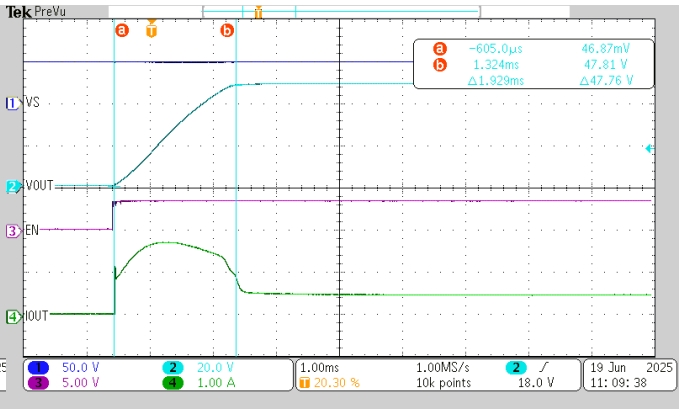

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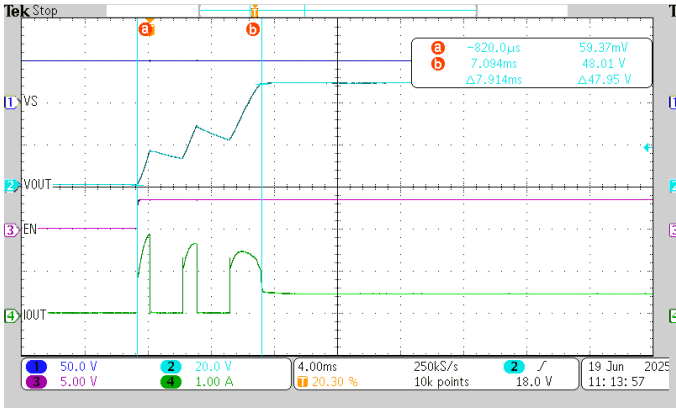

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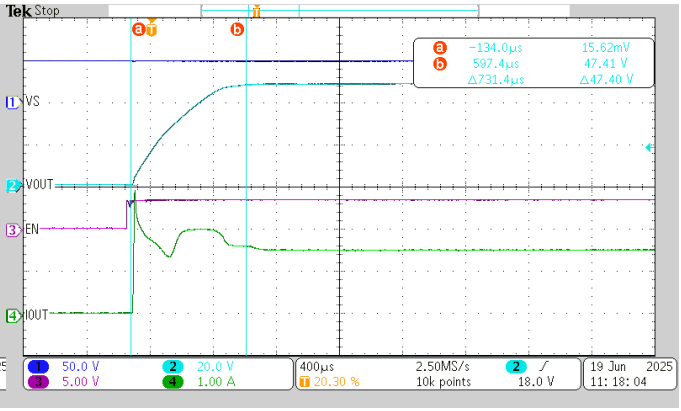

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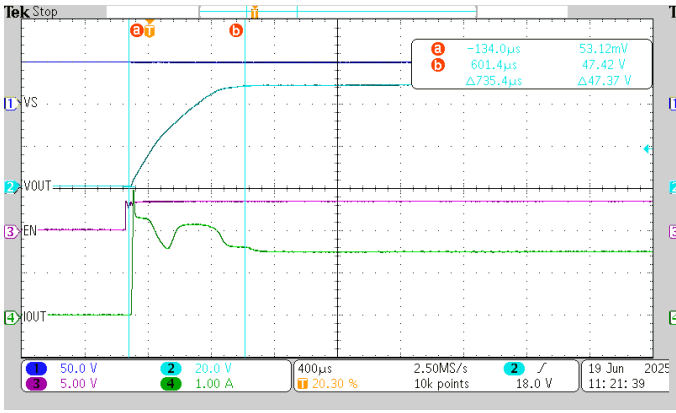

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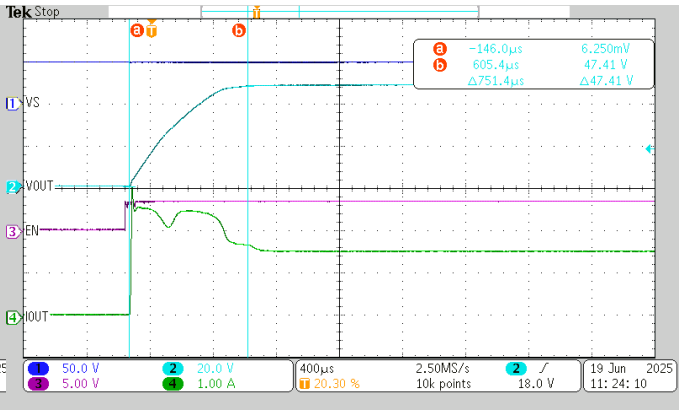

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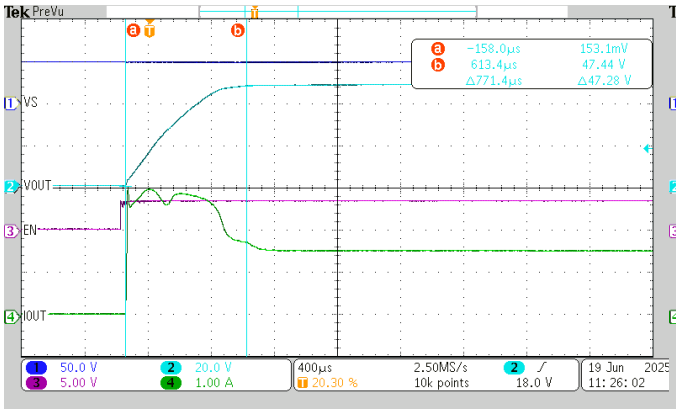

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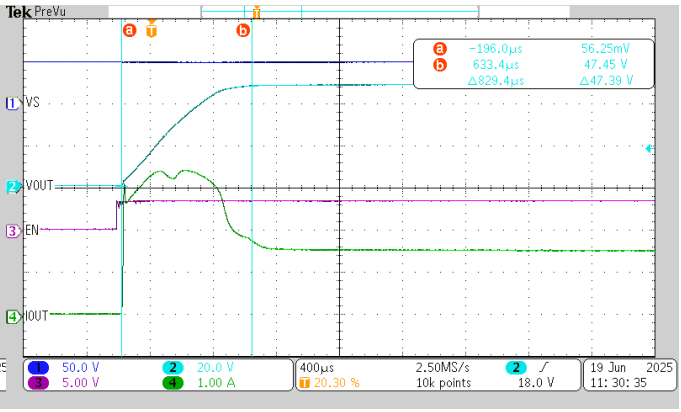

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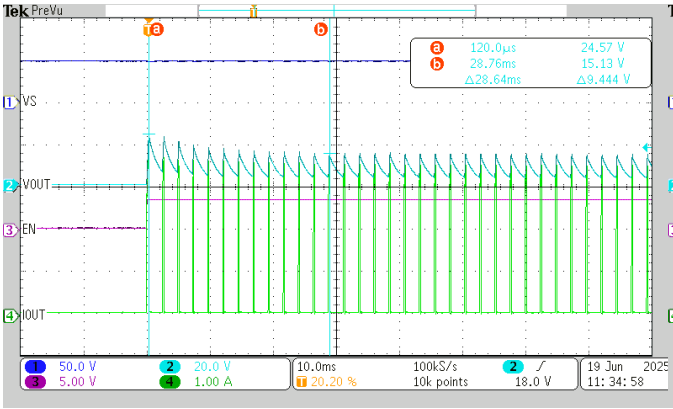

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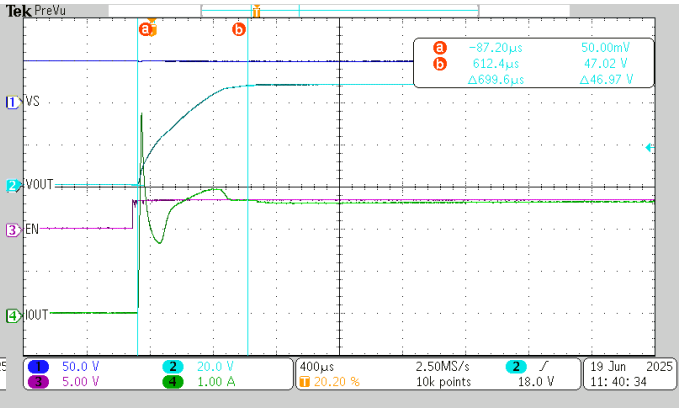

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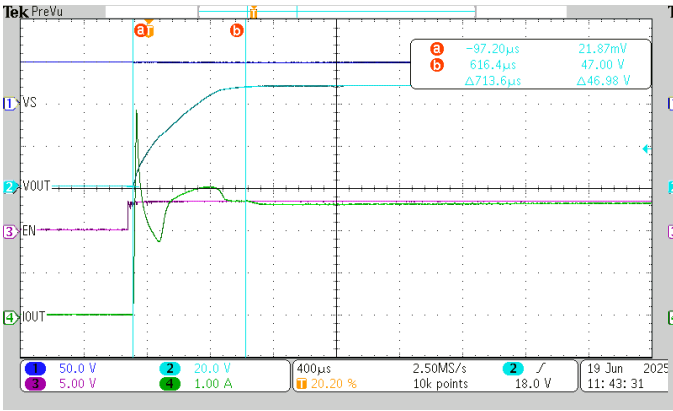

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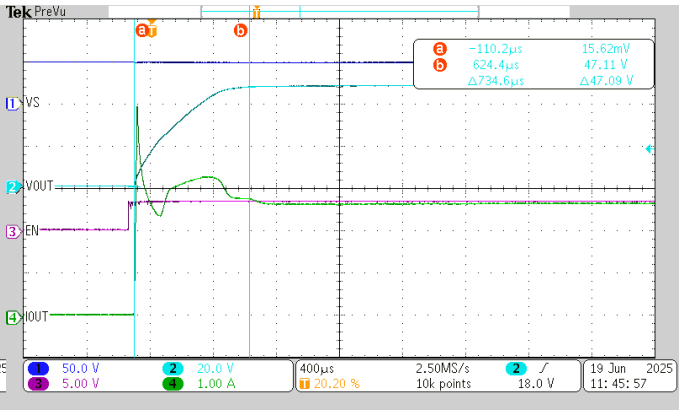

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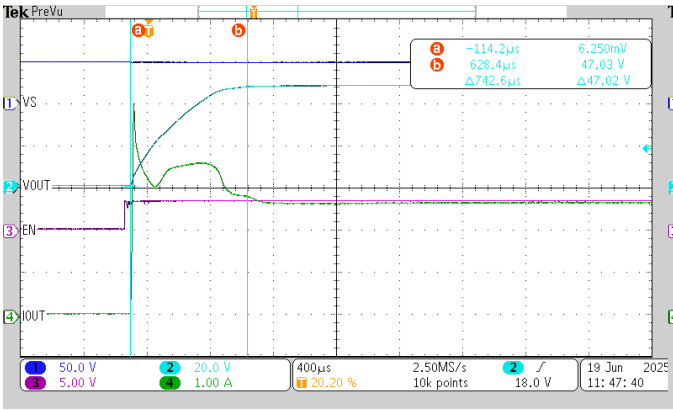

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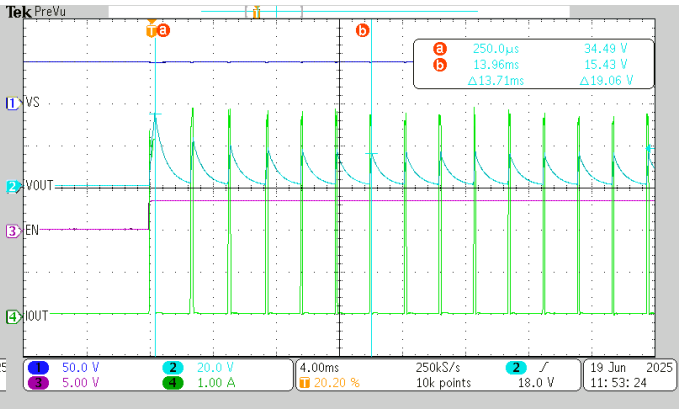

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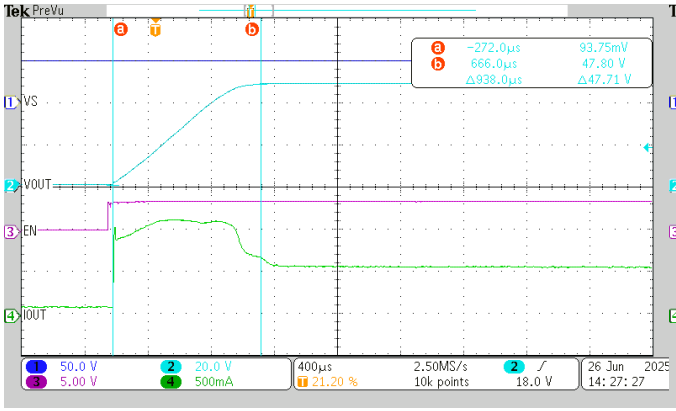

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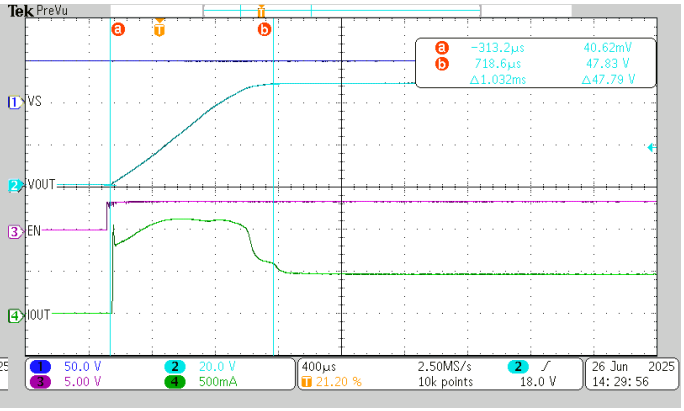

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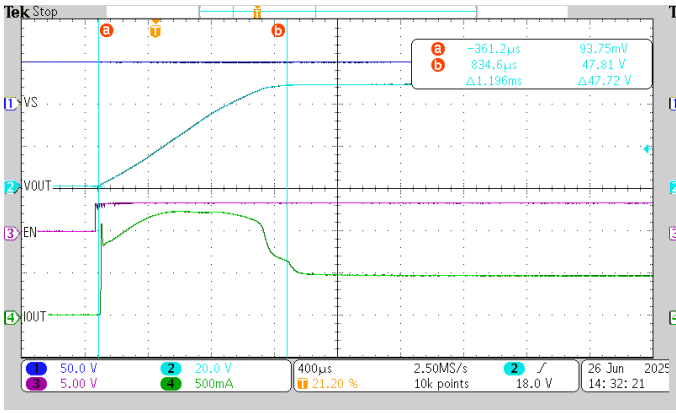

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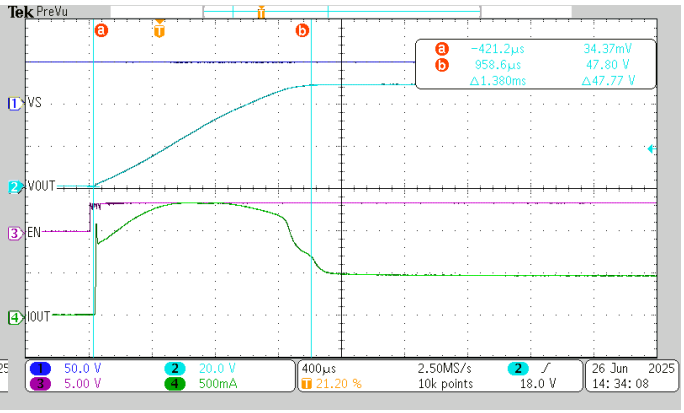

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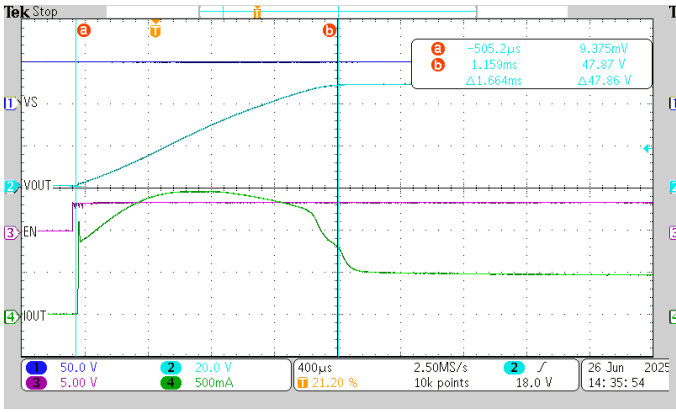

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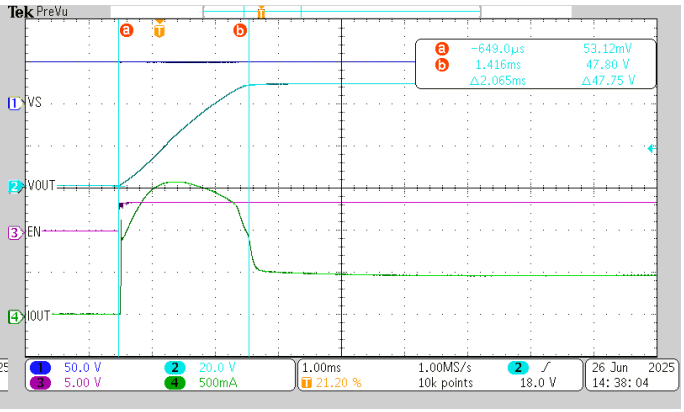

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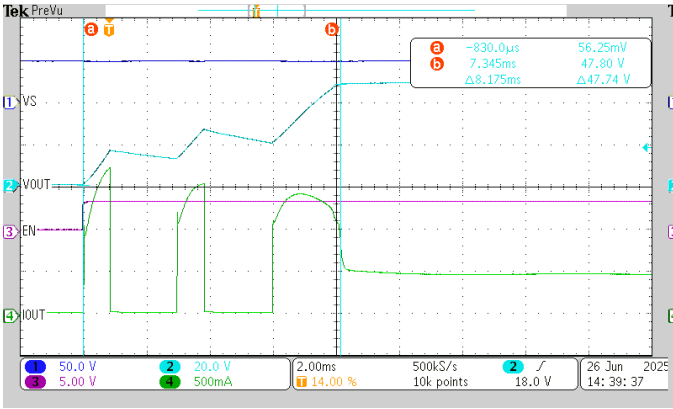

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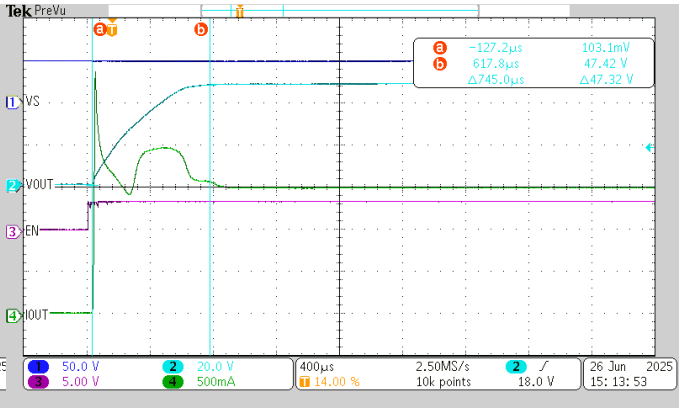

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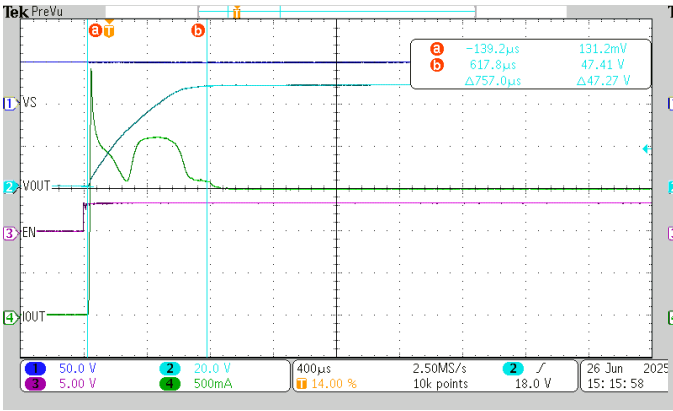

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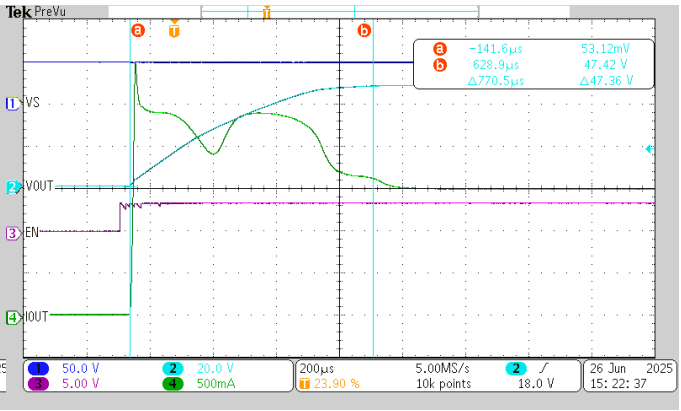

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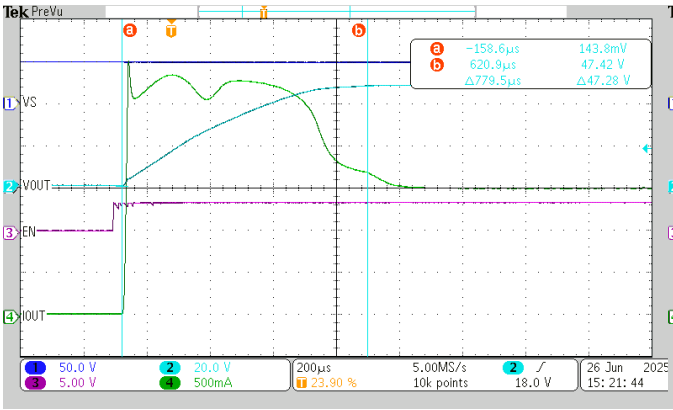

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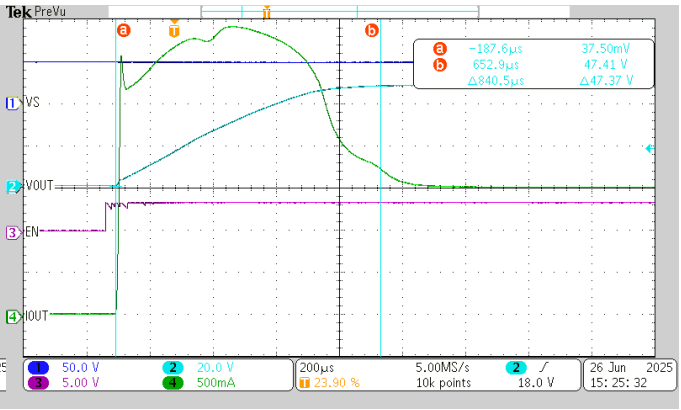

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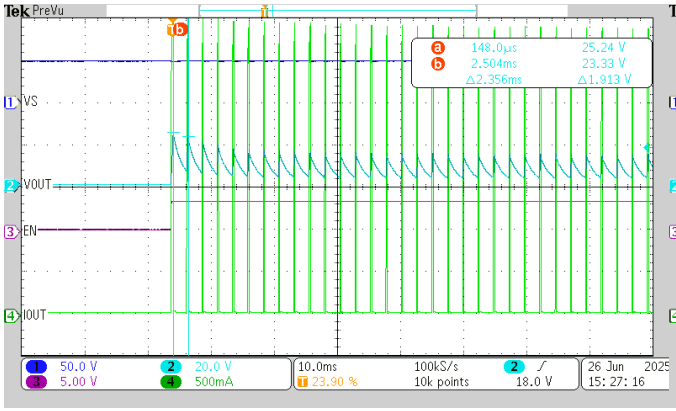

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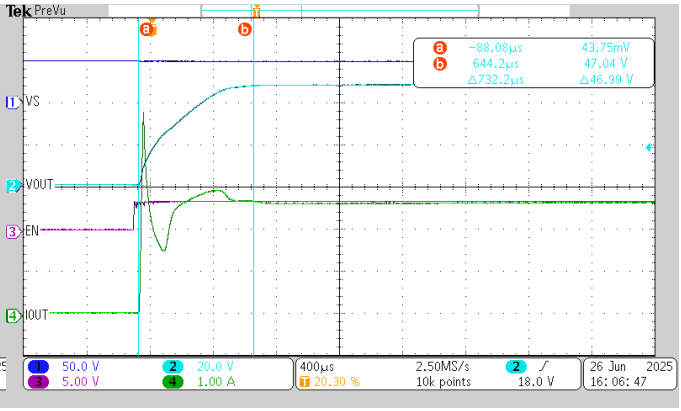

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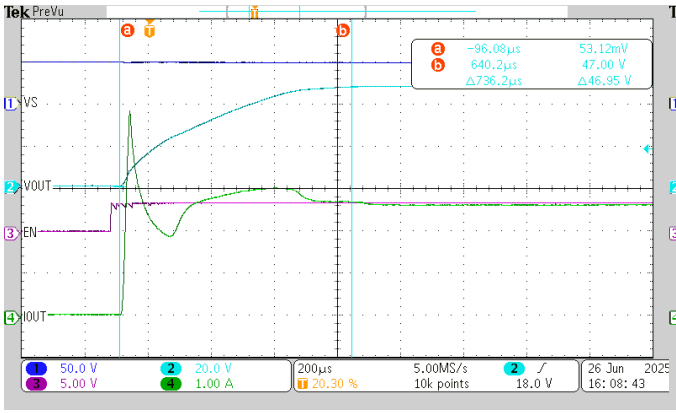

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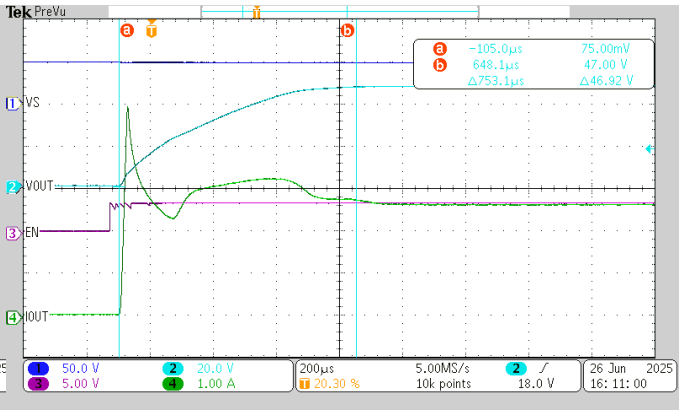

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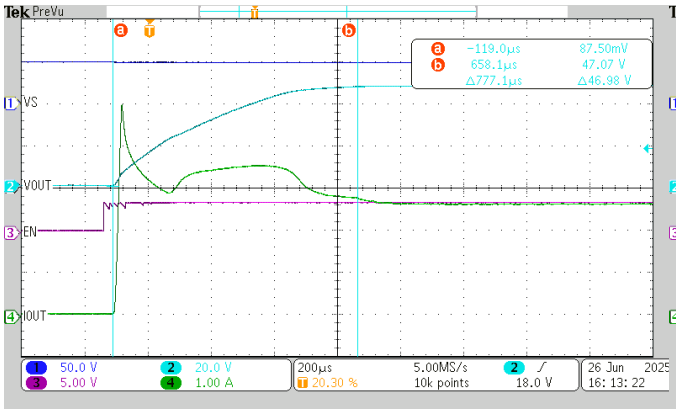

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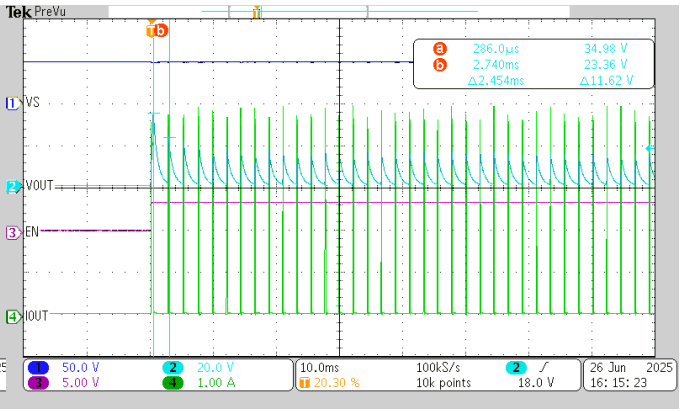

Figure 5-108. Test Condition 108

6 Summary

Powering capacitive loads is a common application where TI's smart HSSs are used. The main obstacle when driving this type of load is the resulting inrush current. TI's switches include current limit and thermal protection features to help suppress large inrush currents and create a more reliable system. The current limit threshold and junction temperature can affect the ability of the switch to charge a capacitor. By setting low current limits and at lower temperatures, the amount of capacitance the HSS can successfully charge increases.

7 References

- Texas Instruments, How To Drive Resistive, Inductive, Capacitive, and Lighting Loads, application note
- Texas Instruments, Adjustable Current Limit of Smart Power Switches, application note
- Texas Instruments, TPS1HTC30-Q1, 30mΩ, 6A Single-Channel Automotive Smart High-Side Switch, data sheet
- Texas Instruments, TPS1HTC30-Q1 Evaluation Module, EVM user's guide
- Texas Instruments, TPS1HTC100-Q1 , 83mΩ , 4A Single-Channel Automotive Smart High-Side Switch, data sheet
- Texas Instruments, TPS1HTC100-Q1 Evaluation Module, EVM user's guide
- Texas Instruments, (+) [FAQ] Why does my e-load cause my high side switch to shut down? - Power management forum - Power management - TI E2E support forums

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