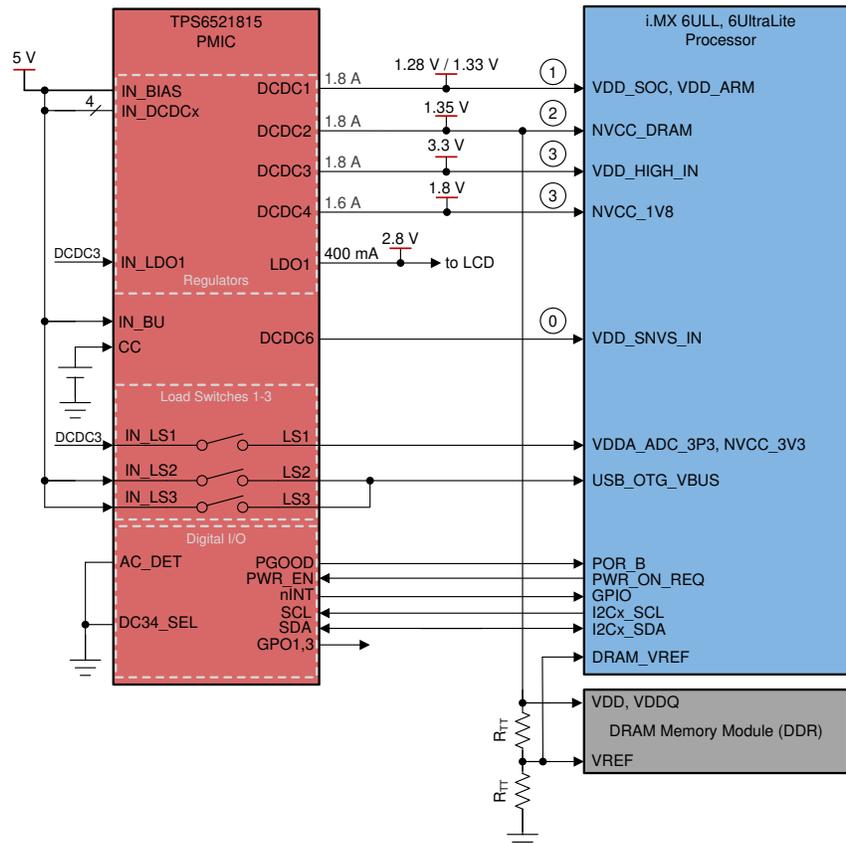


# Powering the NXP i.MX 6ULL, 6UltraLite with the TPS6521815 PMIC



## System Power Block Diagram



### Can you change PMICs?

Using a multi-rail power management IC (PMIC) for an applications processor is common, but typically the vendor recommends the PMIC that should be used for each processor. Even if the suggested PMIC is not ideal for the needs of the processor, often the complexity makes it difficult to swap out the PMIC for another solution. The purpose of this tech note is to show that the TPS6521815 PMIC can provide power for the i.MX 6ULL and 6UltraLite processors.

### Why the TPS6521815?

The TPS6521815 device has an input range from 2.7 to 5.5 V, making it appropriate for system-on-module applications powered from a 3.3-V or 5-V DC supply or a Li-Ion battery. The device has four step-down converters that provide the following: 1.28-V power rail with DVS required for the ARM® and SoC cores, 1.35-V (or 1.5-V) rail required for DDR3L (or DDR3)

memory, 1.8-V and 3.3-V rails required for I/Os. A low-dropout (LDO) regulator provides 2.8-V for LCD screen I/O. The TPS6521815 automatically sequences these rails in the correct power-up sequence for the i.MX 6ULL and 6UltraLite processors.

### How do you make the switch?

The TPS6521815 output voltages and sequencing order are determined by an EEPROM-backed register map, which can be programmed using the [BOOSTXL-TPS65218](#) socketed booster pack. Samples of the TPS6521815RSLR can be programmed during the prototype phase of product development and soldered down on the [TPS65218EVM-100](#) or the prototype PCB of the final product to evaluate the performance of the PMIC. To order pre-programmed samples of the TPS6521815RSLR for the NXP i.MX 6ULL, 6UltraLite processor that match this tech note, [contact the programming services](#) organization at ARROW.

**Table 1. i.MX 6ULL and 6UltraLite Power Requirements**

TPS6521815				i.MX 6ULL/6UltraLite		
POWER-UP SEQUENCE	POWER SUPPLY (OUTPUT)	OUTPUT CURRENT [mA]	OUTPUT VOLTAGE [V]	POWER SUPPLY (INPUT)	VOLTAGE RATING [V]	MAX CURRENT <sup>(1)</sup> [mA]
1	DCDC1	1800	1.28 / 1.33 <sup>(2)</sup>	VDD_SOC_IN (for VDD_SOC, VDD_ARM)	Minimum: 1.275 / 1.325 Maximum: 1.5	500
2	DCDC2	1800	1.35 (or 1.5)	NVCC_DRAM	Minimum: 1.283 Typical: 1.35 Maximum: 1.45	124 – 291
3	DCDC3	1800	3.3	VDD_HIGH_IN <sup>(3)</sup>	Minimum: 2.8 Maximum: 3.6	125
3	DCDC4	1600	1.8	NVCC_1V8	Minimum: 1.65 Maximum: 3.6	Maximum IO current
5	LDO1	400	2.8	LCD screen (IOVDD)	Minimum: 1.65 Maximum: 3.3	15
0	DCDC6 <sup>(4)</sup>	25	2.5	VDD_SNVS_IN	Minimum: 2.4 Maximum: 3.6	0.5
4	LS1	350	3.3	VDDA_ADC_3P3, NVCC_3V3	Minimum: 3.0 Maximum: 3.6	35 + Maximum IO current
N/A	LS2, LS3	920, 900	5	USB_OTGx_VBUS	Minimum: 4.4 Maximum: 5.5	50 each + USB device current

- (1) The maximum current for VDD\_SOC\_IN (VDD\_ARM and VDD\_SOC core rails) is from the *Maximum Supply Currents* table in the [i.MX6ULLIEC](#) and [i.MX6ULIEC](#) data sheets. Other maximum currents values are from the same source, from [AN5345](#) application note, or estimates including I/O calculation and peripheral current consumption.
- (2) This set-point is based on the use case where the LDO (which generates VDD\_ARM\_CAP and VDD\_SOC) is enabled. The voltage can be modified by the processor after power-on using I<sup>2</sup>C, a feature named dynamic voltage-frequency scaling (DVS or DVFS) such that VDD\_SOC\_IN is 125 mV greater than the LDO output set-point.
- (3) LDO\_2P5 and LDO\_1P1 internal LDO regulators are enabled to generate voltages for all NVCC power inputs not using 3.3 V or 1.8 V
- (4) DCDC6 has direct feedback to a reference of 1.8 V, allowing the use of a resistor divider to generate the correct voltage for VDD\_SNVS

**Table 2. Adjacent Tech Notes**

Processor	Title
i.MX 6Solo and 6DualLite	<a href="#">Powering the NXP i.MX 6Solo, 6DualLite Processor with the TPS6521815 PMIC</a>
i.MX 7Solo and 7Dual	<a href="#">Powering the NXP i.MX 7 Processor with the TPS6521815 PMIC</a>
i.MX 8M Mini and Nano	<a href="#">Powering the NXP i.MX 8M Mini and Nano with the TPS6521825 and LP873347 PMICs</a>

**References**

Texas Instruments, [TPS6521815 User-Programmable Power Management IC \(PMIC\) With 6 DC/DC Converters, 1 LDO, and 3 Load Switches Data Sheet](#)

Texas Instruments, [Power Supply Design for NXP i.MX 6 Using the TPS65023 Application Report](#), SLVA943, Feb. 2018

NXP Semiconductors, [i.MX 6ULL Applications Processors for Industrial Products Data Sheet](#) (i.MX6ULLIEC), Rev. 1.2, 11/2017

NXP Semiconductors, [i.MX6ULL Power Consumption Application Note Application Note](#) (AN5345), Rev. 2, 10/2017

**0.1 Trademarks**

ARM is a registered trademark of Arm Limited.  
All other trademarks are the property of their respective owners.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated