Application Report
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PCB Layout and Parameters Recommendation for TPS2583X EMC Performance

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ABSTRACT

The TPS2583X-Q1 device family integrates a buck converter inside, supports USB Type-C® and BC 1.2 protocols, and is widely used in automotive applications. Automotive product certification typically requires passing the CISPR25 EMC standard. This application report summarizes the kind of PCB layout and attained corresponding parameters which can improve the EMC performance according to the test results from a certified testing agency.

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1 Introduction

It is necessary to know the inner power loop design and the pinout of the TPS2583X family before designing the PCB layout shown in Figure 1. To understand the operating principle of the buck converter and how di/dt and dv/dt influences the operation of the buck converter can also help improve the EMC performance of the PCB layout shown in Figure 2. When placing the devices in the PCB layout, it is important that the larger devices are placed first in a higher priority and then followed by the smaller devices. Therefore, the power circuit layout is placed first and should then be followed by the signal circuit. In this application report, the results of the EMC test use the following conditions: CISPR25 Class5 conduction test Vin = 12 V, f = 400 kHz, Vout = 5.1 V ,Iout = 3 A.

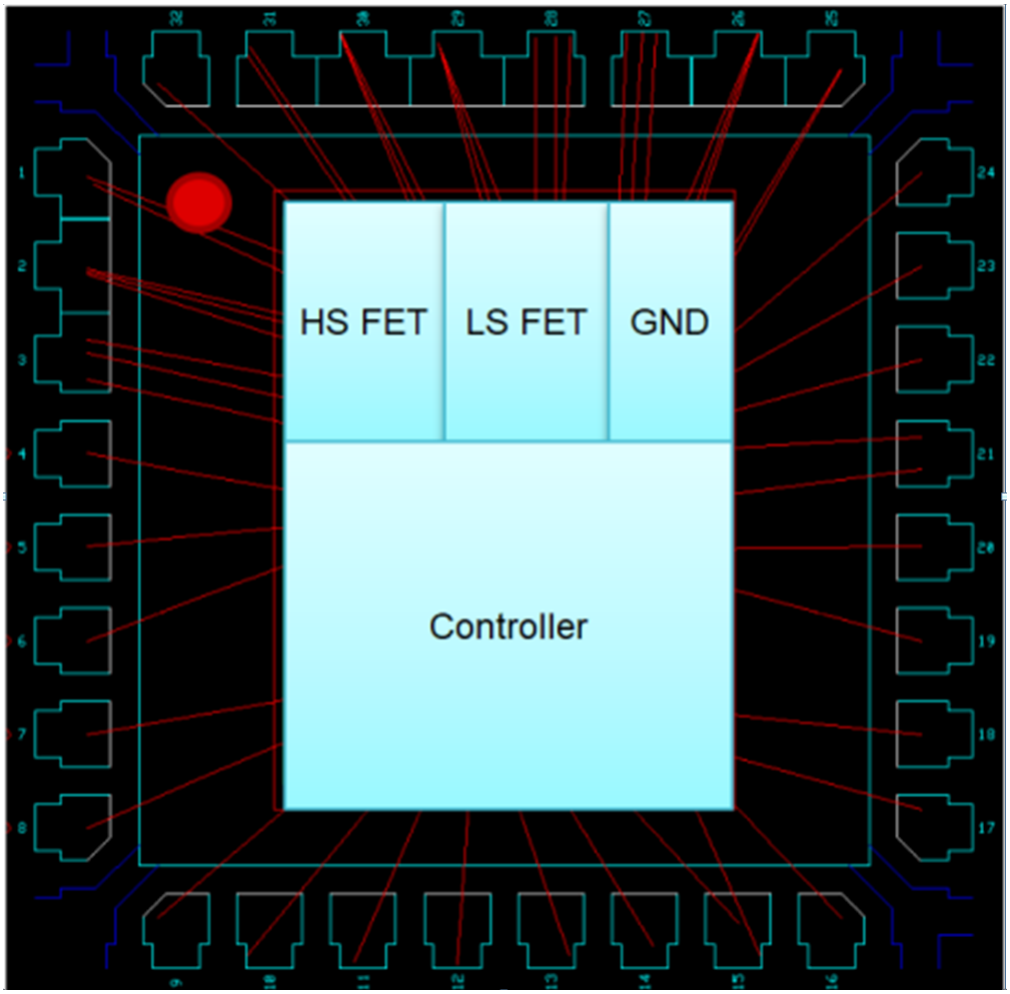

Figure 1. Inner Function Module and Pinout of the TPS2583X

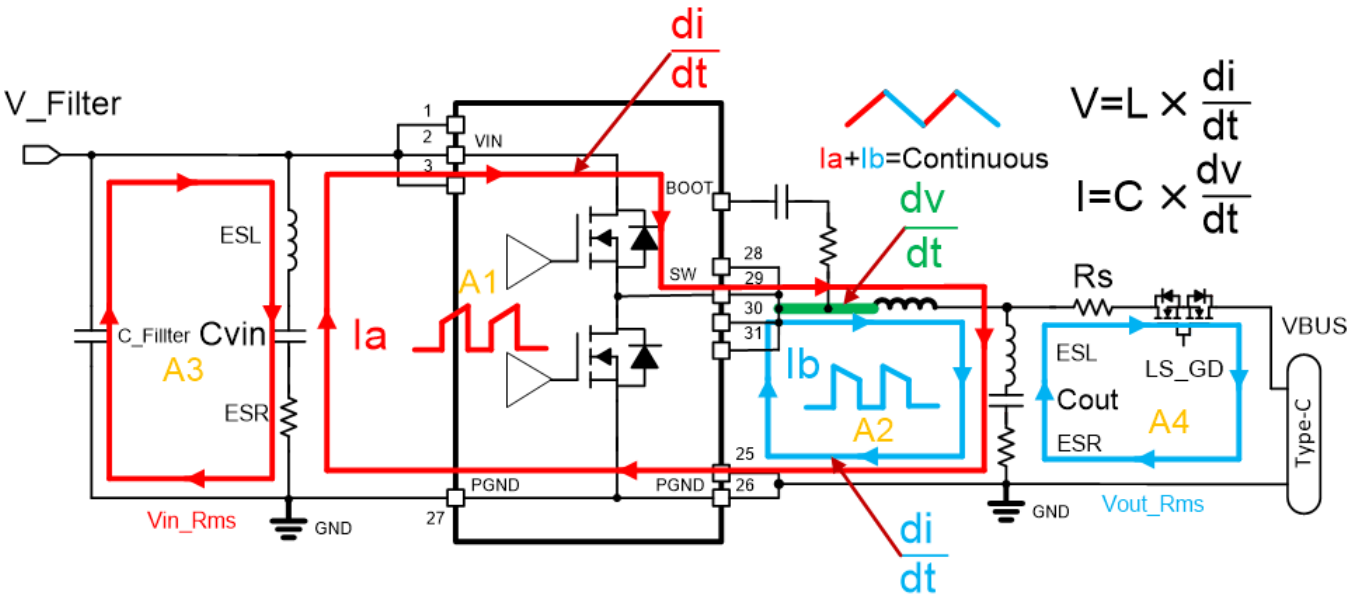

Figure 2. Topology of the Buck Converter and its Operating Principle

2 Input Filter and Input/Output Capacitor Recommendations for the TPS2583X

2.1 LISN Unit

The TPS2583X-Q1 family is designed for automotive applications, which simultaneously supports USB Type-C and BC1.2 protocol. The EMC test standard refers to CISPR25 Class5, and input LISN parameters refer to Figure 3 (LISN section). The parameters of the LISN section are standard parameters from a certificated testing agency.

2.2 FILTER Unit

The FILTER unit uses two-stage differential mode filtering. L1 is an 880?magnetic bead (SMD package), used to filter out high-frequency differential mode signals. L2 is a 1-µH inductor (SMD package), used to filter out line differential mode signals. It is better to choose shielded inductor or molded inductor. L1, C2, C3, and C4 can be deleted according to the test margin.

2.3 Power Unit

The DC/DC converter consists of three parts, which are the input capacitor, freewheeling inductor, and output capacitor.

Input capacitor: The input capacitor section consists of two 10-µF (C7, C8) capacitors, one 0.1-µF (C9) capacitor, and one 2.2-nF (C10) capacitor. C9 and C10 are vital to suppress high-frequency EMI. C9 (0.1 µF) has a good performance to suppress EMI above 40 MHz, and C10 (2.2 nF) can suppress EMI above 100 MHz. The value of C10 can be varied around 2.2 nF according to different PCB parasitic parameters.

Freewheeling inductor: An 8.2-µH inductor is recommended. The package size selection is made according to the size of the PCB, and it is better to choose the inductor with a smaller R_{DC} and smaller core loss. It is very important to reduce high-frequency radiation. To accomplish this, use shielded inductors or molded inductors for their better performance to reduce high-frequency radiation.

Output capacitor: The output capacitor section consists of three 22- µF (C11, C12, C13) capacitors and one 2.2-nF (C14) capacitor. C14 is used to suppress the EMI above 30 MHz, and the value of this capacitor can be chose from 1 nF to 100 nF, according to the test result.

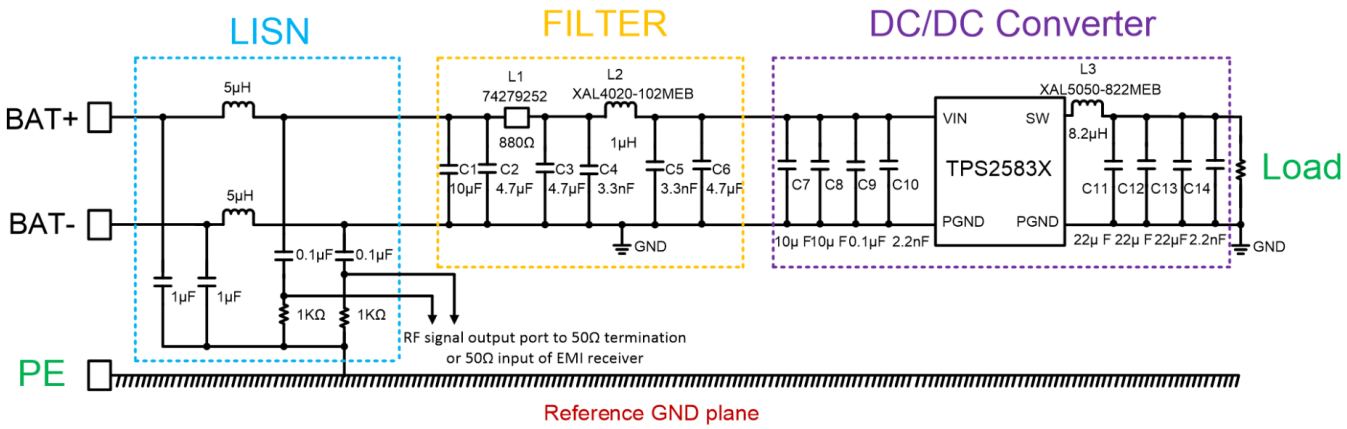

Figure 3. Recommended Parameters for Input Filter, Input Capacitor, Freewheeling Inductor, and Output Capacitor

3 Common TPS2583X PCB Layout and the Results of EMI Conduction Test

3.1 Common TPS2583X PCB layout

As Figure 4 shows, the green box represents the input capacitor section, the yellow box represents the freewheeling inductor, and the blue box represents the output capacitor.

Point A is the VIN+ port of input capacitor. Usually the high-frequency filtering capacitor with small-capacity is set close to the chip, and the two input capacitors with large-capacity are far away from the chip.

Point B is the connecting point of the inductor and pin SW. Usually the inductor is placed vertically, L-shaped or T-shaped copper, which results in a right angle. A right angle will cause a sudden change of the impedance, which will further cause signal reflection. It will impact the EMC performance of the PCB.

Point C is the ground of the output capacitor. As the arrow shows, the ground of the output capacitor is far away from pin PGND of the TPS2583X device.

Point D is the ground of the input capacitor. As the arrow shows, the ground of the input capacitor is far away from pin PGND of the TPS2583X device.

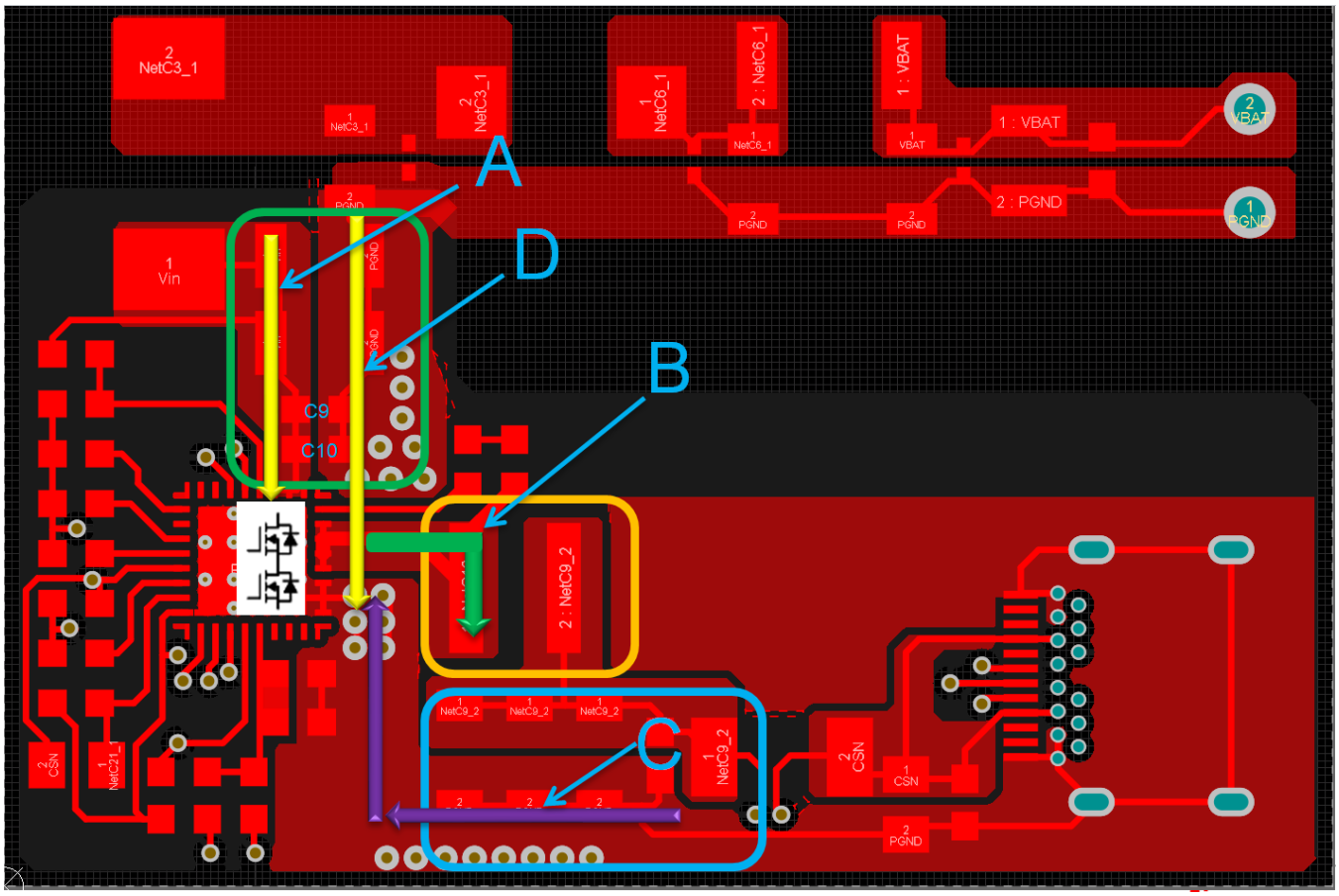

Figure 4. Common TPS2583X PCB Layout

3.2 EMC Conduction Test Result of Common TPS2583X PCB Layout

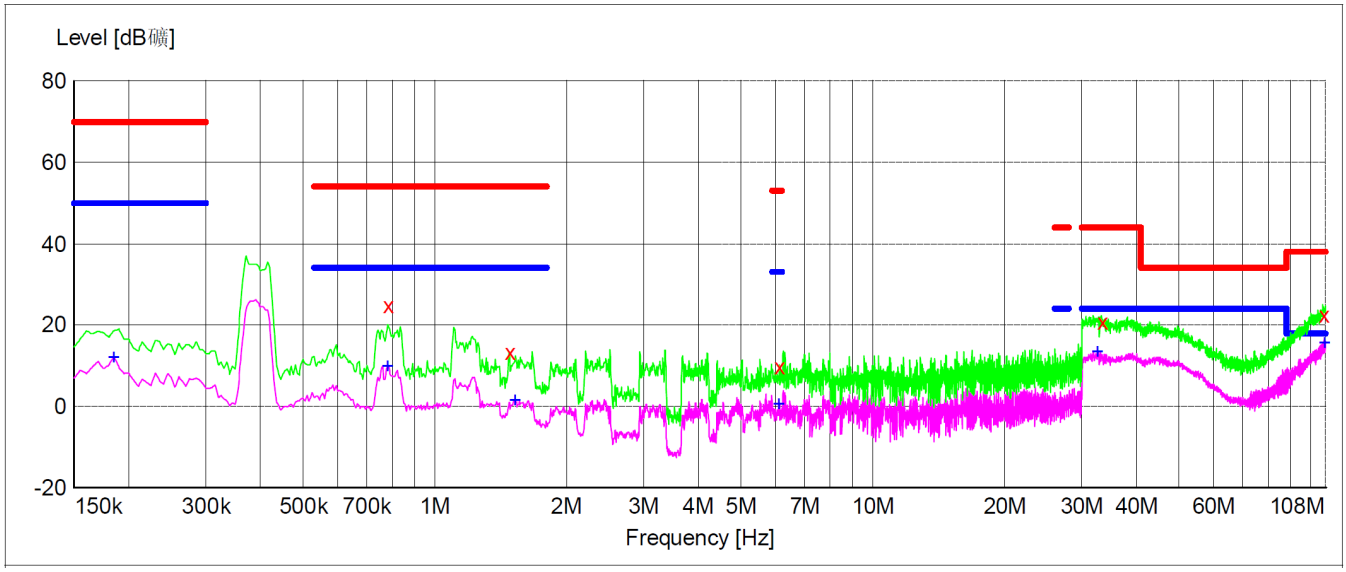

Figure 5. EMC Construction Test Result of Common TPS2583X PCB Layout

4 Single-Sided Device Placement, Multi-Layer PCB Layout Applications

To reduce costs or meet the process requirements, customers may choose single-sided device placement with multi-layer PCB layout. This kind of layout needs to take the distance from the input filter to output into consideration. For details, see Section 4.1.

4.1 Application of Input Filter PCB Layout

The TPS2583X devices use single-sided device placement with multi-layer PCB layout application, see Figure 6. This kind of layout should keep an abundant distance between the input filter and output. The distance indicated by the yellow arrow in Figure 6 cannot be less than 15 mm (experience value for TPS2583X). The larger the output power, the longer the distance, to prevent the high-frequency signals of the input/output power circuit (B Region) from coupling into the input filter circuit (A Region) causing the failure of the input filter. Also, the copper of the ground of the input filter (A Region) and the copper of the ground of the input/output power circuit (B Region) should be removed thoroughly. The ground line finally converges at point C after the filter, and is connected to the ground line of the input/output power circuit.

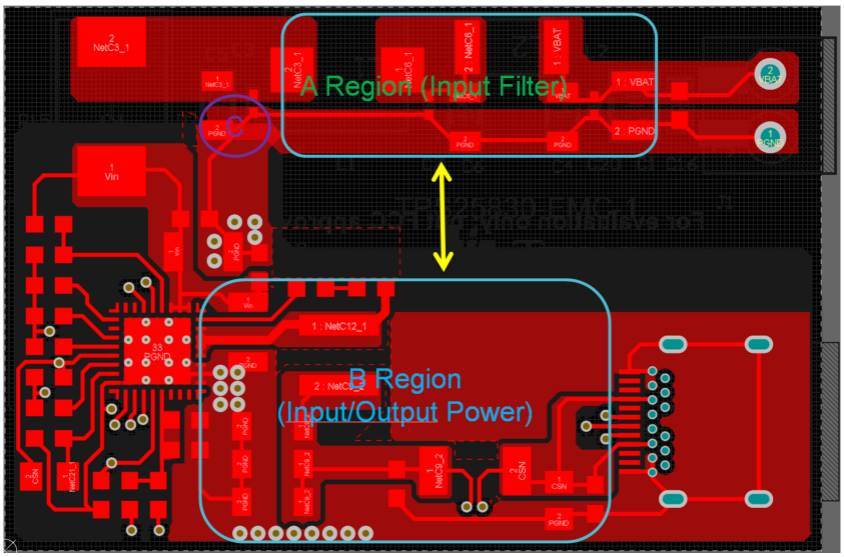

Figure 6. Single-Sided Device Placement, Multi-Layer PCB Layout

4.2 Application of DC/DC Power Loop PCB Layout

Figure 7 shows the DC/DC converter schematic of the TPS2583X device. The red box with the arrow indicates the loop current Ia and the blue box with arrow indicates the loop current Ib. Ia and Ib have a large current change rate (di/dt), especially the area shaded with the red slash. Thus, the area should be as small as possible when designing PCB layout.

As Figure 8 shows, in the actual PCB layout, make the power loop area as small as possible. The BOOT loop should also be as small as possible.

As Figure 7 and Figure 8 show, line A, line B, line C, and line D should be as short as possible. Line A and line D should follow this principle more strictly, because these two lines have the largest current change rate (di/dt) in the whole circuit. So line A and line D should be short and wide enough to reduce the parasitic inductance of the PCB. Importantly, the VIN+ port of the input capacitor should be as close as possible to the pinout of the TPS2583X device, as well as meet the processing requirements. Additionally, one input capacitor should be close to the TPS2583X device, and the other is connected across SW to ensure the shortest path between VIN and PGND.

Point B has the biggest voltage change range (dv/dt) in the whole loop. Therefore, under the premise of meeting the heat dissipation and current carrying capacity, the area of copper clad should be as small as possible to reduce the parasitic capacity of the PCB. It is very important not to punch copper through the entire wiring of the SW. All signal lines and susceptible components should not pass under the SW traces or inductor, which is to avoid the oscillation caused by a high-frequency switch signal coupling to signal lines or vulnerable devices through the parasitic capacity of the PCB.

The ground of point C and point D is also crucial. The PCB layout of the ground of point C and point D cannot be neglected. Its area of the copper should be as short and wide as possible.

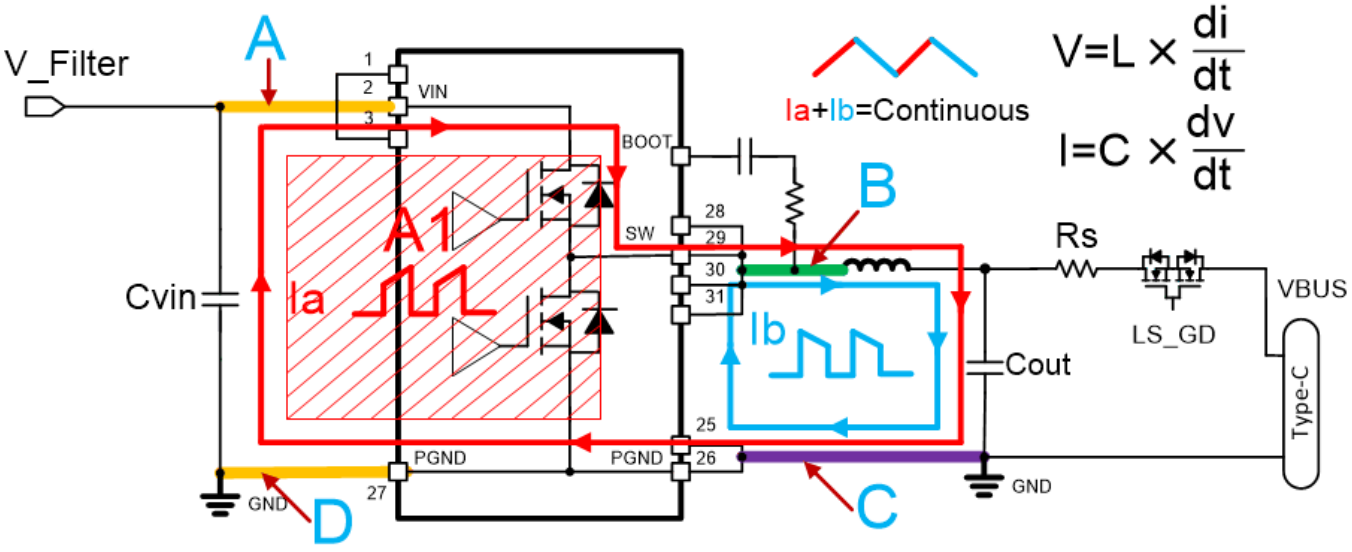

Figure 7. Buck Converter Schematic

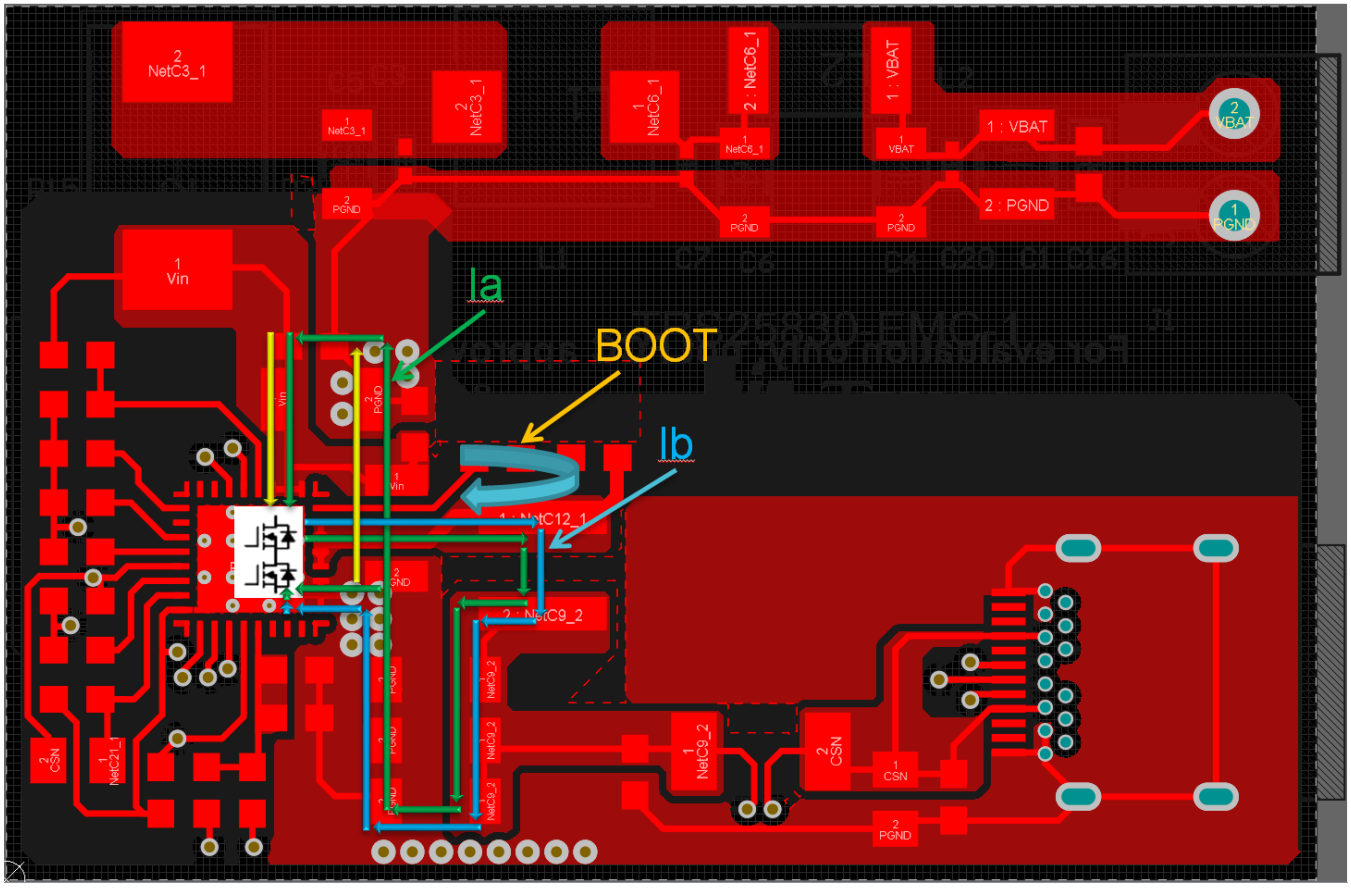

Figure 8. TPS2583X PCB Layout

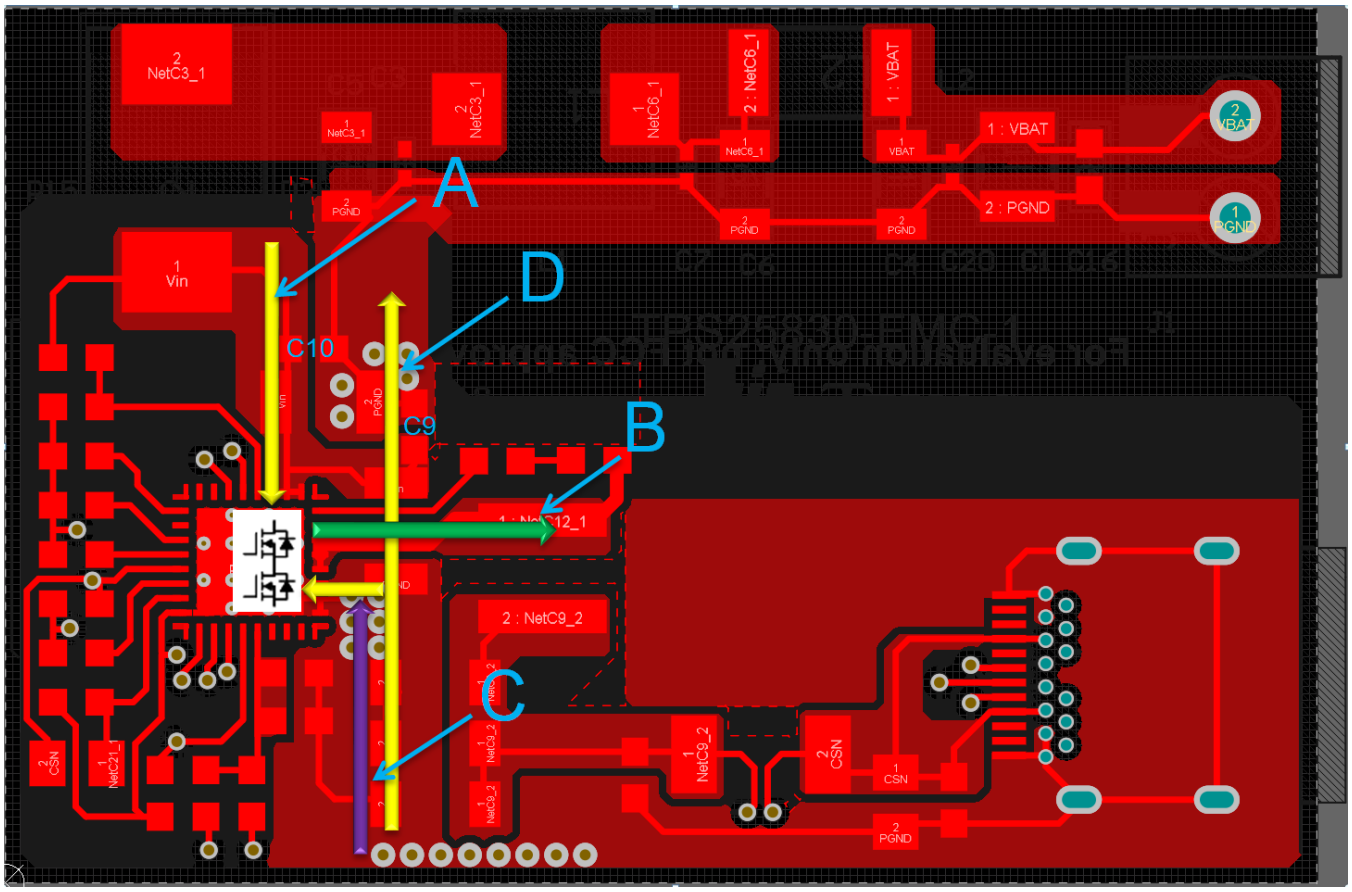

Figure 9. Power Loop of the PCB Layout for the TPS2583X

4.3 Application of Four-Layer PCB Layout

In addition to the previous two points on the PCB layout EMC, the PCB layer distribution also has a very large impact on EMC. The arrangement of the PCB layer directly affects the test results PCB. It is recommended that the top layer and the bottom layer are the main parts of power lines and signal lines, and the second layer do not need any line to prevent a complete PGND. The rest of power and signal lines are place in the third layer. Keep the bottom layer as complete as possible. As for the TPS2583X device, in reality, the grounds are separated into two kinds of ground which are power ground and signal ground in the actual PCB layout.

The top-layer PCB layout (Figure 9)**:** Placing large devices above the 0805 package on the top layer as much as possible helps improve PCB processing efficiency and cost. Additionally, some terminal blocks and control chips are placed on the top layer as much as possible. The layout principle, “the larger devices go first and the smaller follow; power circuits go first and signal circuits follow”, was mentioned in the *Introduction*. Finally, CSN and CSP current and voltage sampling resistor capacitors, RT resistors, IMON resistors, ILIM resistors, PIN capacitors for BUS, PIN resistors and capacitors for BOOT, and filter capacitors for VCC should be placed on the top layer as close to the chip PIN as possible.

The second layer PCB layout (Figure 10)**:** To ensure a complete PGND, this layer does not need any line, which shields the high- frequency signals caused by di/dt and dv/dt from high-level power loop, to reduce interference and coupling between the third layer and the bottom layer.

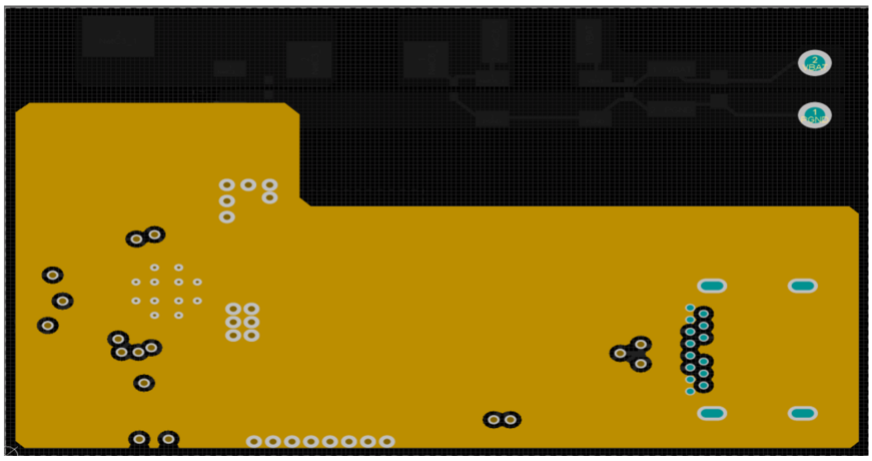

Figure 10. Second Layer of the PCB Layout for the TPS2583X

The third layer PCB layout (Figure 11)**:** Except for the first layer of signal lines, as much as possible, place the rest on the third layer. If the conditions allow, try to ensure that the power ground (PGND) is completely in the red wire box. Use PGND to shield the SW traces below the inductor.

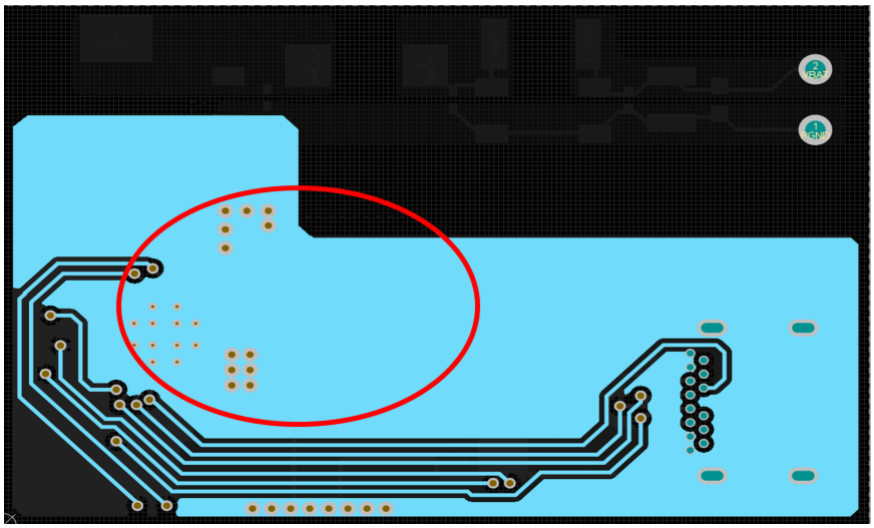

Figure 11. Third Layer of the PCB Layout for the TPS2583X

The bottom layer PCB layout (Figure 12)**:** If the top layer and the third layer cannot meet the requirements of signal lines and the bottom layer must be used to arrange signal lines, try to ensure that the power ground PGND is completely in the red wire box. Use PGND to shield the SW traces below the inductor.

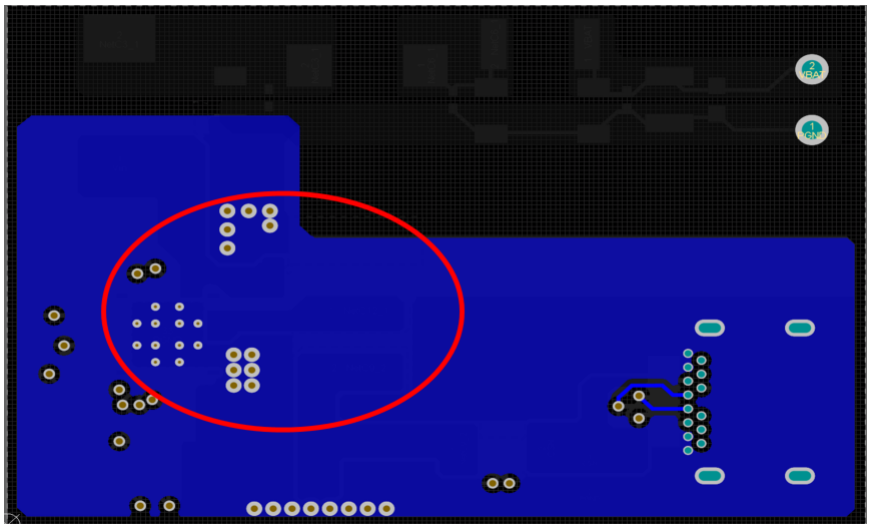

Figure 12. Bottom Layer of the PCB Layout for the TPS2583X

4.4 Application of PGND and AGND

The signal ground AGND and the power ground PGND need to be separated in the actual PCB layout to reduce the power ground PGND causing fluctuations to interfere with the signal ground AGND and causing oscillation.

PGND includes: the ground of the input capacitor, output capacitor, VCC capacitor, input port, output port, and so forth.

AGND includes: the ground of RT, IMON, ILMIT, CC1, CC2, FAULT, LD_DET, POL, CTRL1/2, DP, DM resistors, capacitors and ground lines.

As Figure 13 shows, the red highlight lines of PCB are the common connecting point of the grounds of all signal lines. PGND and signal ground AGND finally converge to the pin 16, and AGND is connected to the thermal pad. (As shown in the blue circle in Figure 13). The chip thermal pad serves as the common connection point for all ground wires. The power ground (PGND) or the input and output capacitor is as close as possible to the chip PGND pins: 25, pin 26, pin 27.

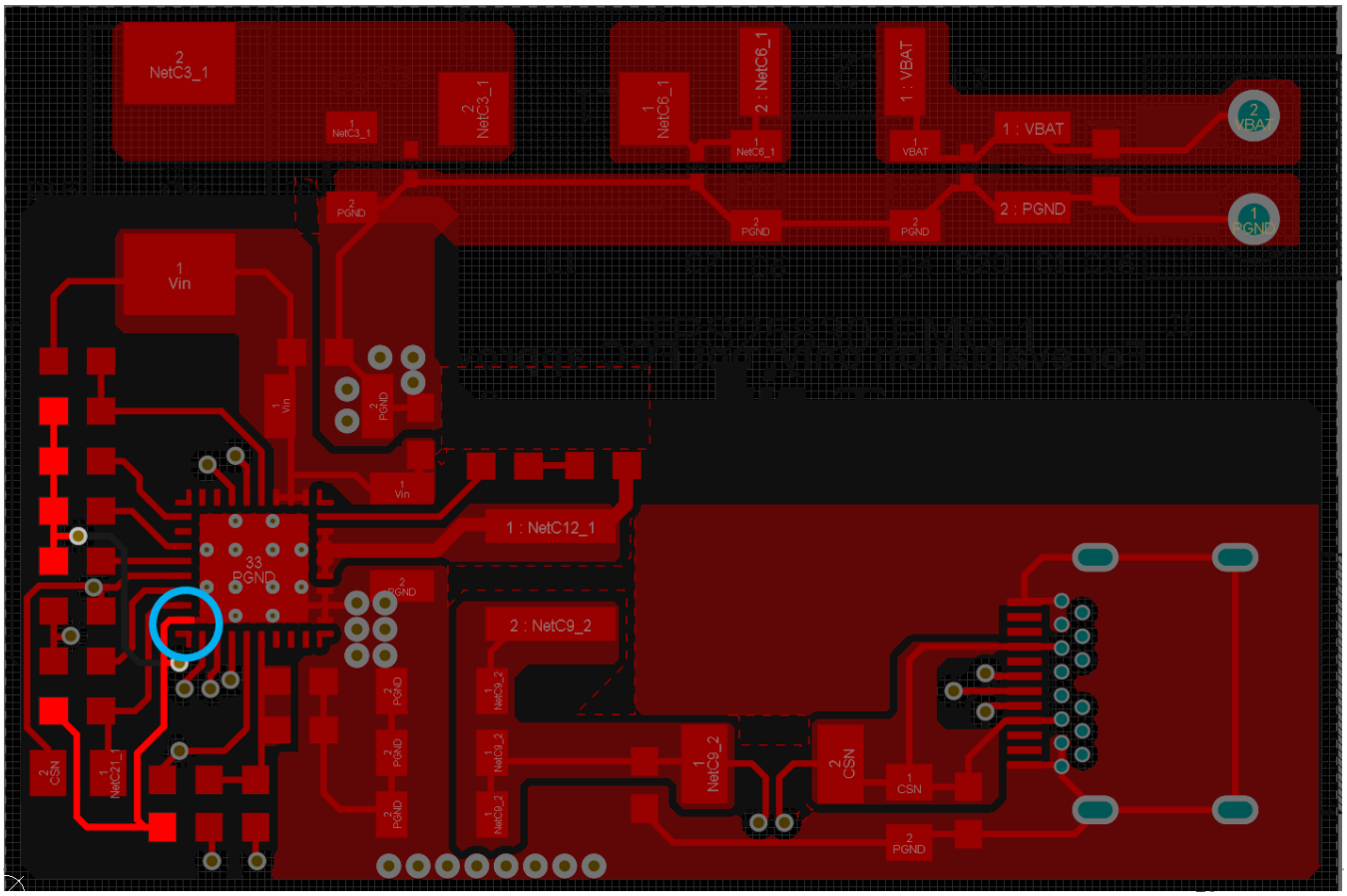

Figure 13. Bottom Layer of PCB Layout for TPS2583X

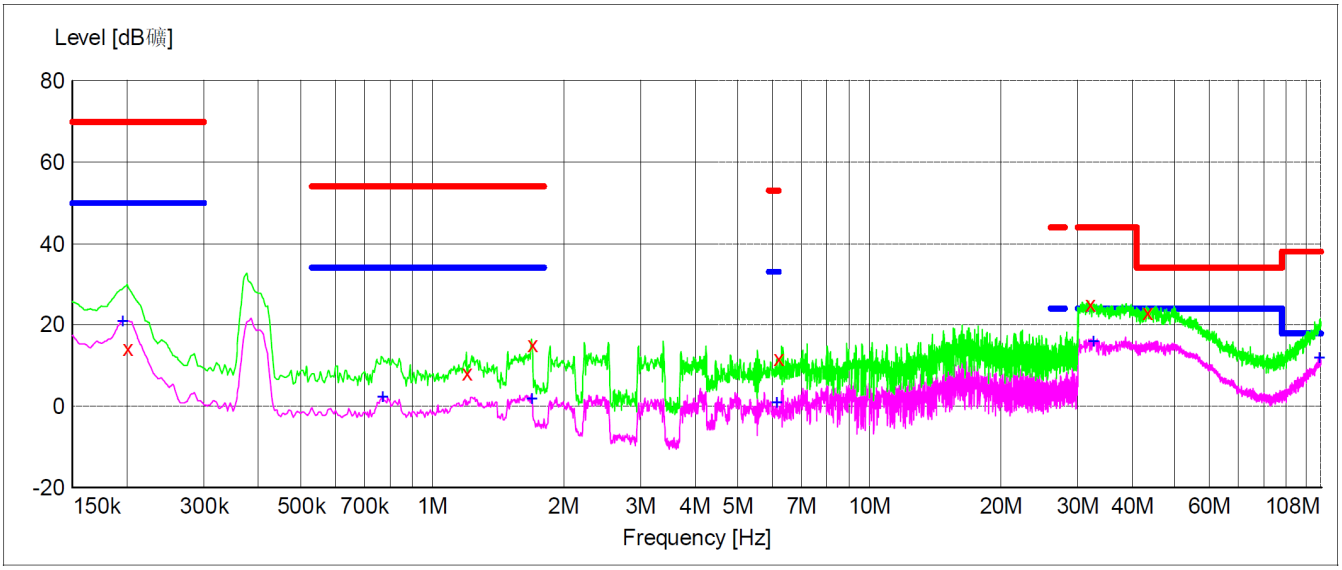

Figure 14. EMC Conduction Test Result When the Device is Placed on One Side

5 Double-Sided Device Placement, Multi-Layer PCB Layout Applications

Sometimes customers use double-sided device placement to reduce costs and PCB size. Therefore, the PCB layout should be adjusted accordingly.

5.1 PCB Layout for Input Filter

If the device is placed on both sides, the input filter should be placed on the bottom layer as much as possible to reduce the coupling of the high-frequency part of the output to the input filter. The part in the red box as Figure 15 shows.

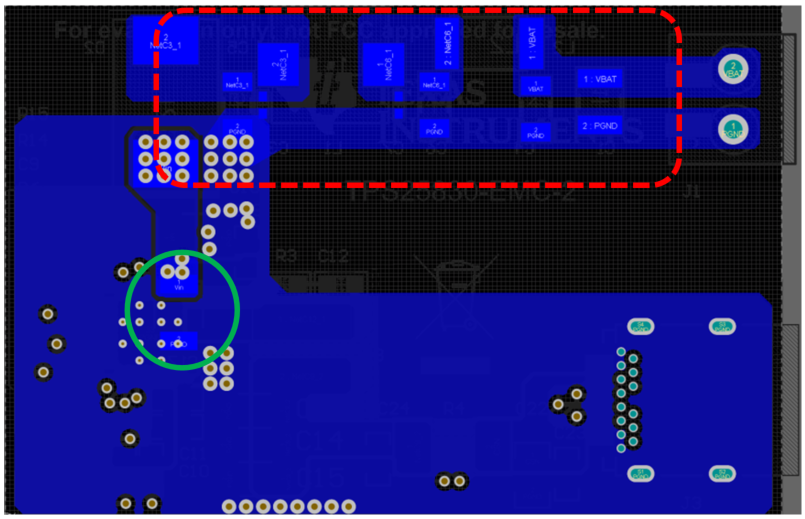

Figure 15. Bottom Layer of the PCB Layout for Input Filter

5.2 Application of DC/DC Power Loop PCB Layout

For specific PCB layout, see Section 4.2. The SW line of point B should be as short as possible (Figure 16). The output inductor should be as close as possible to the chip. One input capacitor is placed on the top layer near the VIN pin of the chip, and the other input capacitor is placed on the bottom layer in the green circle in Figure 15. One end of the capacitor should be as close as possible to the VIN input of the chip, and place the other end (ground) of the capacitor as close as possible to the via of the PGND pin of the chip to ensure the shortest path between the VIN and PGND pin of the chip.

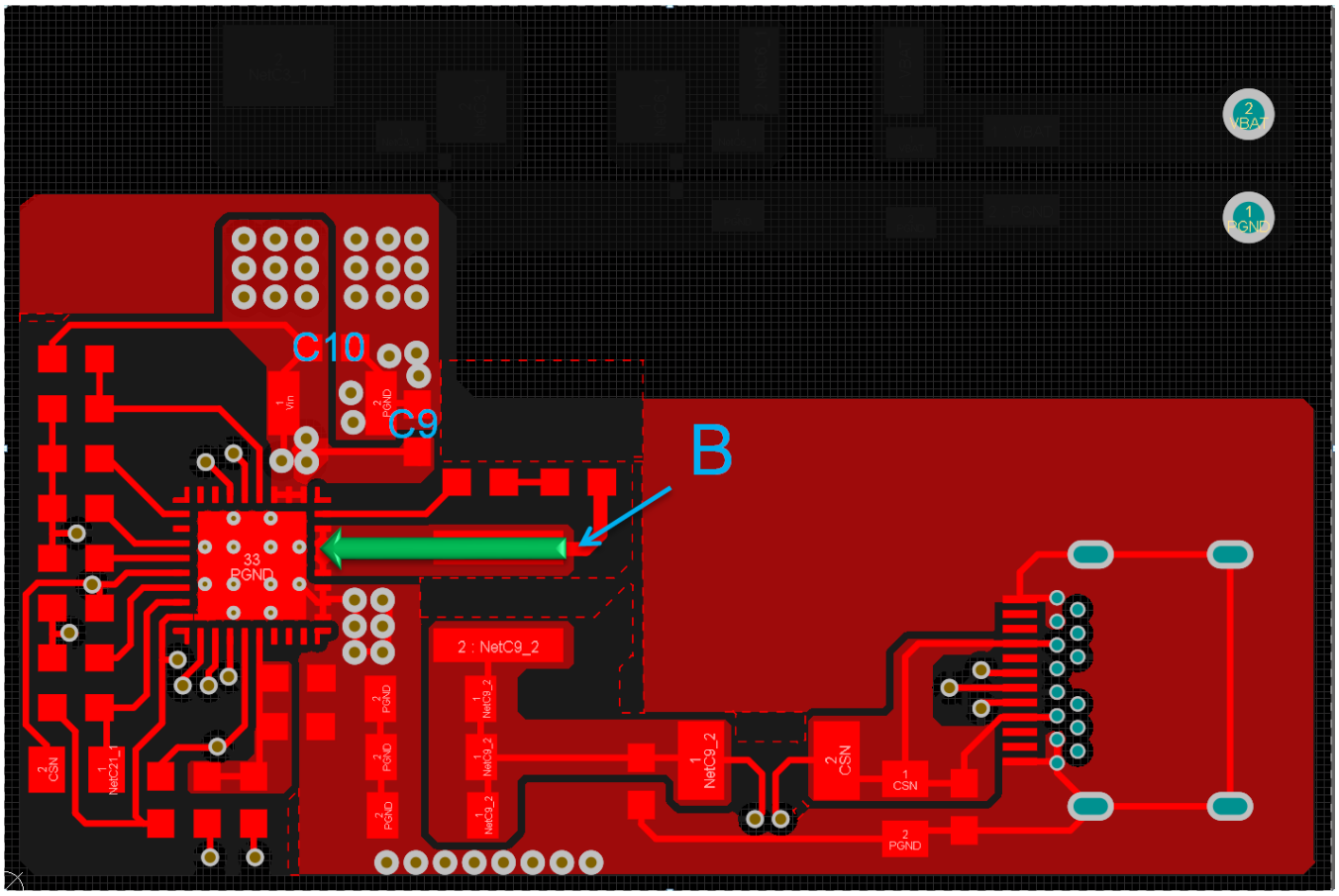

Figure 16. PCB Layout for the Power Part in the Top Layer

5.3 Application of Four-Layer PCB Layout

For specific PCB layout, see Section 4.3. The power part is mainly placed on the top layer and the bottom layer, and the signal part is mainly placed on the top layer and the third layer. Do not include any power and signal lines on the second layer. The entire layer of the power ground PGND should be copper clad.

5.4 EMC Conduction Test Result When the Device is Placed on Both Sides

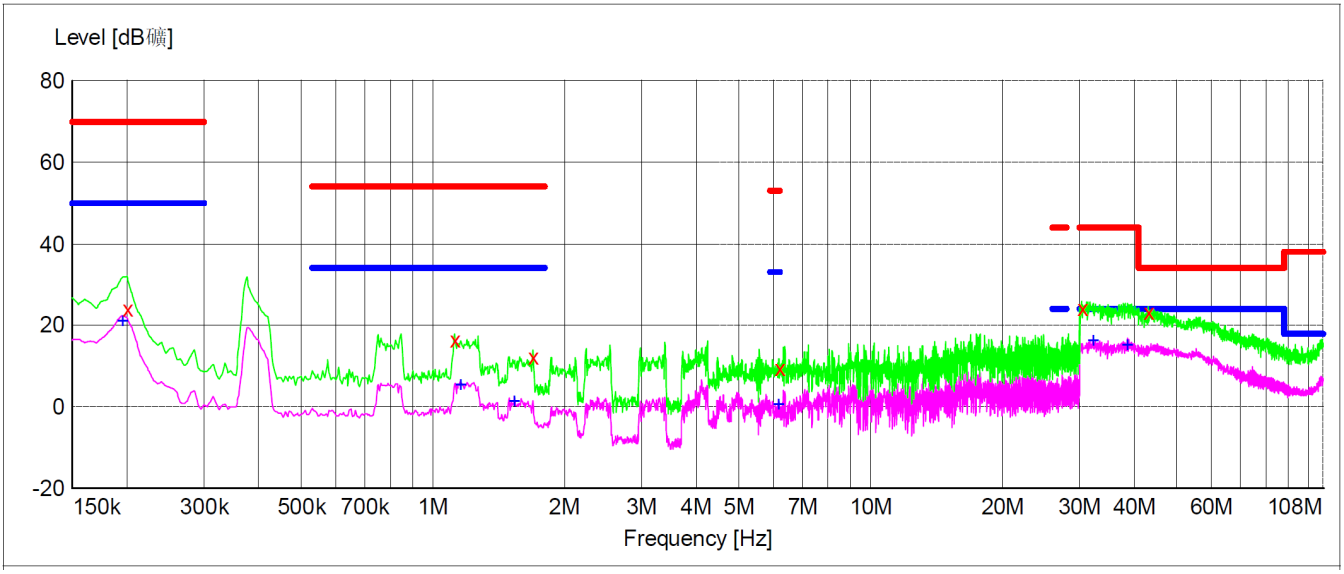

Figure 17. EMC Conduction Test Result When the Device is Placed on Both Sides

6 Conclusion of PCB Layout

1. The input and output capacitors should be as close as possible to the input and output pins of the chip, and the traces should be as wide and short as possible. This point is very important. If the PCB layout allows, do not punch holes in VIN lines and copper.
2. Do not punch holes on SW lines. Under the premise of meeting the heat dissipation and current carrying capacity, the area of copper clad should be as small as possible to reduce the parasitic capacity of the PCB. This is vital.
3. For the PCB layout of Ia and Ib, the loop area surrounded by the power loop should be as small as possible.
4. The area enclosed by the BOOT circuit is as small as possible.
5. Power ground PGND and the signal ground AGND should be separated in the actual PCB layout.
6. The distance between the input filter section and the output power section must be at least 15 mm to prevent the output high-frequency signal from coupling into the input filter.
7. The power and signal lines of each layer of the PCB should be designed as reasonable.
8. Filter capacitors, RT, IMON, ILMIT signal parts and the resistors and capacitors of other parts should be as close as possible to the chip pins.
9. Use shielded inductors or molded inductors to reduce high-frequency radiation.
10. The input and output capacitors should be selected from different capacities and packages, and should be in parallel when designing the PCB layout. This can filter high-frequency signals at different frequencies. This is very important. For example: 10 µF + 0.1 µF + 2.2 nF.

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