Application Report
SLVAE93–December 2019

The Stability of a D-CAP2™ Converter with Different Kinds of Capacitors

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ABSTRACT

D-CAP2™ converters realize a low-ESR ceramic output capacitor by using a ripple injection method, but the ceramic capacitors are currently out of stock in the market, resulting in higher prices. This application report discusses the stability of D-CAP2 converters with different kinds of capacitors, especially electrolytic and polymer capacitors.

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Trademarks

D-CAP2 is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

1 Characteristics of Different Capacitors

1.1 MLCC

MLCC (multi-layer ceramic capacitors) are fixed capacitors with the ceramic material acting as the dielectric. They are constructed of two or more alternating layers of ceramic and a metal layer acting as the electrodes. MLCCs offer the following:

- Small volume
- Lowest ESR and ESL
- A capacitance derating with DC bias

1.2 Non-solid Electrolytic Capacitor

An electrolytic capacitor is a type of capacitor that uses an electrolyte (an ionic conducting liquid) as one of its plates to achieve a larger capacitance per unit volume than other types. An electrolytic capacitor offers the following:

- Mature technology with low cost materials
- Higher capacitance values than MLCC
- High ESR and ESL

1.3 Solid Polymer Electrolytic Capacitor

A solid polymer capacitor is an electrolytic capacitor with a solid electrolyte of a conductive polymer. Table 1 shows the comparison of different types of capacitors. Solid polymer capacitors offer the following:

- Lower ESR and higher ripple current ratings than non-solid electrolytic capacitors
- Much better temperature dependence
- Considerably longer service life than aluminum electrolytic capacitors with non-solid electrolytes.

Table 1. The Comparison of Different Types of Capacitors

TYPE	SIZE	CAPACITANCE	COST	ESR/ESL	OTHER
MLCC	Small	Small	High	Low	There is a capacitance derating with DC bias.
Non-solid Electrolytic Capacitor	Large	Large	Low	High	Offering higher capacitance values than MLCC
Solid Electrolytic Capacitor	Middle	Large	Middle	Middle	Has much better temperature dependence and a considerably longer service life

2 The Stability of the Converter

In general, bode plots and load transients are used to evaluate the stability of the system.

2.1 D-CAP2™ Open Loop Transfer Function

Figure 1 shows the block diagram of the D-CAP2, including a comparator that has a ripple injection circuit. Equation 1 is the open-loop transfer function.

$$G_{open}(s) = G_{dv}(s) H_{FB}(s) H_{COMP}(s) H_d(s)$$

$$= \frac{V_{in}(1 + r_C C_{out} s)}{1 + \frac{L + R_L C_{out}(r_L + r_C)}{R_L + r_L} s + \frac{L C_{out}(R_L + r_C)}{R_L + r_L} s^2} \frac{R_2}{R_1 + R_2} \frac{A_{cp}}{V_{in}} (1 + s\tau_c) e^{-sT_{on}/2}$$

where

- V_{in} is input voltage
- L is the inductance
- C_{out} is the output capacitance
- R_L is the load resistance
- r_L is DCR of the inductor
- r_C is the ESR of the output capacitor
- R_1 is the upper resistance of feedback
- R_2 is the bottom resistance of feedback
- A_{cp} is the voltage gain of ripple injection circuit
- T_c is the time constant of ripple injection circuit

(1)

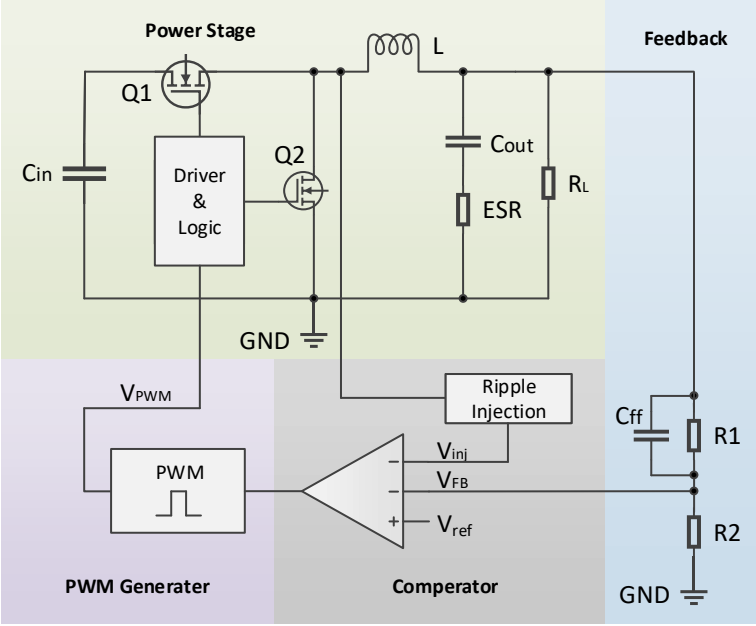

Figure 1. The Block Diagram of the D-CAP2

From Equation 1, there are two zeros and two poles in D-CAP2 system.

$$f_{z1} = \frac{1}{2\pi T_c} \quad (2)$$

$$f_{z2} = \frac{1}{2\pi r_C C_{out}} \quad (3)$$

$$f_{p1,2} = \frac{1}{2\pi \sqrt{L C_{out}}} \quad (4)$$

For the D-CAP2, the ripple injection circuit is inside the IC, so f_{z1}, which is generated by a ripple injection circuit, cannot be changed by external components. f_{z2} and $f_{p1,2}$ can be designed by r_C, L, and C_{out} to make the system stable. If the output capacitors are ceramic capacitors, the ESR is lower and f_{z2}, which is generated by ESR and C_{out}, is very high. Figure 2 shows the bode plot of the D-CAP2.

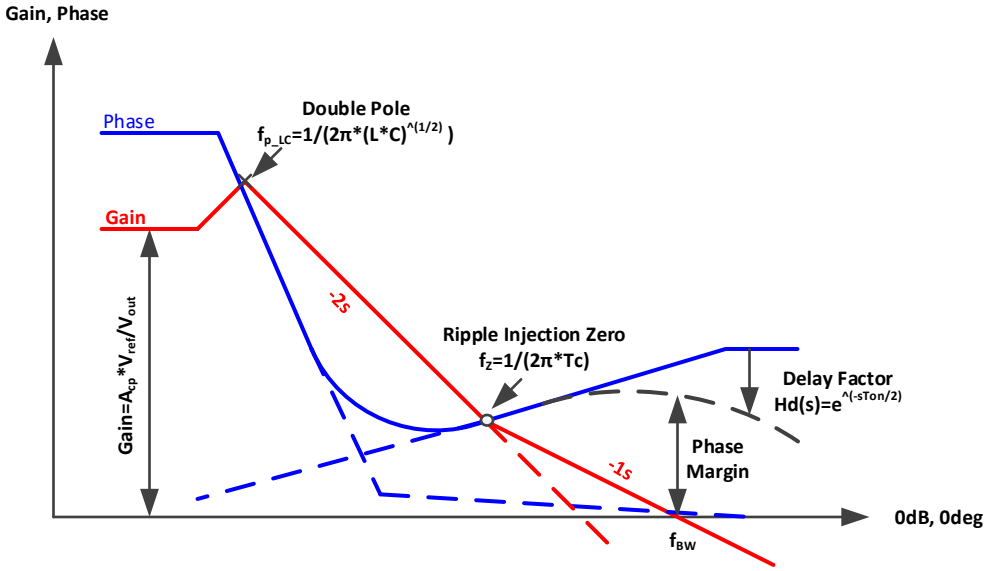

Figure 2. Bode Plot of the D-CAP2

2.2 Stability Analysis

Figure 3 shows the bode plots with different ESR. If C_{out} is large and ESR is small, $f_{p1,2}$ is lower, which can lead to very low bandwidth. If the phase margin is lower than 45°, the system can be unstable. If C_{out} remains unchanged and increasing, the ESR of the output capacitors and the frequency of ESR zero is decreased. It is helpful to increase the bandwidth and phase margin.

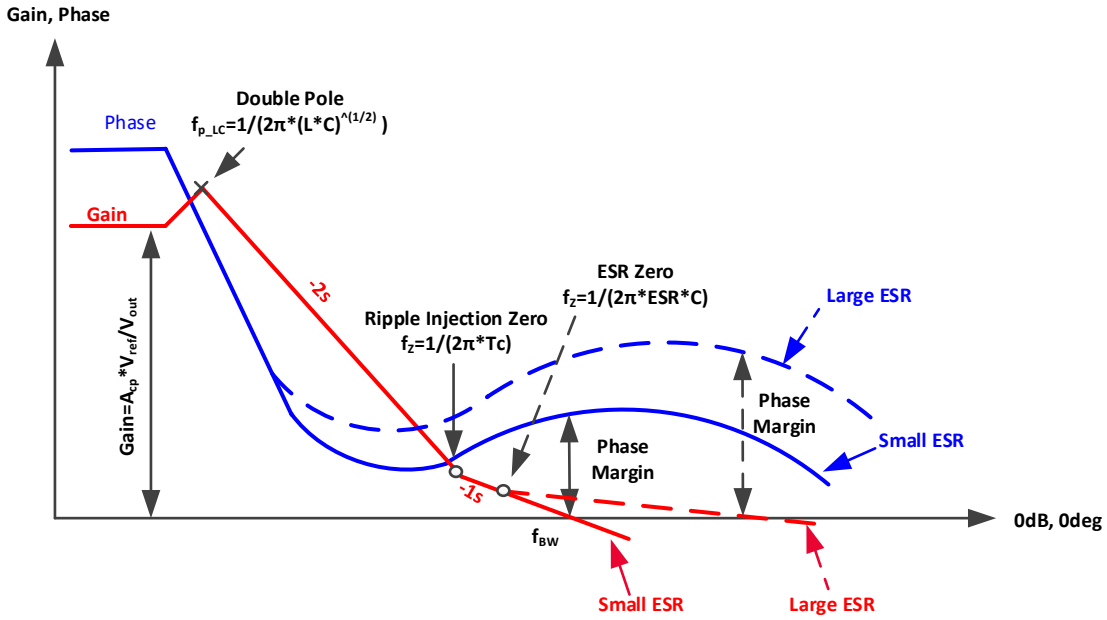

Figure 3. Bode Plot with Different ESR

In addition, the loop stability criteria for the D-CAP2 mode with ripple injection can be expressed as:

$$\left(\frac{L}{R_r C_r} + R_{ESR}\right) C_{out} \geq \frac{T_{on}}{2} \tag{5}$$

Note that in Equation 5, increasing R_{ESR} is helpful for the stability.

PWM is generated by FB ripple and reference voltage. It is very important that the FB ripple must be synchronic with inductor current, or the system is unstable. The equivalent FB ripple consists of output ripple and internal ripple injection. Output ripple includes ESR ripple and C_{out} ripple, which is generated by charging and discharging of output capacitor. Internal ripple injection and ESR ripple are synchronic with inductor current, but C_{out} ripple has a 90° phase shift. To keep the loop stable, the sum of the internal ripple injection and ESR ripple must be larger than the C_{out} ripple. There are four cases for FB ripple:

- If C_{out} is large and ESR is small, C_{out} ripple is small. The equivalent FB ripple is dominated by internal ripple. It is stable. Figure 4 shows the ripple waveforms.

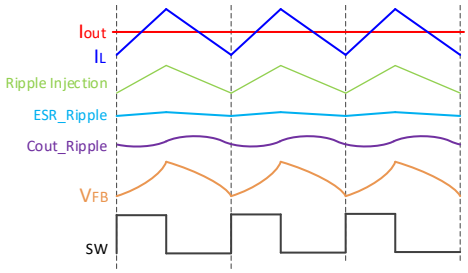

Figure 4. Ripple Waveforms (Large Cout and Small ESR)

- If C_{out} is large and ESR is large, C_{out} ripple is small. The equivalent FB ripple is dominated by internal ripple and ESR ripple. It is stable. Figure 5 shows the ripple waveforms.

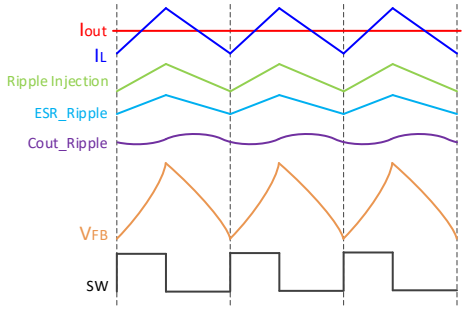

Figure 5. Ripple Waveforms (Large Cout and Large ESR)

- If C_{out} is small and ESR is small, C_{out} ripple is large. The equivalent FB ripple is dominated by internal ripple and C_{out} ripple. When C_{out} ripple is larger than internal ripple, it is unstable. Figure 6 shows the ripple waveforms.

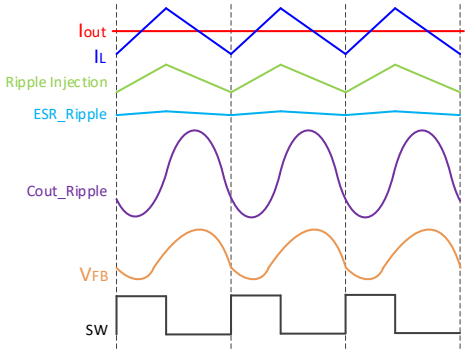

Figure 6. Ripple Waveforms (Large Cout and Small ESR)

- If C_{out} is small and ESR is large, C_{out} ripple would be large. The ESR ripple is helpful for the stability, but it hard to say whether it is stable or not.

2.3 Bench Verification

To verify the previously described theoretical analysis, different kinds of capacitors are used as the output capacitors. Table 2 shows the detailed information of these capacitors.

Table 2. Capacitor Information

CAPACITANCE	SIZE	RATED VOLTAGE	CAPACITANCE AT 5 V	ESR
4.7 µF	5 × 11	50 V	4.7 µF	1900 mΩ
10 µF	0805	16 V	5.2 µF	2 mΩ
2 × 22 µF	1210	25 V	38 µF	1 mΩ
47 µF	5 × 11	25 V	47 µF	900 mΩ
100 µF	6.3 × 6	16 V	100 µF	25 mΩ
100 µF	6.3 × 11	16 V	100 µF	220 mΩ

The TPS563201EVM is used for the verification. Figure 7 shows the schematic of the TPS563201EVM.

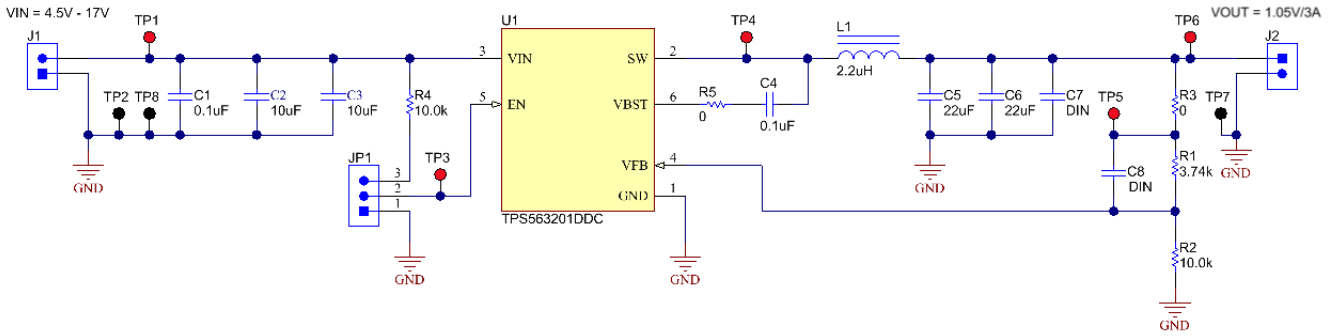

Figure 7. Schematic of the TPS563201EVM

2.3.1 Bode Plot

Figure 8 through Figure 13 show the bode plots. Table 2 is the test results of bode plot. The test conditions: V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 2 A.

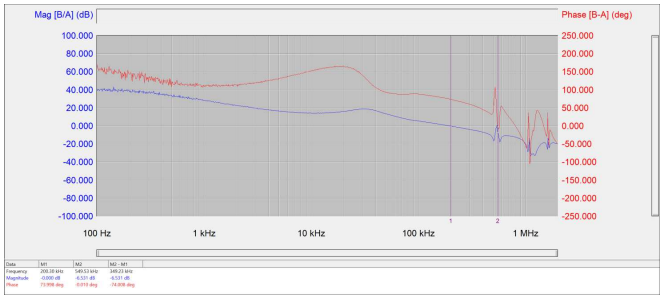

Figure 8. C_{out} = 4.7 µF

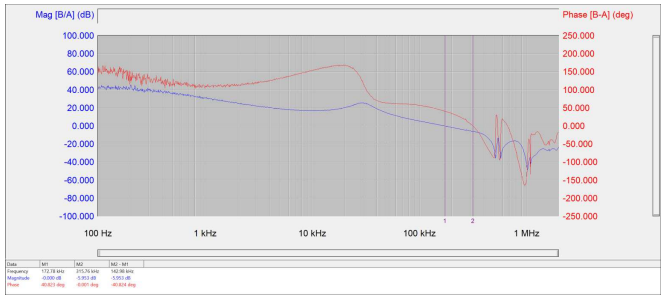

Figure 9. C_{out} = 10 µF

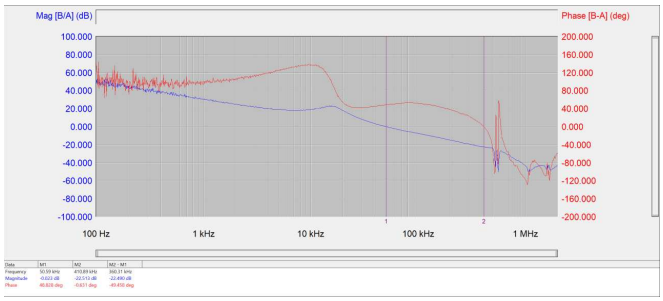

Figure 10. C_{out} = 2 × 22 µF

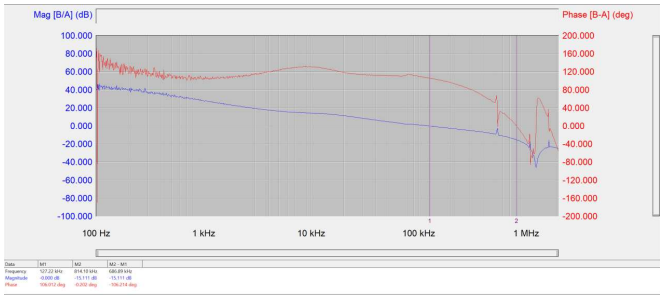

Figure 11. C_{out} = 47 µF

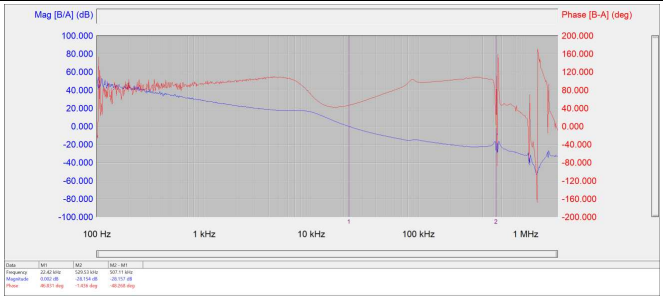

Figure 12. C_{out} = 100 µF, 25 mΩ

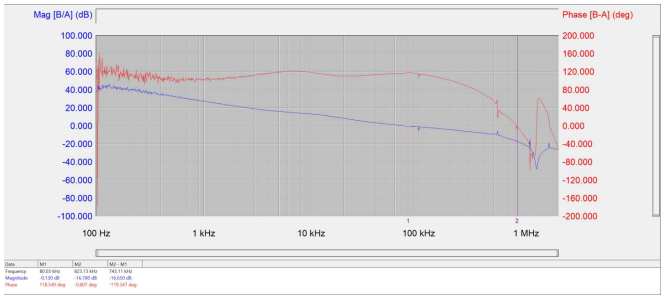

Figure 13. C_{out} = 100 µF, 220 mΩ

Table 3. The Test Result of the Bode Plot

CAPACITANCE	BANDWIDTH	PHASE MARGIN	PHASE MARGIN
4.7 µF, 1.9 Ω	200 kHz	73.9°	6.5 dB
10 µF, 2 mΩ	172 kHz	40.8°	5.9 dB
2 × 22 µF, 1 mΩ	50 kHz	48.8°	22.5 dB
47 µF, 900 mΩ	127 kHz	106°	15.1 dB
100 µF, 25 mΩ	22 kHz	46.8°	28.1 dB
100 µF, 220 mΩ	80 kHz	118.5°	16.8 dB

From the bode plots, it can be seen that the phase margin is not enough. You can also see that ESR is small and the large ESR is helpful for the phase margin. The test results are consistent with the theoretical analysis.

2.3.2 Load Transient

Figure 14 through Figure 19 show the load transient waveforms. Table 3 is the test results of load transient. The test conditions: V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 1 A- > 3 A with a slew rate = 0.25 A/µs.

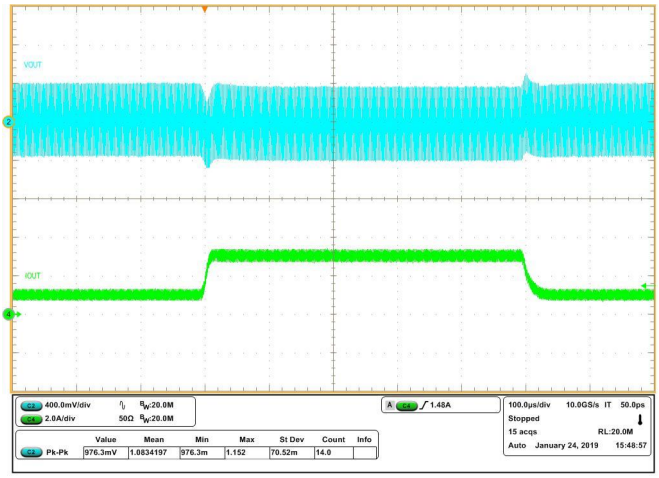

Figure 14. C_{out} = 4.7 µF

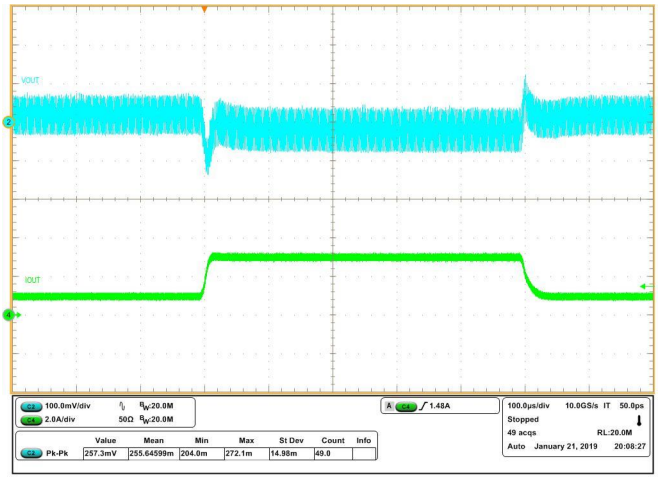

Figure 15. C_{out} = 10 µF

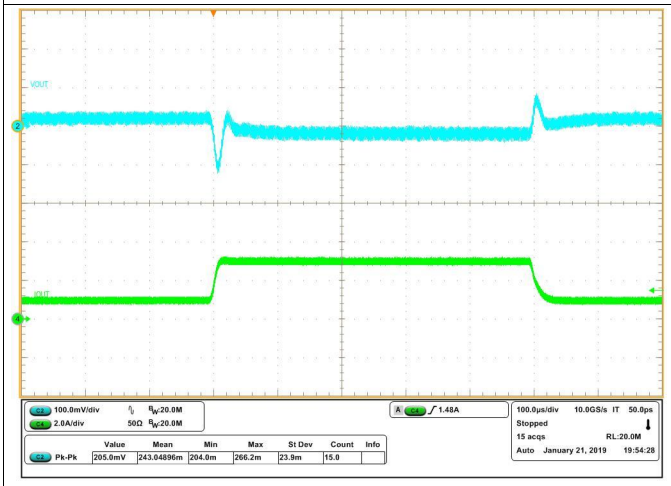

Figure 16. C_{out} = 2 × 22 µF

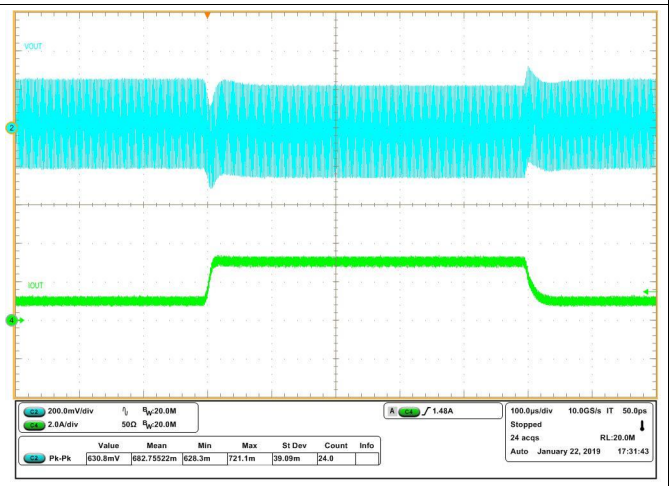

Figure 17. C_{out} = 47 µF

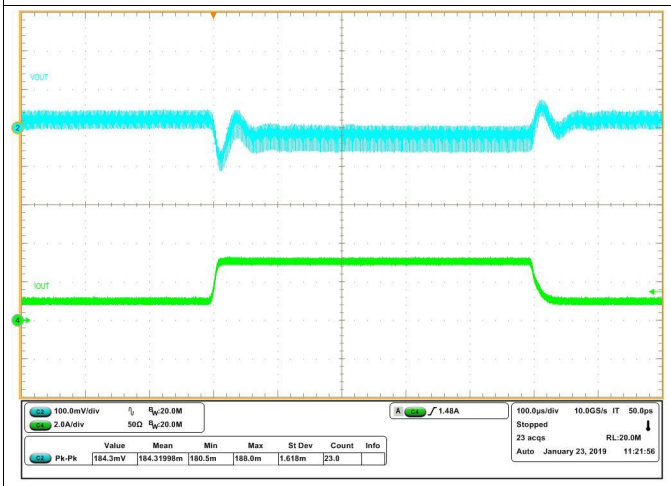

Figure 18. C_{out} = 100 µF, 25 mΩ

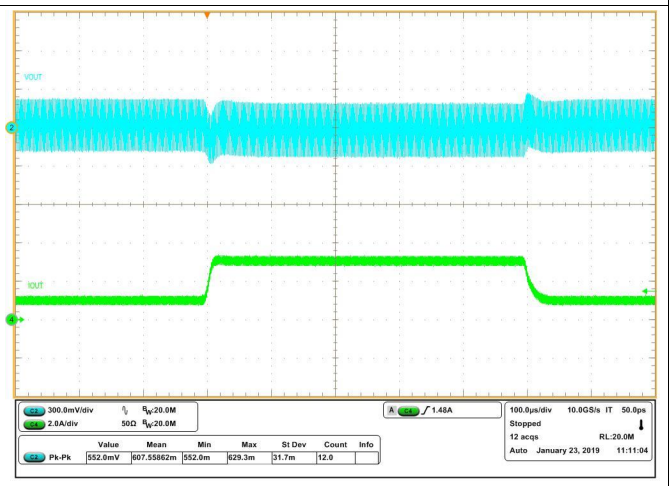

Figure 19. C_{out} = 100 µF, 220 mΩ

Table 4. The Test Result of the Bode Plot

CAPACITANCE	VOUT PEAK-TO-PEAK
4.7 µF, 1.9 Ω	976.3 mV
10 µF, 2 mΩ	257.3 mV

Table 4. The Test Result of the Bode Plot (continued)

CAPACITANCE	VOUT PEAK-TO-PEAK
2 × 22 µF, 1 mΩ	205 mV
47 µF, 900 mΩ	630.8 mV
100 µF, 25 mΩ	184.3 mV
100 µF, 220 mΩ	552 mV

From the load transient waveforms, the system is stable when the electrolytic capacitor is used.

2.3.3 Output Voltage Ripple

Figure 20 through Figure 25 show the load transient waveforms. Table 5 is the test results of output voltage ripple. The test conditions: V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 1 A.

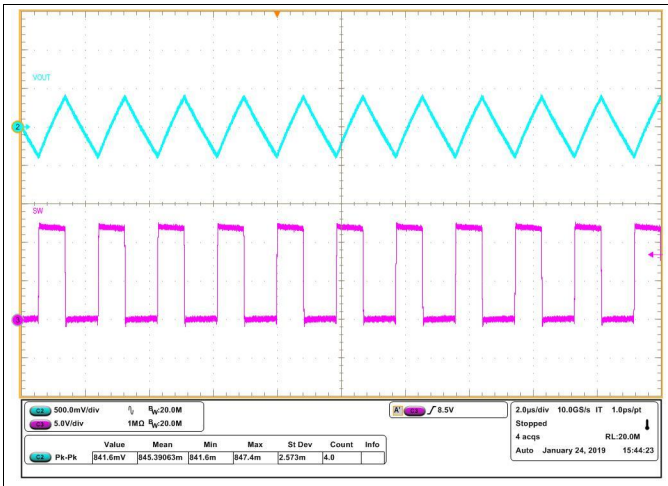

Figure 20. C_{out} = 4.7 µF

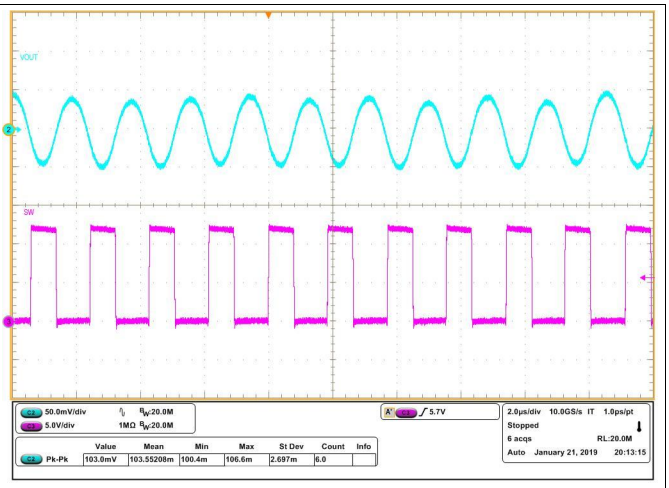

Figure 21. C_{out} = 10 µF

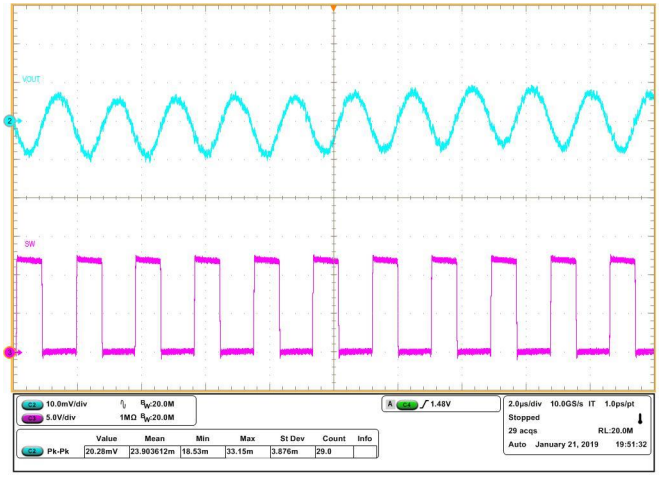

Figure 22. C_{out} = 2 × 22 µF

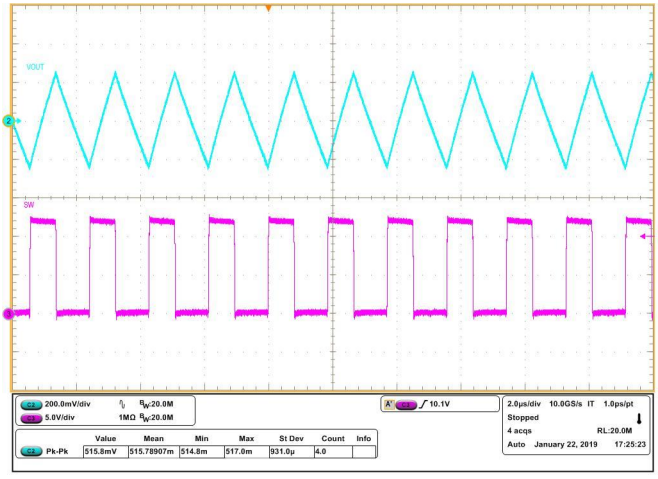

Figure 23. C_{out} = 47 µF

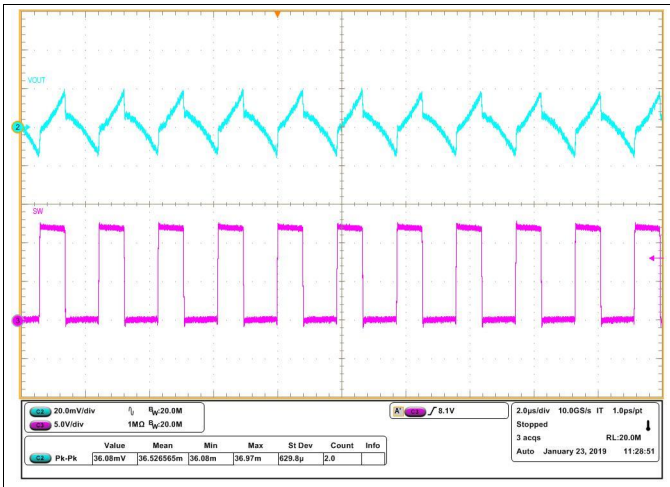

Figure 24. C_{out} = 100 µF, 25 mΩ

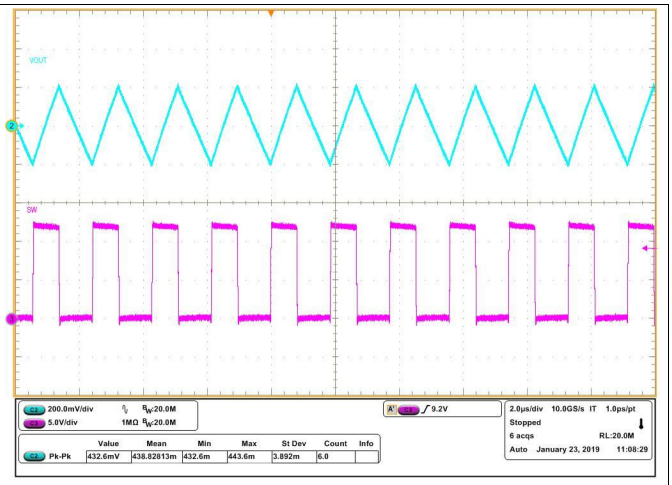

Figure 25. C_{out} = 100 µF, 220 mΩ

Table 5. The Test Results of the Bode Plot

CAPACITANCE	VOUT PEAK-TO-PEAK
4.7 µF, 1.9 Ω	841.6 mV
10 µF, 2 mΩ	103 mV
2 × 22 µF, 1 mΩ	20.3 mV
47 µF, 900 mΩ	515.8 mV
100 µF, 25 mΩ	36.1 mV
100 µF, 220 mΩ	432.6 mV

From the output voltage ripple waveforms, the large ESR increases output voltage ripple. If the application is sensitive to the output ripple, it is necessary to reduce the output ripple by some methods.

3 Hybrid Output Capacitors

From the previously described theoretical analysis and bench verification, it can be seen that the output voltage ripple would be very large because of the larger ESR if the electrolytic capacitor is used. A ceramic capacitor in parallel at the output is useful to reduce the output ripple.

3.1 Impedance of Hybrid Output Capacitor

Figure 26 shows the hybrid output capacitor network. The equivalent impedance can be expressed as Equation 6 and Equation 7.

$$Z_{out} = \frac{\left[R_1R_2\left(R_1+R_2\right)+\frac{R_1}{w^2C_2^2}+\frac{R_2}{w^2C_1^2}\right]+j\left[\left(R_1R_2+\frac{wR_2C_2-wR_1C_1-1}{w^2C_1C_2}\right)\left(\frac{1}{wC_1}+\frac{1}{wC_2}\right)\right]}{\left(R_1+R_2\right)^2+\left(\frac{1}{wC_1}+\frac{1}{wC_2}\right)^2} \quad (6)$$

$$Z_{ESR} = \frac{R_1 R_2 (R_1 + R_2) + \frac{R_1}{w^2 C_2^2} + \frac{R_2}{w^2 C_1^2}}{(R_1 + R_2)^2 + \left(\frac{1}{wC_1} + \frac{1}{wC_2}\right)^2} \quad (7)$$

where

- C_1 is the capacitance of electrolytic capacitor
- R_1 is the ESR
- C_2 is the capacitance of ceramic capacitor
- R_2 is the ESR

Since $R_1 \gg R_2$ and $C_1 > C_2$, it is easy to note that $R1 / (w\ C_2)^2 \gg R_2 / (w\ C1)^2$. In addition, the value of $R_1R_2(R_1 + R_2)$ and $(R_1 + R_2)^2$ are very small, and can be ignored. So, the equivalent ESR can be expressed as Equation 8.

$$Z_{ESR} \approx \frac{R_1}{\left(1 + \frac{C_2}{C_1}\right)^2} \quad (8)$$

In Equation 8, note that the equivalent ESR is related to the value of R_1 and C_2 / C_1. So if $C_2 \ll C_1$, the parallel ceramic capacitor would be not useful in reducing ESR.

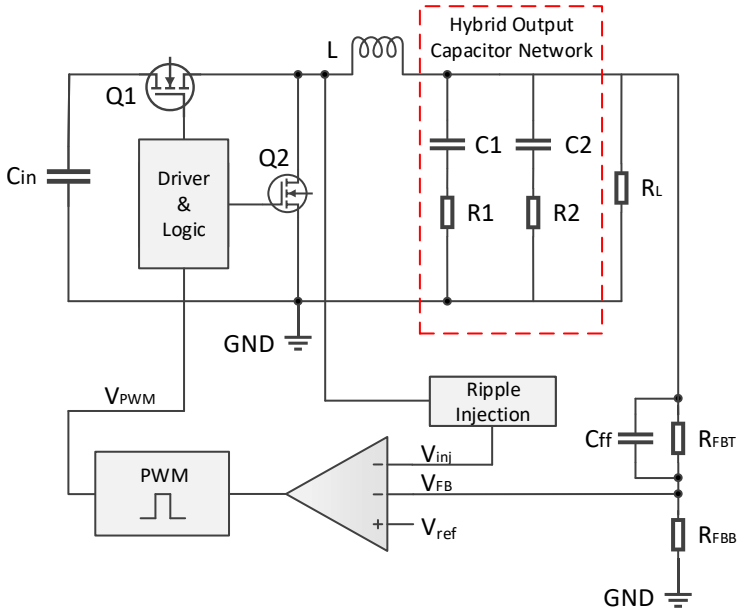

Figure 26. The Hybrid Output Capacitor

3.2 Test Result

Table 6 shows the test result of output voltage ripple with hybrid output capacitors. The test is based on the TPS561201EVM. Test conditions: V_{in} = 12 V, V_{out} = 1.05 V, I_{out} = 1 A.

Table 6. The Output Voltage Ripple with Hybrid Output Capacitors

OUTPUT CAPACITORS	OUTPUT RIPPLE VOLTAGE
22 µF (electrolytic)	344 mV
22 µF (electrolytic) + 0.1 µF (ceramic, 0603)	345.5 mV
22 µF (electrolytic) + 0.1 µF (ceramic, 0805)	298.4 mV
22 µF (electrolytic) + 0.47 µF (ceramic, 0805)	209.5 mV
22 µF (electrolytic) + 1 µF (ceramic, 0603)	211.9 mV
22 µF (electrolytic) + 1 µF (ceramic, 0805)	157.3 mV
22 µF (electrolytic) + 2.2 µF (ceramic, 0805)	99.8 mV
22 µF (electrolytic) + 4.7 µF (ceramic, 0805)	56.5 mV
22 µF (electrolytic) + 10 µF (ceramic, 0805)	30.9 mV

From the test result, the 0.1-µF (0603) ceramic capacitor is not useful in reducing output voltage ripple because the capacitance is too small in relation to the 22-µF electrolytic capacitor. With the increase of the value of ceramic capacitor, the output voltage ripple becomes smaller and smaller.

4 Summary

This application report discussed the influence of the electrolytic capacitor on system stability from theoretical analysis and bench verification. The large ESR of an electrolytic capacitor is useful for increasing the phase margin, and then enhancing the stability of the system. Large ESR results in large output voltage ripple, so the effect of parallel ceramic capacitors on output ripple is further analyzed. The larger the capacitance ratio of ceramic capacitor to electrolytic capacitor, the smaller the ESR and the smaller the output ripple.

5 References

1. Texas Instruments, *D-CAP2™ Frequency Response Model Based on Frequency Domain Analysis of Fixed On-Time with Bottom Detection having Ripple Injection Application Report*

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