TPS386000-Q1 Pin FMEA

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ABSTRACT

The TPS386000-Q1 family of voltage supervisors monitors four power rails that are greater than 0.4 V and one power rail that is less than 0.4 V (including negative voltage) with a 0.25% (typical) threshold accuracy. Each of the four supervisory circuits (SVS-*n*) assert a $\overline{\text{RESET}}n$ or RESET*n* output signal when the SENSE*m* input voltage drops below the programmed threshold. With external resistors, the threshold of each SVS-*n* can be programmed (where *n* = 1, 2, 3, 4 and *m* = 1, 2, 3, 4L, 4H).

Each SVS-*n* has a programmable delay before releasing $\overline{\text{RESET}}n$ or RESET*n*. The delay time can be set from 1.4 ms to 10 seconds through the CT*n* pin connection. Only SVS-1 has an active-low manual reset ($\overline{\text{MR}}$) input which is a logic-low input to $\overline{\text{MR}}$ that asserts $\overline{\text{RESET1}}$ or RESET1.

SVS-4 monitors the threshold window using two comparators. The extra comparator can be configured as a fifth SVS to monitor negative voltage with the voltage-reference output, VREF.

The TPS386000-Q1 device has a very-low quiescent current of 12 mA (typical) and is available in a small, 4–mm × 4–mm, QFN-20 package.

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This application note provides a **F**ailure **M**odes and **E**ffects **A**nalysis (FMEA) for the device pins of the TPS386000-Q1 quad-supply voltage-supervisor device with programmable delay and watchdog timer. The failure conditions covered in this document include typical failure scenarios such as short-circuit to GND, short-circuit to VCC, short-circuit to a neighboring pin, and if the pin is left open. The following tables list how these conditions affect the device. The first effect considered is whether the condition damages the pin in question or the device itself. The second effect considered is whether the device is functional under the condition. Lastly, the analysis includes a comments section that discusses how the particular condition affects the device operation.

NOTE: The first letter, *X*, of the pin name is expressed with the active-low bar.

Table 1. Classification of Failure Effects

Class	Failure Effects
A	Damage to device affects application functionality
B	No damage to device but thermal damage must be considered
C	No damage to device but can affect application functionality
D	No damage to device and no affect to application functionality

Table 2. Pin FMEA Analysis for Pin Short-Circuit to GND

Pin		Short to GND			
No.	Name	Damage	Functionality	Comments	Class
1	$\overline{\text{MR}}$	NO	YES	Can affect functionality of the sub-CPU circuit that drives $\overline{\text{MR}}$ pin.	D
2	CT4	NO	YES	A pulldown transistor is located on each pin. If these pins are shorted to GND, the programmable delay circuit does not function correctly.	D
3	CT3				
4	CT2				
5	CT1				
6	SENSE4H	NO	YES		D
7	SENSE4L	NO	YES	The corresponding $\overline{\text{RESETn}}$ output is always asserted if the SENSEn input is shorted to GND.	D
8	SENSE3				
9	SENSE2				
10	SENSE1				
11	NC	NO	YES	This pin has no electrical connection.	D
12	GND	NO	YES	Normal operating condition	D
13	VREF	NO	YES	1.2 V at 5 mA (max)	B
14	VCC	NO	Can affect functionality	No damage to device, can affect application functionality. Increases leakage.	C
15	$\overline{\text{RESET1}}$	NO	YES	Whichever device is connected to the $\overline{\text{RESETn}}$ the output is always in reset if these pins are shorted to GND.	D
16	$\overline{\text{RESET2}}$				
17	$\overline{\text{RESET3}}$				
18	$\overline{\text{RESET4}}$				
19	$\overline{\text{WDO}}$	NO	Can affect functionality	User does not have any watchdog functionality.	C
20	WDI	NO	Can affect functionality	User does not have any watchdog functionality.	C

Table 3. Pin FMEA Analysis for Pin Left Open

Pin		Short to GND			
No.	**Name**	**Damage**	**Functionality**	**Comments**	**Class**
1	$\overline{\text{MR}}$	NO	Can affect functionality	Undefined operating condition, no damage, increases leakage	C
2	CT4	NO	YES	Leaving these pins open results in a 20-ms (typical) delay.	D
3	CT3				
4	CT2				
5	CT1				
6	SENSE4H	NO	YES	Undefined operating condition ($\overline{\text{RESET4}}$ tends to become High)	D
7	SENSE4L	NO	YES	Undefined operating condition ($\overline{\text{RESET4}}$ tends to become Low)	D
8	SENSE3	NO	YES	Undefined operating condition ($\overline{\text{RESET3}}$ tends to become Low)	D
9	SENSE2	NO	YES	Undefined operating condition ($\overline{\text{RESET2}}$ tends to become Low)	D
10	SENSE1	NO	YES	Undefined operating condition ($\overline{\text{RESET1}}$ tends to become Low)	D
11	NC	NO	YES	This pin has no electrical connection.	D
12	GND	NO	NO	Undefined operating condition, no damage, increases leakage	C
13	VREF	NO	YES	Normal operating condition	D
14	VCC	NO	NO	Undefined operating condition, no damage, increases leakage	C
15	$\overline{\text{RESET1}}$	NO	YES	Normal operating condition, this pin is an open-drain output.	D
16	$\overline{\text{RESET2}}$				
17	$\overline{\text{RESET3}}$				
18	$\overline{\text{RESET4}}$				
19	$\overline{\text{WDO}}$				
20	WDI	NO	Can affect functionality	User does not have any watchdog functionality.	C

Table 4. Pin FMEA Analysis for Pin Short-Circuit to VCC

Pin		Short to GND			
No.	**Name**	**Damage**	**Functionality**	**Comments**	**Class**
1	$\overline{MR}$	NO	YES	Can affect functionality of the sub-CPU circuit that drives $\overline{MR}$ pin.	D
2	CT4	NO	YES	A large current flows during wakeup, but it can be low power. TI recommends to pull these pins up to VCC with a 40k to 200k resistor.	D
3	CT3				
4	CT2				
5	CT1				
6	SENSE4H	NO	YES	The $\overline{RESET4}$ output is always be asserted if the SENSE4H input is shorted to VCC. The DC-DC or LDO that is monitored is affected.	D
7	SENSE4L	NO	YES	The DC-DC or LDO that is monitored is affected.	D
8	SENSE3				
9	SENSE2				
10	SENSE1				
11	NC	NO	YES	This pin has no electrical connection.	D
12	GND	NO	NO	No damage to device, can affect application functionality. Increases leakage.	C
13	VREF	NO	YES	1.2 V at 5 mA (max)	B
14	VCC	NO	YES	Normal operating condition	D
15	$\overline{RESET1}$	YES	NO	I_{RESET} < 5 mA (absolute)	A
16	$\overline{RESET2}$				
17	$\overline{RESET3}$				
18	$\overline{RESET4}$				
19	$\overline{WDO}$	YES	NO	I_{WDO} < 5 mA (absolute)	A
20	WDI	NO	YES	Functionality of FPGA connected to this pin can be affected.	D

Table 5. Pin FMEA Analysis for Pin Short-Circuit to Neighboring Pin

Pin		Short to GND			
No.	**Name**	**Damage**	**Functionality**	**Comments**	**Class**
1	$\overline{MR}$ to CT4	NO	Can affect functionality	No electric damage, increases leakage at $\overline{MR}$. The desired delay is not achieved if these pins are shorted together.	B
2	CT4 to CT3	NO	YES	The desired delay is not achieved if these pins are shorted together.	D
3	CT3 to CT2				
4	CT2 to CT1				
5	CT1 to SENSE4H	NO	YES	The desired delay is not achieved if these pins are shorted together. The respective $\overline{RESETn}$ outputs do not function as desired.	D
6	SENSE4H to SENSE4L	NO	YES	The respective $\overline{RESETn}$ outputs do not function as desired.	D
7	SENSE4L to SENSE3				
8	SENSE3 to SENSE2				
9	SENSE2 to SENSE1				
10	SENSE1 to NC	NO	YES		D
11	NC to GND	NO	YES		D
12	GND to VREF	NO	YES	1.2 V at 5 mA (max)	B
13	VREF to VCC	NO	YES	1.2 V at 5 mA (max)	B
14	VCC to $\overline{RESET1}$	YES	NO	I_{RESET} < 5 mA (absolute)	A
15	$\overline{RESET1}$ to $\overline{RESET2}$	NO	YES		C
16	$\overline{RESET2}$ to $\overline{RESET3}$				
17	$\overline{RESET3}$ to $\overline{RESET4}$				
18	$\overline{RESET4}$ to $\overline{WDO}$				
19	$\overline{WDO}$ to WDI	NO	Can affect functionality	Functionality of FPGA connected to this pin can be affected.	B
20	WDI to $\overline{MR}$	NO	Can affect functionality	Undefined operating condition, no damage, increases leakage	C

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