# TPS43330-Q1 Family Design Checklist

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This application note for the TPS43330-Q1 family, which includes two current-mode synchronous buck controllers and a voltage-mode boost controller, lists the connection details for each pin. The pin details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each pin on a system schematic. In addition to this list, customers are advised to use the information in the data sheets, [TI literature numbers SLVSA82 (TPS43330-Q1 and TPS43332-Q1), SLVSB48 (TPS43333-Q1), SLVSAV6 (TPS43335-Q1 and TPS43336-Q1), SLVSBC2 (TPS43337-Q1), and SLVSAR7 (TPS43350-Q1 and TPS43351-Q1)].

## Device Features

The family members differ in the following features and parameters, with the differences highlighted in red:

| | TPS43330-Q1 | TPS43332-Q1 | TPS43333-Q1 | TPS43335-Q1 | TPS43336-Q1 | TPS43337-Q1 | TPS43350-Q1 | TPS43351-Q1 |
|---|---|---|---|---|---|---|---|---|
| Boost | Yes | Yes | Yes | Yes | Yes | Yes | No | No |
| Buck output drive | 1.5 A | 1.5 A | 1.5 A | 0.7 A | 0.7 A | 1.5 A | 1.5 A | 1.5 A |
| Buck output voltages | ADJ | ADJ | ADJ | ADJ | ADJ | 3.4 V, 1.225 V | ADJ | ADJ |
| Spread-spectrum | No | Yes | No | No | Yes | No | No | Yes |
| Boost-unlock threshold | 8.5 V | 8.5 V | 6.5 V | 8.5 V | 8.5 V | 8.5 V | 8.5 V | 8.5 V |

## Pin Details

Because TPS43350-Q1 and TPS43351-Q1 do not offer a boost converter, some pins are not applicable for these variants. In the following table, those pins are designated by *) following the pin name.

Note that the links in the following table all refer to the TPS43330-Q1 product folder, but the list applies to all variants.

| Pin Name | Pin No. | Pin Group | I/O | Description | Expected Components and Connections | Function, if Not Used |
|---|---|---|---|---|---|---|
| AGND | 23 | Power | O | Analog ground reference | Provide a low-impedance, low-resistance path to GND, ideally, to GND-plane | N/A |
| CBA | 5 | Analog | I | A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckA. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge. | Connect a capacitor of several hundred nF (for example, 220 nF) between CBA and PHA; use low impedance, low inductance, and small loop. Avoid vias. | N/A |
| CBB | 34 | Analog | I | A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckB. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge. | Connect a capacitor of several hundred nF (for example, 220 nF) between CBB and PHB; use low impedance, low inductance, and small loop. Avoid vias. | N/A |

| Pin Name | Pin No. | Pin Group | I/O | Description | Expected Components and Connections | Function, if Not Used |
|---|---|---|---|---|---|---|
| COMPA | 13 | Analog | O | Error amplifier output of BuckA and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of BuckA. Clamping this voltage on the upper and lower ends provides current-limit protection for the external MOSFETs. | Connect a Type 2 compensation network, designed for a bandwidth of 1 / 6th to 1 / 10th of $f_{SW}$. Calculate per Component Selection Tool | N/A |
| COMPB | 26 | Analog | O | Error amplifier output of BuckB and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of BuckB. Clamping his voltage on the upper and lower ends provides current-limit protection for the external MOSFETs. | Connect a Type 2 compensation network, designed for a bandwidth of 1 / 6th to 1 / 10th of $f_{SW}$. Calculate per Component Selection Tool | N/A |
| COMPC *) | 18 | Analog | O | Error-amplifier output and loop-compensation node of the boost regulator | Connect a Type2 compensation network, designed for a bandwidth of 1 / 6th to 1 / 10th of $f_{SW}$ . Consider that boost switches at 50% of buck-swiching frequency. Calculate per Component Selection Tool | N/A |
| DIV *) | 36 | Digital | I | The status of this pin defines the output voltage of the boost regulator. A high input regulates the boost converter at 11 V (for TPS43337-Q1: 8.8 V), a low input sets the value at 7 V, and a floating pin sets 10 V. | Connect to VREG for 11-V (8.8-V) boost output, leave open for 10-V ouput, tie to GND for 7-V output. | Defaults to 10-V boost output |
| DLYAB | 21 | Analog | O | The capacitor at the DLYAB pin sets the power-good delay interval used to de-glitch the outputs of the power- good comparators. Leaving this pin open sets the power-good delay to an internal default value of 20 µs typical. | Choose for desired delay time, for example, 1 nF for 1 ms. Calculate per Component Selection Tool | Defaults to 20 µs typical |
| DS *) | 2 | Digital | I | This input monitors the voltage on the external boost-converter low-side MOSFET for overcurrent protection. An alternative connection for better noise immunity is to a sense resistor between the source of the low-side MOSFET and ground via a filter network. | Connect to top end of boost current sense-resistor or to the drain of the MOSFET. A filter network may be required. | N/A |
| ENA | 16 | Digital | I | Enable input for BuckA (active-high with an internal pullup current source). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller. When both ENA and ENB are low, the device shuts down and consumes less than 4 µA of current. | Pull high for activation, low to de-activate. Hard-wired or µC-controlled | BuckA is active. |
| ENB | 17 | Digital | I | Enable input for BuckB (active-high with an internal pullup current source). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller. When both ENA and ENB are low, the device shuts down and consumes less than 4 µA of current. | Pull high for activation, low to de-activate. Hard-wired or µC-controlled | BuckB is active |
| ENC *) | 19 | Digital | I | This input enables and disables the boost regulator. An input voltage higher than 1.7 V enables the controller. Voltages lower than 0.7 V disable the controller. Because this pin provides an internal pulldown resistor (500 kΩ), enabling the boost function requires pulling it high. When enabled, the controller starts switching as soon as VBAT falls below the boost threshold, depending upon the programmed output voltage. Note that the voltage on VBAT must exceed the boost-unlock threshold of 8.5 V (for TPS43333-Q1, 6.5 V) once, before boost can activate itself with dropping VBAT. | Pull high for activation, low to de-activate. Hard-wired or µC-controlled | Boost is active. |

| Pin Name | Pin No. | Pin Group | I/O | Description | Expected Components and Connections | Function, if Not Used |
|---|---|---|---|---|---|---|
| EXTSUP | 37 | Power | I | One can use EXTSUP to supply the VREG regulator from one of the TPS43330-Q1 or TPS43332-Q1 buck regulator rails to reduce power dissipation in cases where there is an expectation of high VIN. If EXTSUP is unused, leave the pin open without a capacitor installed. | Connect to a permanent source supplying 4.6 V to VIN. If the source in not permanently on, insert a diode prior to the EXTSUP input. Decouple with approximately 100 nF. | Leave open |
| FBA | 12 | Analog | I | Feedback voltage pin for BuckA. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor-divider network between the buck output and the feedback pin sets the desired output voltage. | Choose a resistor network to set the FBA voltage to 0.8 V, allow for >10 µA current. For noise cancellation, a capacitor on the order of 47 pF to 100 pF in parallel with the lower resistor can help. | N/A |
| FBB | 27 | Analog | I | Feedback voltage pin for BuckB. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage. | Choose a resistor network to set the FBA voltage to 0.8 V, allow for >10 µA current. For noise cancellation, a capacitor on the order of 47 pF to 100 pF in parallel with the lower resistor can help. | N/A |
| GA1 | 6 | Power | O | This output can drive the external high-side N-channel MOSFET for buck regulator BuckA. The output provides high peak currents to drive capacitive loads. The gate drive reference is to a floating ground provided by PHA that has a voltage swing provided by CBA. | Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If FETs must be slowed down, use a series resistor in this line (for example, 10 Ω). | N/A |
| GA2 | 8 | Power | O | This output can drive the external low-side N-channel MOSFET for buck regulator BuckA. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin. | Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If FETs must be slowed down, use a series resistor in this line (for example, 10 Ω). | N/A |
| GB1 | 33 | Power | O | This output can drive the external high-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. The gate drive reference is to a floating ground provided by PHB that has a voltage swing provided by CBB. | Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If FETs must be slowed down, use a series resistor in this line (for example, 10 Ω). | N/A |
| GB2 | 31 | Power | O | This output can drive the external low-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin. | Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If FETs must be slowed down, use a series resistor in this line (for example, 10 Ω). | N/A |
| GC1 *) | 3 | Power | O | This output can drive an external low-side N-channel MOSFET for the boost regulator. This output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin. | Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If FETs must be slowed down, use a series resistor in this line (for example, 10 Ω). | N/A |
| GC2 | 4 | Power | O | This pin makes a floating output drive available to control the external P-channel MOSFET. This MOSFET can bypass the boost rectifier diode or a reverse protection diode when the boost is not switching or if boost is disabled, and thus reduce power losses. | Connect to gate of diode-bypass FET to reduce losses in the diode and improve efficiency. | Leave open |
| PGA | 15 | Digital | O | Open-drain power-good indicator pin for BuckA. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls below 93% of the set value, or if either VIN or VBAT drops below its respective undervoltage threshold. It has an internal pullup to SA2 (that is, VoutA) of about 50 kΩ. | Connect to the interrupt input of the processor; use for sequencing of the rails [requires Vout of the first rail to be higher than the enable voltage (>1.7 V)] or leave open. An additional pullup of, for example, 10 kΩ can strengthen the output. | Leave open |

| Pin Name | Pin No. | Pin Group | I/O | Description | Expected Components and Connections | Function, if Not Used |
|---|---|---|---|---|---|---|
| PGB | 24 | Digital | O | Open-drain power-good indicator pin for BuckB. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls below 93% of the set value, or if either VIN or VBAT drops below its respective undervoltage threshold. It has an internal pullup to SB2 (that is, VoutB) of about 50 kΩ. | Connect to the interrupt input of the processor; use for sequencing of the rails [requires Vout of the first rail to be higher than the enable voltage (>1.7 V)] or leave open. An additional pullup of, for example, 10 kΩ can strengthen the output. | leave open |
| PGNDA | 9 | Analog | O | Power ground connection to the source of the low-side N-channel MOSFETs of BuckA | Connect solidly (low inductance, low impedance, that is, short, wide PCB trace and plenty of vias) to the GND plane. | N/A |
| PGNDB | 30 | Analog | O | Power ground connection to the source of the low-side N-channel MOSFETs of BuckB | Connect solidly (low inductance, low impedance, that is, short, wide PCB trace and plenty of vias) to the GND plane. | N/A |
| PHA | 7 | Power | O | Switching terminal of buck regulator BuckA, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous-mode operation is desired. | Keep the trace to the FETs and inductor short and low-impedance. | N/A |
| PHB | 32 | Power | O | Switching terminal of buck regulator BuckB, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous-mode operation is desired. | Keep the trace to the FETs and inductor short and low-impedance. | N/A |
| RT | 22 | Analog | O | Connecting a resistor to ground on this pin sets the operational switching frequency of the buck and boost controllers. A short circuit to ground on this pin defaults operation to 400 kHz for the buck controllers and 200 kHz for the boost controller. | Connect a resistor to GND for the appropriate frequency, for example, 160 kΩ for 150 kHz, 40 kΩ for 600 kHz. | Defaults to 400 kHz typical for bucks, 200 kHz for boost |
| SA1 | 10 | Analog | I | High-impedance differential-voltage inputs from the current-sense element (sense resistor or inductor DCR) for each buck controller. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and VIN. (SA1 positive node, SA2 negative node). | Connect to a current-sense resistor chosen for an adequate peak-current limit. Calculate per Component Selection Tool. Route differentially with the SA2 line. A capacitor between SA1 and SA2 can reduce noise; choose approximately 10 nF. | N/A |
| SA2 | 11 | Analog | I | | | N/A |
| SB1 | 29 | Analog | I | High-impedance differential voltage inputs from the current-sense element (sense resistor or inductor DCR) for each buck controller. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and VIN. (SB1 positive node, SB2 negative node). | Connect to a current-sense resistor chosen for an adequate peak-current limit. Calculate per Component Selection Tool. Route differentially with the SB2 line. A capacitor between SB1 and SB2 can reduce noise; choose approximately 10 nF. | N/A |
| SB2 | 28 | Analog | I | | | N/A |
| SSA | 14 | Analog | O | Soft-start or tracking input for buck controller BuckA. The buck controller regulates the FBA voltage to the lower of 0.8 V or the SSA pin voltage. An internal pullup current source of 1 µA (for TPS43337-Q1: 50 µA) is present at the pin, and an appropriate capacitor connected here sets the soft-start ramp interval. Alternatively, a resistor divider connected to another supply can provide a tracking input to this pin. | Connect a capacitor to GND for soft-start (calculate per Component Selection Tool) or connect with a voltage-divider to a leading supply to track that rail. Adapt the value for TPS43337-Q1. | N/A |

| Pin Name | Pin No. | Pin Group | I/O | Description | Expected Components and Connections | Function, if Not Used |
|---|---|---|---|---|---|---|
| SSB | 25 | Analog | O | Soft-start or tracking input for buck controller BuckB. The buck controller regulates the FBB voltage to the lower of 0.8 V or the SSB pin voltage. An internal pullup current source of 1 µA (for TPS43337-Q1: 50 µA) is present at the pin, and an appropriate capacitor connected here sets the soft-start ramp interval. Alternatively, a resistor divider connected to another supply can provide a tracking input to this pin. | Connect a capacitor to GND for soft-start (calculate per Component Selection Tool) or connect with a voltage-divider to a leading supply to track that rail. Adapt the value for TPS43337-Q1. | N/A |
| SYNC | 20 | Digital | I | If an external clock is present on this pin, the device detects it and the internal PLL locks onto the external clock, thus overriding the internal oscillator frequency. The device can synchronize to frequencies from 150 kHz to 600 kHz. A high logic level on this pin ensures forced continuous-mode operation of the buck controllers and inhibits transition to low-power mode. An open or low allows discontinuous-mode operation and entry into low-power mode at light loads. On the TPS43332-Q1, a high level enables frequency-hopping spread spectrum, whereas an open or a low level disables it. | Tie high to force the device to remain in the continuous mode. Leave open or tie to GND to allow LPM. In both cases, the device switches at the frequency as defined by the RT resistor. Apply an external clock to synchronize to a clocking system (150 kHz to 600 kHz). | Leaving it open allows LPM. |
| VBAT | 1 | Analog | I | Battery input sense for the boost controller. If, with the boost controller enabled, the voltage at VBAT falls below the boost threshold, the device activates the boost controller and regulates the voltage at VIN to the programmed boost output voltage. Note that voltage on VBAT must exceed the boost-unlock threshold of 8.5 V (for TPS43333-Q1: 6.5 V) once, before boost can activate itself with dropping VBAT. | Connect via a series resistor on the order of 1 kΩ to VBAT. The resistor acts as a current limit. | N/A |
| VIN | 38 | Power | I | Main Input pin. This is the buck-controller input pin as well as the output of the boost regulator. Additionally, VIN powers the internal control circuits of the device. | Decouple with a capacitance on the order of 10 µF; keep close to the IC with a low-impedance, low-inductance path. Avoid vias. | N/A |
| VREG | 35 | Analog | O | The device requires an external capacitor on this pin to provide a regulated supply for the gate drivers of the buck and boost controllers. TI recommends capacitance on the order of 4.7 µF. The regulator obtains its power from either VIN or EXTSUP. This pin has current-limit protection; do not use it to drive any other loads. | Decouple with 3.3 µF to 10 µF, recommended is 4.7 µF; keep close to the IC with a low-impedance, low-inductance path. Avoid vias. | N/A |

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