

TPS22976 Dual-Channel Load Switch in Parallel Configuration

ABSTRACT

This application note demonstrates how to use the TPS22976 dual-channel load switch in parallel configuration to achieve lower R_{ON} and higher maximum continuous current. This configuration reduces power losses across the load switch and improves the overall system efficiency.

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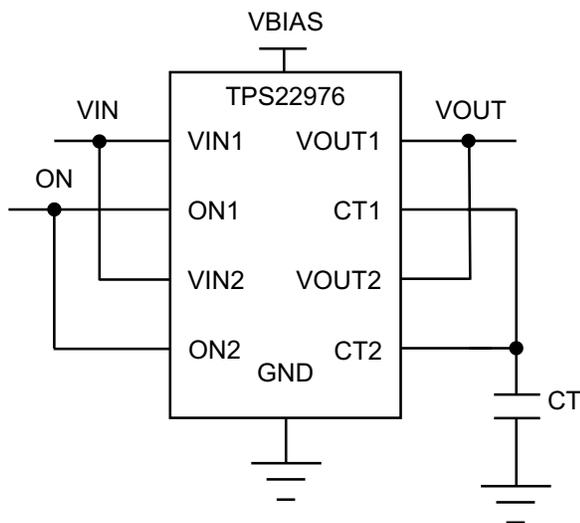
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1 Description

The TPS22976 is an 14-m Ω , 6-A per channel, dual-channel load switch with adjustable controlled turnon. The user reduces the R_{ON} by approximately 50% and increases the maximum continuous current to 10 A by connecting the two channels in parallel, forming a single channel.

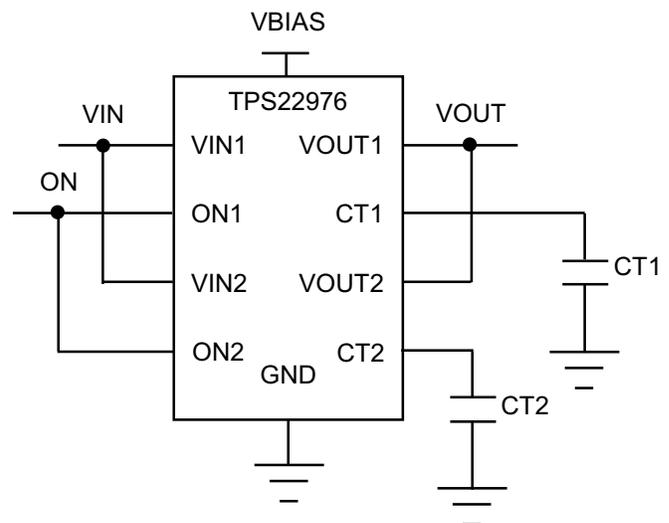
2 Setting up Dual-Channel Parallel Configuration

To configure the TPS22976 in parallel configuration, the user must tie together the corresponding pins of each channel, as shown in [Figure 1](#). This means connecting VIN1 and VIN2 for the input, ON1 and ON2 for the enable, and VOUT1 and VOUT2 for the output. The CT1 and CT2 pins can be tied together to use one capacitor, CT, as shown in [Figure 1](#). Otherwise, two separate capacitors of the same value, CT1 and CT2, can be used to connect to the individual CT pins as shown in [Figure 2](#).



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Figure 1. TPS22976 Parallel Configuration Circuit



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Figure 2. TPS22976 Parallel Configuration Circuit With Separate CT Capacitors

2.1 Operation

The ON1 and ON2 pins of the device must be tied together to ensure that both channels are controlled simultaneously. The tied ON pins control the state of the switch. Asserting ON holds the switch in the ON state. ON is active high and has a low-voltage threshold, thus making it able to interface with low-voltage signals and compatible with standard GPIO logic.

2.2 CT Capacitor Setup

The value of the capacitors attached to the CT pins affects the slew rate of the TPS22976, increasing or decreasing the rise time. If the user chooses to tie the CT pins together and use a single CT capacitor, as shown in [Figure 1](#), the resulting approximate rise times are listed in [Table 1](#).

Table 1. TPS22976 Parallel Configuration Rise Times Versus CT Capacitor Values

C _T (pF)	V _{OUT} Rise Time ⁽¹⁾ (μs)						
	V _{IN}						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.6 V
0 ⁽²⁾	115.5	87.26	56.67	55.48	47.65	42.04	32.98
220	279.7	194.9	127.8	109.9	92.06	81.08	46.99
470	462.8	322.5	183.2	161.5	126.5	107.7	80.6
1000	1029	652.2	387.7	331.3	271.1	257.2	156.2
2200	2008	1287	754.6	587.6	475.4	427.5	270.8
4700	3936	2666	1420	1245	1028	847.6	550.3
10000	7803	5150	3040	2562	2158	1795	1087

⁽¹⁾ 25°C, V_{OUT} = no load, C_{OUT} = 0.1 μF, 25 V X7R 10% ceramic capacitor.

⁽²⁾ C_T = 0 indicates that the CT capacitor is not populated.

The circuit in [Figure 1](#) has a rise time that is half of the rise-time value of the circuit in [Figure 2](#), assuming the capacitors tied to the CT pins have the same value (that is, CT = CT1 = CT2). Both channels of [Figure 1](#) will have less variation, thus allowing for a smoother curve. It is possible to leave the CT pins disconnected, which results in the rise times associated with CT = 0.

For the circuit in [Figure 2](#), the values of the capacitors must be identical to ensure proper operation. Two capacitors with different values will cause a non ideal start-up behavior that could damage the device. The rise times associated with the circuit in [Figure 2](#) are equivalent to the rise times associated with the single-channel configuration (see the *Adjustable Rise Time* table in the *Application Information* section of the TPS22976 data sheet, [TPS22976 5.7-V, 6-A, 14-mΩ On-Resistance Dual-Channel Load Switch](#)).

2.3 Parallel Configuration Versus Single-Channel Configuration Performance

The biggest differences in performance between the parallel configuration and the single-channel configuration are the R_{ON} and the maximum continuous current. When the two channels are connected in parallel, the R_{ON} of the device is reduced by approximately 50% and the maximum continuous current increases to 10 A. The rise time is also reduced by approximately 50% when the circuit is connected in the configuration shown in [Figure 1](#). Unlike a 50% reduction of the R_{ON} and rise times, the maximum continuous current does not double due to potential R_{ON} mismatch causing uneven current distribution between the channels.

3 Performance Data

Figure 3 through Figure 6 show the performance of the TPS22976 in parallel configuration.

3.1 TPS22976 Parallel Configuration R_{ON} Measurements

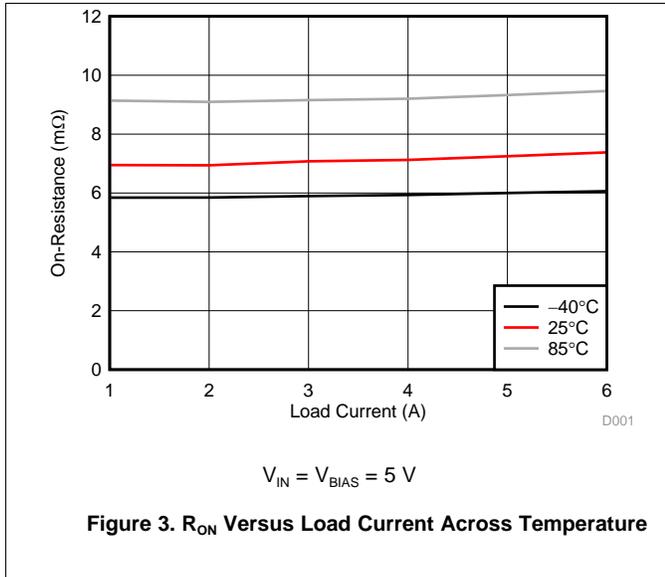


Figure 3. R_{ON} Versus Load Current Across Temperature

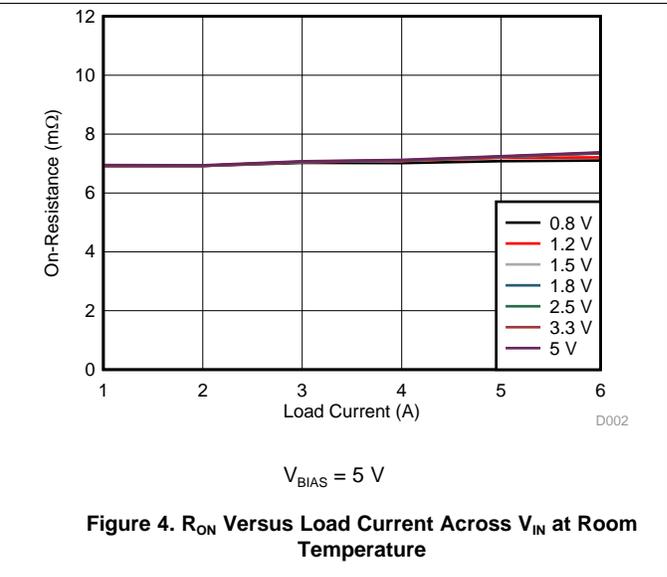


Figure 4. R_{ON} Versus Load Current Across V_{IN} at Room Temperature

3.2 TPS22976 Parallel Configuration Rise Time Measurements

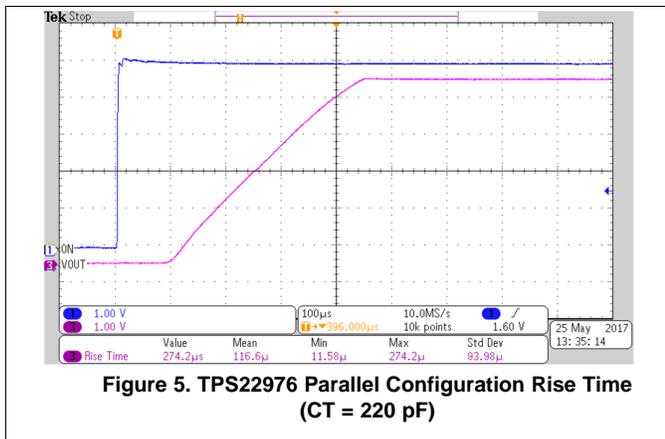


Figure 5. TPS22976 Parallel Configuration Rise Time (CT = 220 pF)

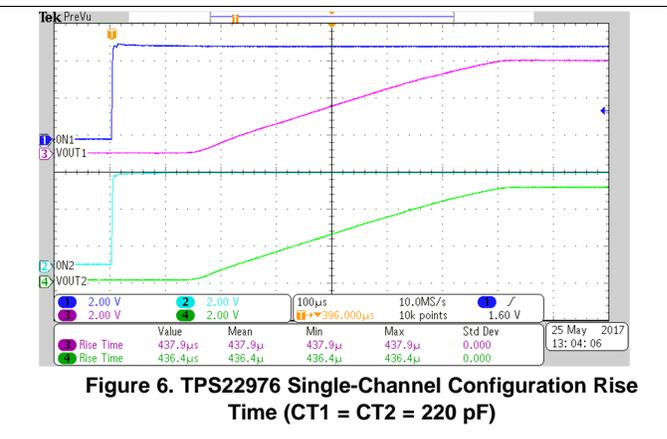


Figure 6. TPS22976 Single-Channel Configuration Rise Time (CT1 = CT2 = 220 pF)

4 Conclusion

Connecting the TPS22976 dual-channel load switch in parallel configuration reduces R_{ON} by approximately 50% to minimize power losses and improve system efficiency. Additionally, the maximum continuous current increases to 10 A and the rise time reduces by approximately 50% if the CT pins are tied together and a single CT capacitor is used.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (June 2015) to B Revision Page

- Changed the part number from TPS22066 to TPS22976 [2](#)
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Changes from Original (May 2013) to A Revision Page

- the last value of the C_T column from 1000 to 10 000 in the *TPS22976 Parallel Configuration Rise Times Versus C_T Capacitor Values* table [3](#)
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