Application Report
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Using the TPS62175 in an Inverting Buck Boost Topology

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ABSTRACT

The need to generate negative rails for electronic designs is a challenge that engineers face every day. This application report is a how-to guide on designing an inverting buck boost using the highly efficient TPS62175. Due to its wide operating input voltage range of 4.75 V to 28 V, it is ideal for inverting buck boost circuits powered from multi-cell batteries, AC adapters, and 12-V supplies.

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1 Inverting Buck Boost Topology

1.1 Concept

The inverting buck boost topology is very similar to the buck topology. In the buck configuration shown in Figure 1, the positive connection (V_{OUT}) is connected to the inductor and the return connection is connected to the integrated circuit (IC) ground. However, in the inverting buck boost configuration shown in Figure 2, the IC ground is used as the negative output voltage pin (labeled as $-V_{OUT}$). What used to be the positive output in the buck configuration is used as the ground (GND). This inverting topology allows the output voltage to be inverted and is always lower than the ground.

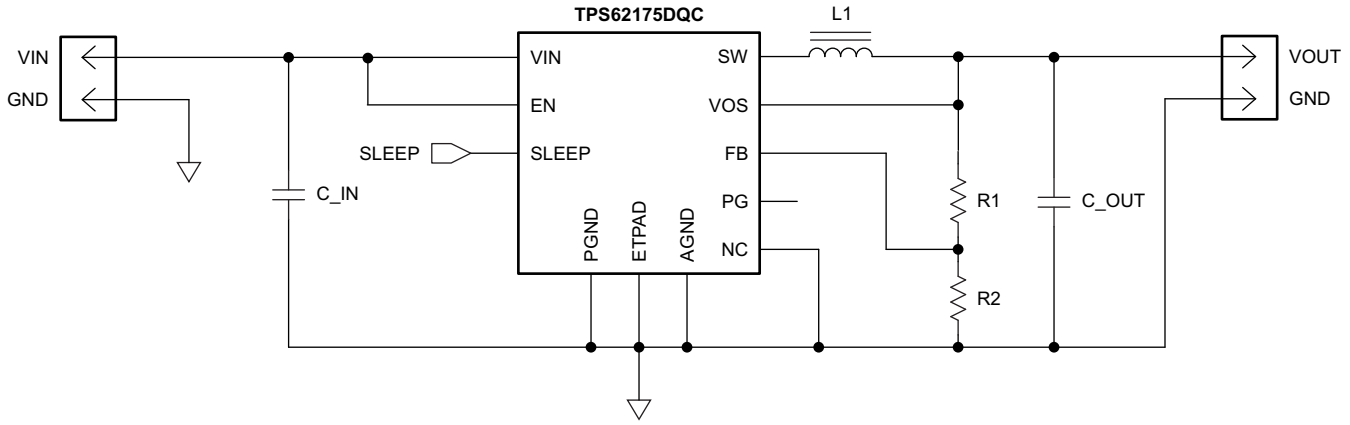


Figure 1. TPS62175 Buck Topology

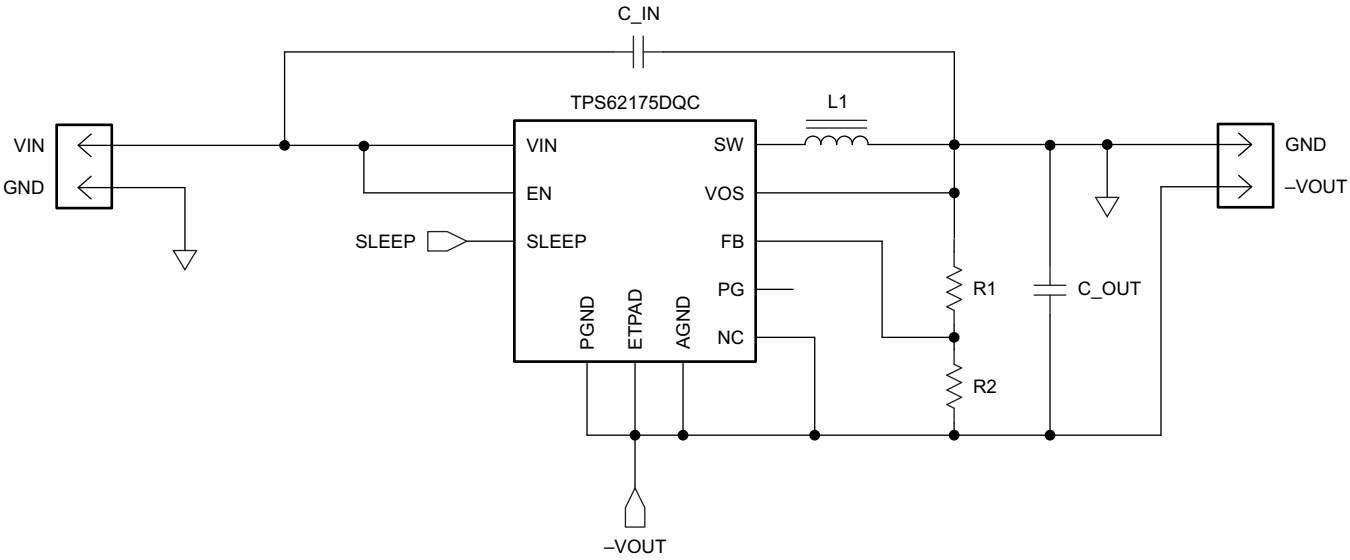


Figure 2. TPS62175 Inverting Buck Boost Topology

The circuit operation is different in the inverting buck boost topology than in the buck topology. Figure 3 (a) illustrates that the output voltage terminals are reversed, though the components are wired the same as a buck converter. During the on time of the control MOSFET, shown in Figure 3 (b), the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during that time. During the off time of the control MOSFET and the on time of the synchronous MOSFET, shown in Figure 3 (c), the inductor provides current to the load and the output capacitor. These changes affect many parameters described in the upcoming sections.

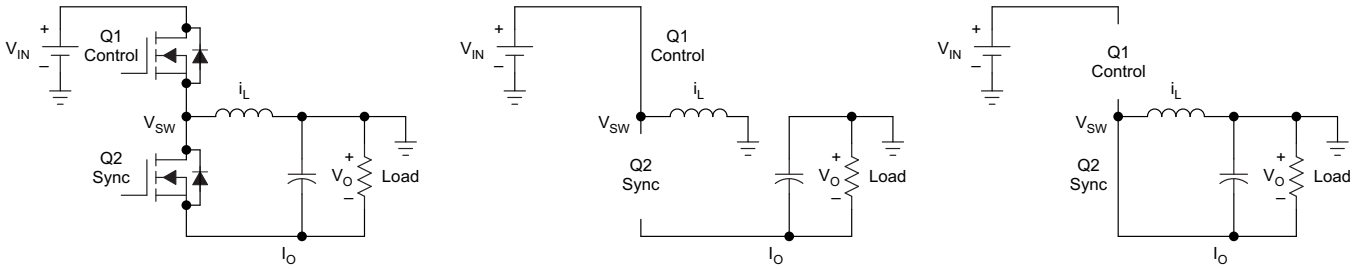


Figure 3. Inverting Buck Boost Configuration

1.2 Output Current Calculations

The average inductor current is affected in this topology. In the buck configuration, the average inductor current equals the average output current because the inductor always supplies current to the load during both the on and off times of the control MOSFET. However, in the inverting buck boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the on time of the control MOSFET. During the off time, the inductor connects to both the output cap and the load (see Figure 3). Knowing that the off time is 1-D of the switching period, then the average inductor current is:

$$I_{L(avg)} = \frac{I_{OUT}}{1-D} \tag{1}$$

The duty cycle for the typical buck converter is simply V_{OUT} / V_{IN} but the duty cycle for an inverting buck boost converter becomes:

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} \times \frac{1}{\eta} \tag{2}$$

The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. The peak to peak inductor ripple current is calculated as:

$$\Delta I_L = \frac{V_{IN} \times D}{f_s \times L} \tag{3}$$

Where,

ΔI_L (A): Peak to peak inductor ripple current

D: Duty cycle

η: Efficiency

f_s (MHz): Switching frequency

L (µH): Inductance

V_{IN} (V): Input voltage with respect to ground, instead of IC ground or V_{OUT}.

Finally, the maximum inductor current becomes:

$$I_{L(max)} = I_{L(avg)} + \frac{\Delta I_L}{2} \tag{4}$$

For an output voltage of –5 V, a 10-µH inductor, and an input voltage of 12 V, the following calculations produce the maximum allowable output current that can be delivered based on the minimum current limit value of 800 mA. The efficiency term is estimated at 80%.

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} \times \frac{1}{\eta} = \frac{-5}{-5-12} \times \frac{1}{0.8} = 0.368 \tag{5}$$

$$\Delta I_L = \frac{V_{IN} \times D}{f_s \times L} = \frac{12 \times (0.368)}{1MHz \times 10\mu H} = 441mA \quad (6)$$

Rearranging Equation 4 and setting $I_{L(max)}$ equal to the minimum value of I_{LIMF}, as specified in the datasheet, gives:

$$I_{L(avg)} = I_{L(max)} - \frac{\Delta I_L}{2} = 0.8 - \frac{0.441}{2} = 579mA \quad (7)$$

This result is then used in Equation 1 to calculate the maximum achievable output current:

$$I_{OUT} = I_{L(avg)} \times (1 - D) = 579mA \times (1 - 0.368) = 366mA \quad (8)$$

Table 1 provides several examples of the calculated maximum output currents for different output voltages (–1.8 V, –3.3 V and –5 V) based on an inductor value and switching frequency of 10 µH and 1 MHz, respectively. Increasing the inductance and/or input voltage allows higher output currents in the inverting buck boost configuration. The maximum output currents for the TPS62175 in the inverting buck boost topology are frequently lower than 500 mA due to the fact that the average inductor current is higher than that of a typical buck. The output current for the same three output voltages and different input voltages is displayed in Figure 4.

Table 1. Maximum Output Current Calculation for Different Values of V_{IN} and V_{OUT}

f_s (MHz)	1	1	1
V_{OUT} (V)	–5	–3.3	–1.8
L(µH)	10	10	10
V_{IN} (V)	12	12	12
$I_{L(max)}$ (A)	0.8	0.8	0.8
η	0.8	0.8	0.8
D	0.368	0.270	0.163
ΔI_L (mA)	441	324	196
$I_{L(avg)}$ (mA)	579	638	702
I_{OUT} (mA)	366	466	588

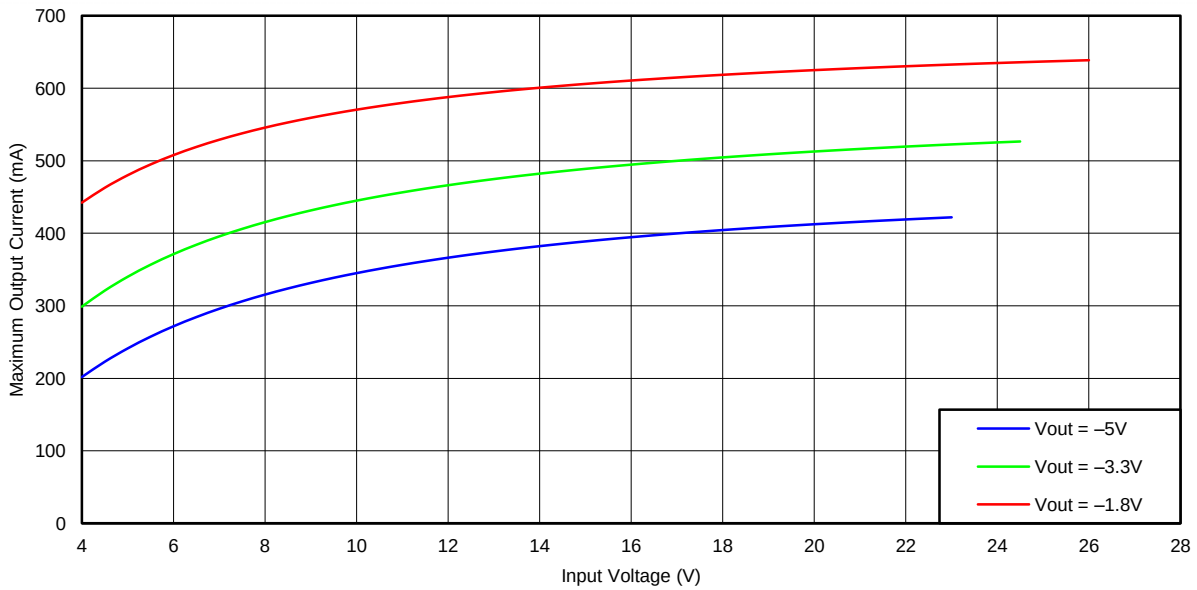


Figure 4. Maximum Output Current vs. V_{IN}

1.3 V_{IN} and V_{OUT} Range

The input voltage that can be applied to an inverting buck boost converter IC is less than the input voltage that can be applied to the same buck converter IC. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT}, not V_{IN} to ground. Thus, the input voltage range of the TPS62175 is 4.75 V to 28 + V_{OUT}, where V_{OUT} is a negative value.

The output voltage range is the same as when configured as a buck converter, but negative. The output voltage for the inverting buck boost topology should be set between –1 V and –6 V. It is set the same way as in the buck configuration, with two resistors connected to the FB pin. Due to the increased noise of the inverting buck boost topology and for a more robust design, use smaller value resistors than are used for the buck configuration.

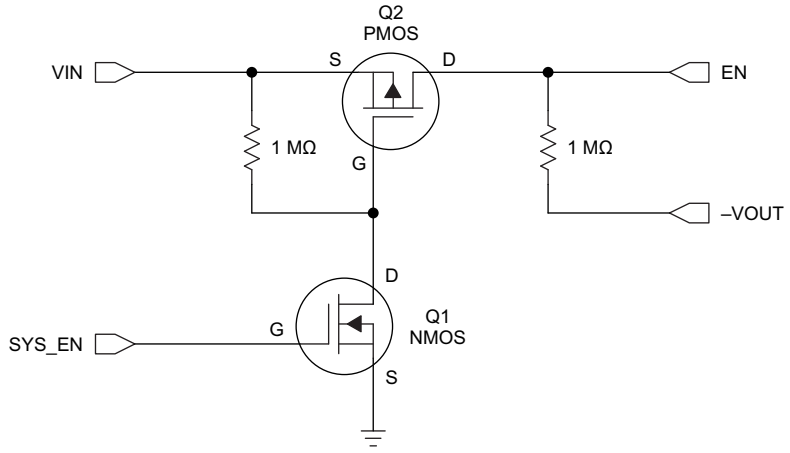
2 Digital Pin Configurations

2.1 Enable Pin

The device is enabled once the voltage at the EN pin trips its threshold and the input voltage is above the UVLO threshold. The TPS62175 stops operation once the voltage on the EN pin falls below its threshold or the input voltage falls below UVLO threshold.

Because V_{OUT} is the IC ground in this configuration, the EN pin must be referenced to V_{OUT} instead of ground. In the buck configuration, 0.9 V is considered high and less than 0.3 V is considered a low. In the inverting buck-boost configuration, however, the V_{OUT} voltage is the reference; therefore, the high threshold is 0.9 V + V_{OUT} and the low threshold is 0.3 V + V_{OUT}. For example, if V_{OUT} = –5 V, the V_{EN} is considered at a high level for voltages above –4.1 V and at a low level for voltages below –4.7 V.

This behavior can cause difficulties enabling or disabling the part, since in some applications, the IC providing the EN signal may not be able to produce negative voltages. The level shifter circuit shown in Figure 5 alleviates any difficulties associated with the offset EN threshold voltages by eliminating the need for negative EN signals. If disabling the TPS62175 is not desired, the EN pin may be directly connected to V_{IN} without this circuit.



VOUT is the negative output voltage of the inverting buck-boost converter

Figure 5. EN Pin Level Shifter

The positive signal that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN grounded), Q2 sees 0 V across its VGS, and also remains off. In this state, the EN pin sees –5 V which is below the low level threshold and it disables the device.

When SYS_EN provides enough positive voltage to turn Q1 on (V_{GS} threshold as specified in the MOSFET datasheet), the gate of Q2 sees ground through Q1. This drives the V_{GS} of Q2 negative and turns Q2 on. Now, V_{IN} ties to EN through Q2 and the pin is above the high level threshold, turning the device on. Be careful to ensure that the V_{GD} and V_{GS} of Q2 remain within the MOSFET ratings during both the enabled and disabled states. Failing to adhere to this constraint can result in damaged MOSFETs.

The enable and disable sequence is illustrated in Figure 6. The SYS_EN signal activates the enable circuit, and the GD NODE signal represents the shared node between Q1 and Q2. This circuit was tested with a 1.8-V SYS_EN signal and dual N/PFET Si1029X. The EN signal is the output of the circuit and goes from V_{IN} to $-V_{OUT}$ properly enabling and disabling the device.

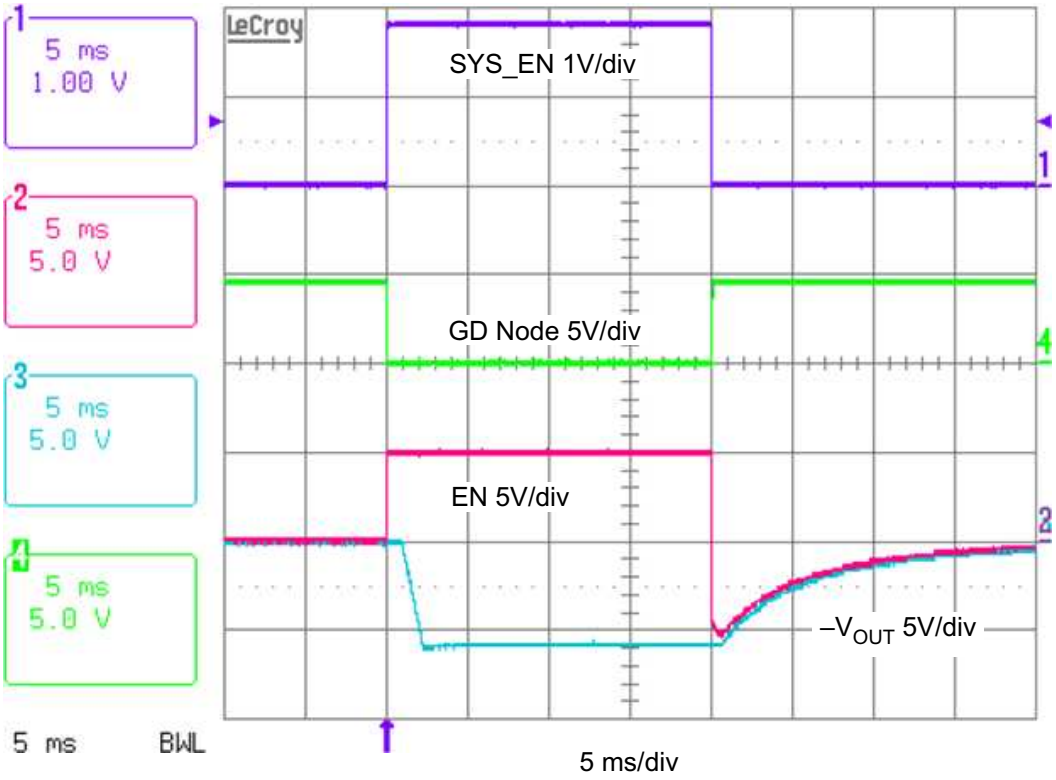


Figure 6. EN Pin Level Shifter Test Results

2.2 SLEEP Pin

The TPS62175 offers a sleep mode that can be activated by pulling the SLEEP pin low if the device goes into a low load current mode (for example, less than 10 mA). The internal circuitry that stays active in sleep mode draws a quiescent current of typically less than 5 µA which increases the efficiency.

Because V_{OUT} is the IC ground in this configuration, the SLEEP pin must be referenced to V_{OUT} instead of ground. In the buck configuration, 0.9 V is considered high and less than 0.3 V is considered a low. In the inverting buck-boost configuration, however, the V_{OUT} voltage is the reference; therefore, the high threshold is 0.9 V + V_{OUT} and the low threshold is 0.3 V + V_{OUT}. For example, if V_{OUT} = –5 V, the V_{SLEEP} is considered at a high level for voltages above –4.1 V and at a low level for voltages below –4.7 V.

This behavior can cause difficulties enabling or disabling sleep mode, since in some applications, the IC providing the sleep signal may not be able to produce negative voltages. The level shifter circuit shown in Figure 7 alleviates any difficulties associated with the offset SLEEP pin threshold voltages by eliminating the need for negative sleep signals. If enabling sleep mode is not desired, the SLEEP pin may be directly connected to ground without this circuit. Note that to avoid violating its absolute maximum rating, the SLEEP pin should not be driven more than 7 V above the negative output voltage (IC ground).

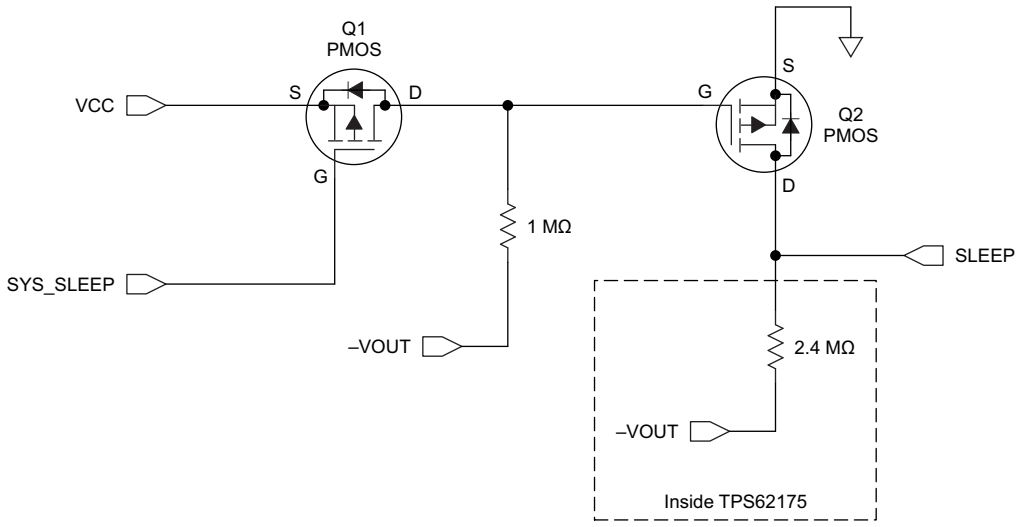


Figure 7. SLEEP Pin Level Shifter

The positive signal that originally drove the SLEEP pin is instead tied to the gate of Q1 (SYS_SLEEP). When Q1 is off (SYS_SLEEP at V_{CC} voltage), Q2 sees $-V_{OUT}$ across its V_{GS} and turns on. In this state, the SLEEP pin sees ground, which is above the high level threshold and disables sleep mode. Note that the VCC voltage must be at the same logic high level as the SYS_SLEEP signal.

When SYS_SLEEP is at ground potential, providing enough voltage to turn Q1 on (V_{GS} threshold as specified in the MOSFET datasheet), the gate of Q2 sees V_{CC} through Q1. This drives the V_{GS} of Q2 positive and turns Q2 off. Now, the SLEEP pin is pulled down by its internal pulldown resistor and sleep mode is enabled with this logic low. Depending on the leakage current of Q2, an additional pulldown resistance of around 100 kΩ may be needed to pull the SLEEP pin low enough. Be careful to ensure that the V_{GD} and V_{GS} of Q2 and Q1 remain within the MOSFET ratings during both the enabled and disabled states of the sleep mode. Failing to adhere to this constraint can result in damaged MOSFETs.

The sleep mode enable and disable sequence is illustrated in Figure 8. The SYS_SLEEP signal activates the sleep mode enable circuit, and the GD NODE signal represents the shared node between Q1 and Q2. Sleep mode operation is indicated by a higher inductor current than in normal mode at the left and right sides of the graph. This circuit was tested with a V_{CC} of 1.8 V and dual PFET FDG6318P. The SYS_SLEEP net is the input of the circuit and goes between ground and 1.8 V, and is easily driven by a separate device.

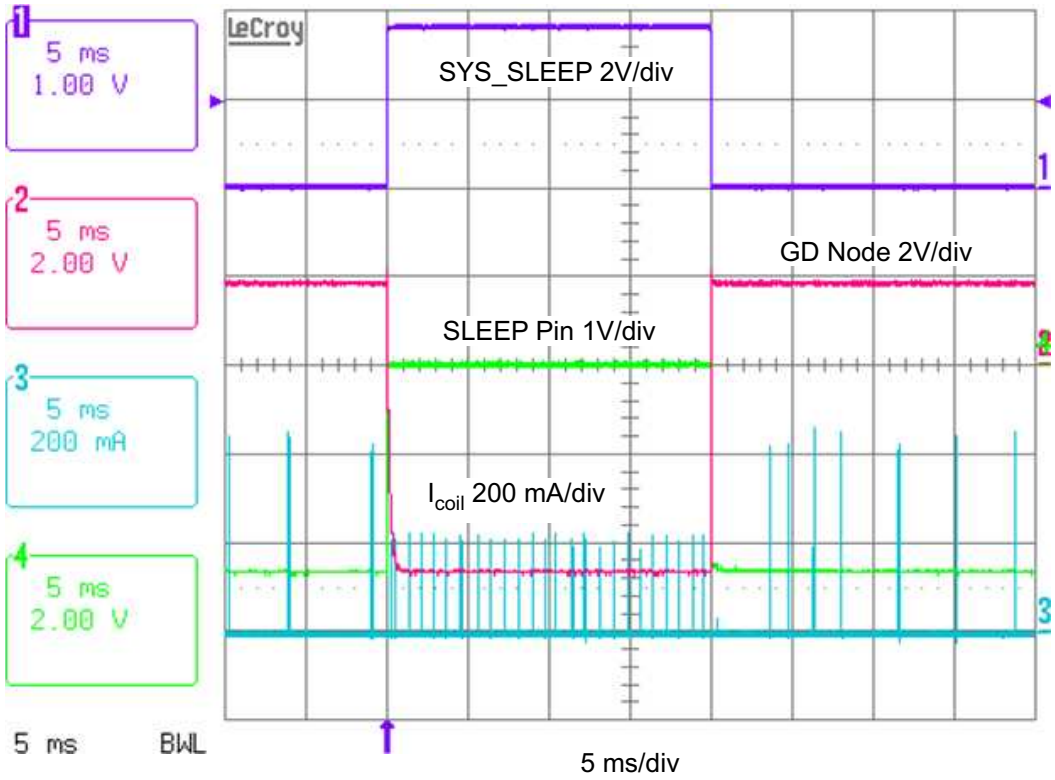


Figure 8. SLEEP Pin Level Shifter Test Results

As with the sleep mode operation as a buck converter on the TPS62175 device, the output current supported in sleep mode is also limited in the inverting buck boost topology. There is no closed form equation for computing the available output current in sleep mode, but generally at least 10 mA of current is supported in the inverting buck boost topology.

2.3 Power Good Pin

The TPS62175 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because V_{OUT} is the IC ground in this configuration, the PG pin is referenced to V_{OUT} instead of ground, which means that the TPS62175 pulls PG to V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PG pin may not be able to withstand negative voltages. The level shifter circuit shown in Figure 9 alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not needed, it may be left floating or connected to V_{OUT} without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin should not be driven more than 7 V above the negative output voltage (IC ground).

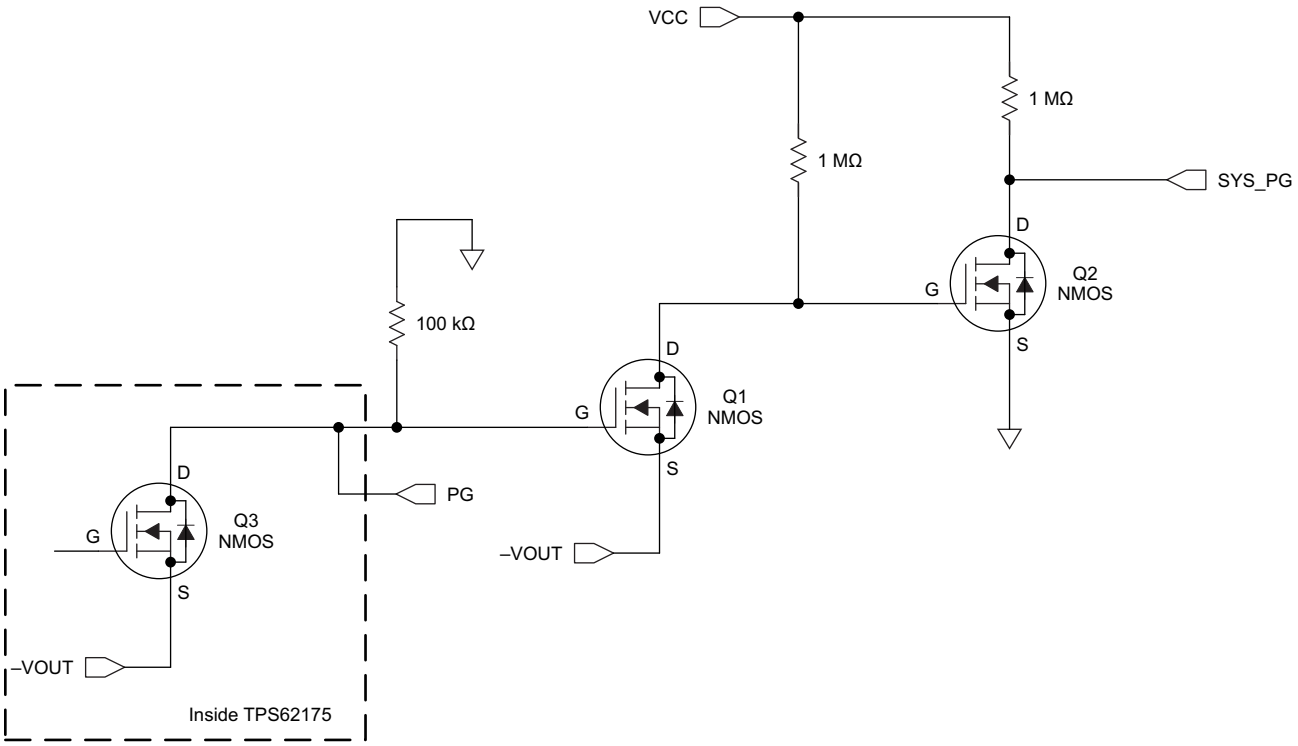


Figure 9. PG Pin Level Shifter

Inside the TPS62175, the PG pin is connected to an N-channel MOSFET (Q3). By tying the PG pin to the gate of Q1, when the PG pin is pulled low, Q1 is off and Q2 is on because its V_{GS} sees V_{CC}. SYS_PG is then pulled to ground.

When Q3 turns off, the gate of Q1 is pulled to ground potential turning it on. This pulls the gate of Q2 below ground, turning it off. SYS_PG is then pulled up to the V_{CC} voltage. Note that the V_{CC} voltage must be at an appropriate logic level for the circuitry connected to the SYS_PG net.

This PG pin level shifter sequence is illustrated in Figure 10 and Figure 11. The PG signal activates the PG pin level shifter circuit, and the GD node signal represents the shared node between Q1 and Q2. This circuit was tested with a V_{CC} of 1.8 V and dual NFET Si1902DL. The SYS_PG net is the output of the circuit and goes between ground and 1.8 V, and is easily read by a separate device.

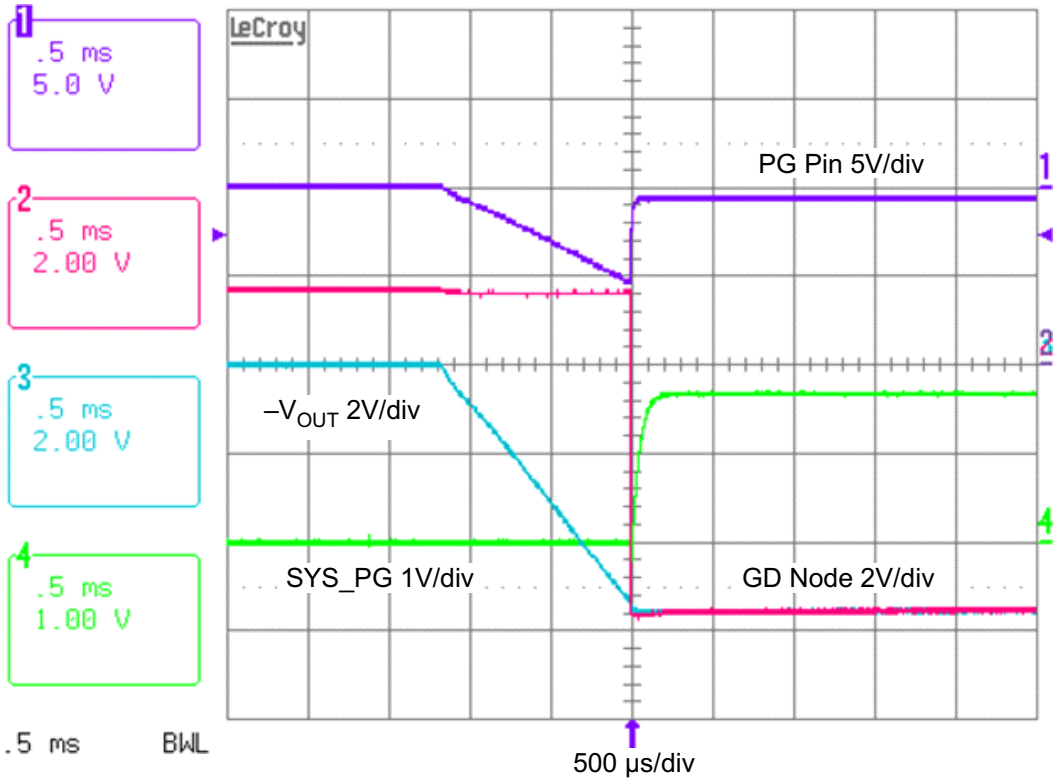


Figure 10. PG Pin Level Shifter on Startup

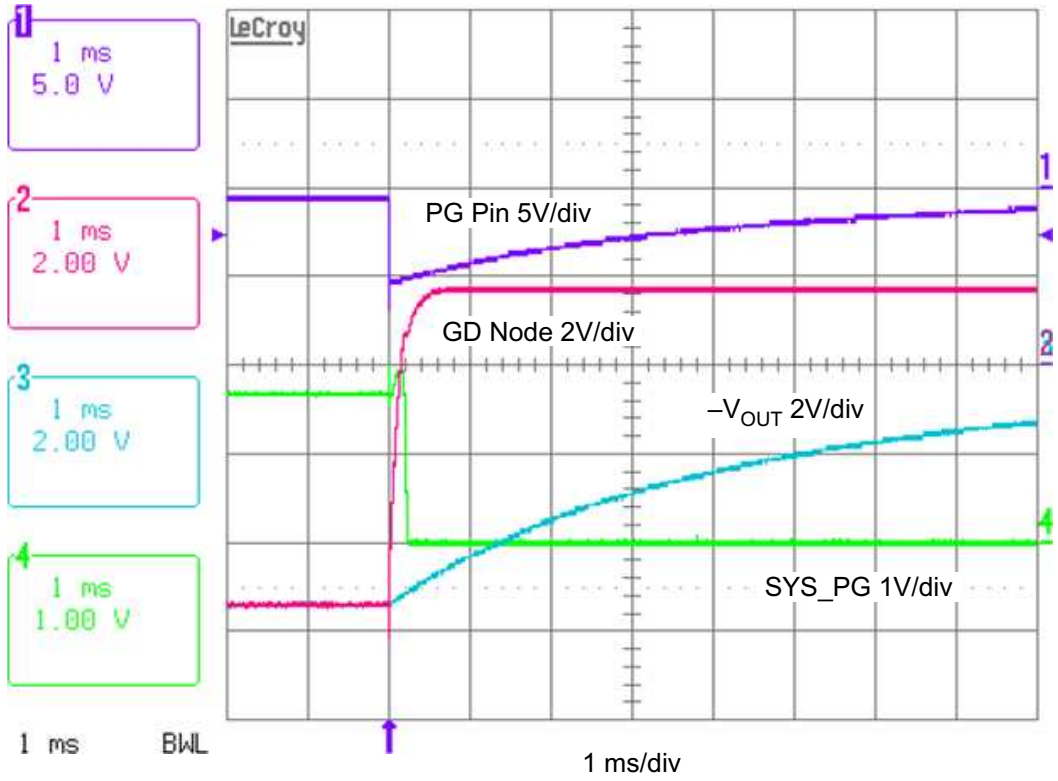


Figure 11. PG Pin Level Shifter on Shutdown

3 Startup Behavior and Switching Node Consideration

Figure 12 shows the startup behavior in the inverting configuration. After EN is taken high, the device starts switching after about a 1-msec delay. Until the output voltage enters regulation, the device switches with its reduced startup current limit. The inductor current going higher at the right side of the graph indicates that regulation is reached and the current limit is increased to the full value. Due to the higher peak currents in the inverting topology, current limit is frequently reached during startup. This is acceptable as long as the saturation current of the inductor is chosen appropriately.

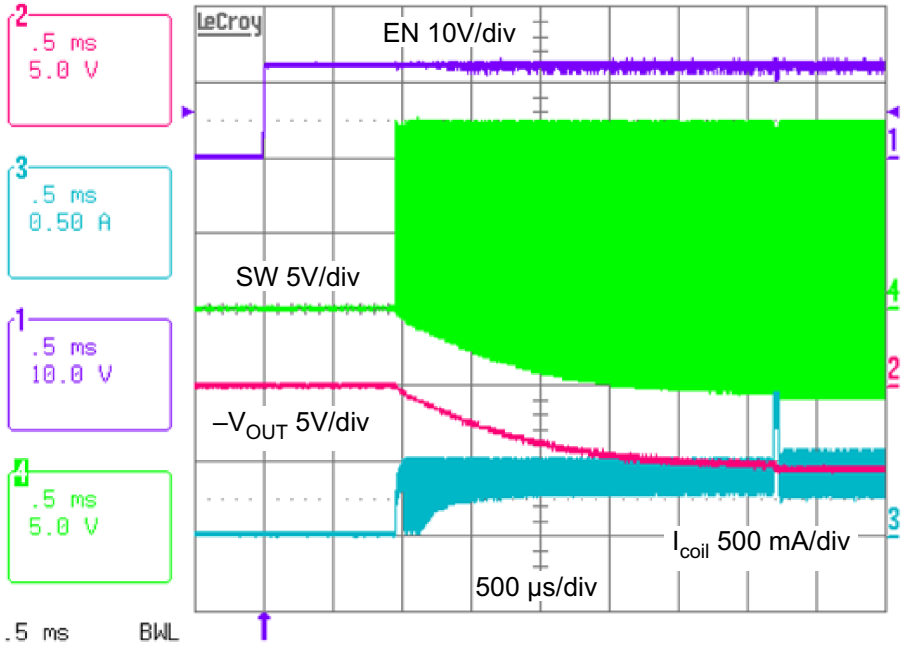


Figure 12. Startup on EN with 250-mA Load

Figure 12 also shows the SW node voltage as the device starts up. The voltage on the SW pin switches from VIN to V_{OUT}. As the high-side MOSFET turns on, the SW node sees the input voltage and as the low-side MOSFET turns on, the SW node sees the IC ground, which is the output voltage. As V_{OUT} continues to ramp down, the SW node low level follows it down.

4 External Component Selection

The inductor and output capacitor need to be selected based on the needs of the application and the stability criteria of the device. The selection criterion for the inductor and output capacitor is different from the buck converter. See Selecting L and Cout for Stability for a discussion of stability.

4.1 Inductor Selection

When selecting the inductor value for the inverting buck boost topology, the equations provided in the Output Current Calculations section should be used instead of the ones provided in the data sheet. These equations help to select the right inductance by designing for a maximum inductor current ($I_{L(max)}$) or finding the peak inductor current for a given inductance. $I_{L(max)}$ should be kept below the minimum current limit value of the device (0.8 A) for a reliable design. The worst case $I_{L(max)}$ occurs at the minimum V_{IN} of the design. It is recommended to size the inductor for the current limit level of the TPS62175, as this level is sometimes reached during startup (shown in Figure 12 above). See Selecting L and Cout for Stability for the stability impact of the inductor selection.

4.2 Input Capacitor Selection

An input capacitor, C_{IN}, is required to provide a local bypass for the input voltage source. A low ESR input capacitor is best for input voltage filtering and minimizing interference with other circuits. For most applications, a 2.2-µF ceramic capacitor is recommended from V_{IN} to ground. The C_{IN} capacitor value can be increased without any limit for better input voltage filtering.

For the inverting buck boost configuration of the TPS62175, it is not recommended to install a capacitor from V_{IN} to V_{OUT}. Such a capacitor, if installed, provides an AC path from V_{IN} to V_{OUT}. When V_{IN} is applied to the circuit, this dV/dt across a capacitor from V_{IN} to V_{OUT} creates a current that must return to ground (the return of the input supply) to complete its loop. This current might flow through the internal low-side MOSFET's body diode and the inductor to return to ground. Flowing through the body diode pulls the SW pin and VOS pin more than 0.3 V below IC ground, violating their absolute maximum rating. Such a condition might damage the TPS62175 and is not recommended. Therefore, a capacitor from V_{IN} to V_{OUT} is not needed or recommended. If such a capacitor (C_BYP) is present, then a Schottky diode should be installed on the output, per Figure 13. Startup testing should be conducted to ensure that the VOS pin is not driven more than 0.3 V below IC ground when V_{IN} is applied.

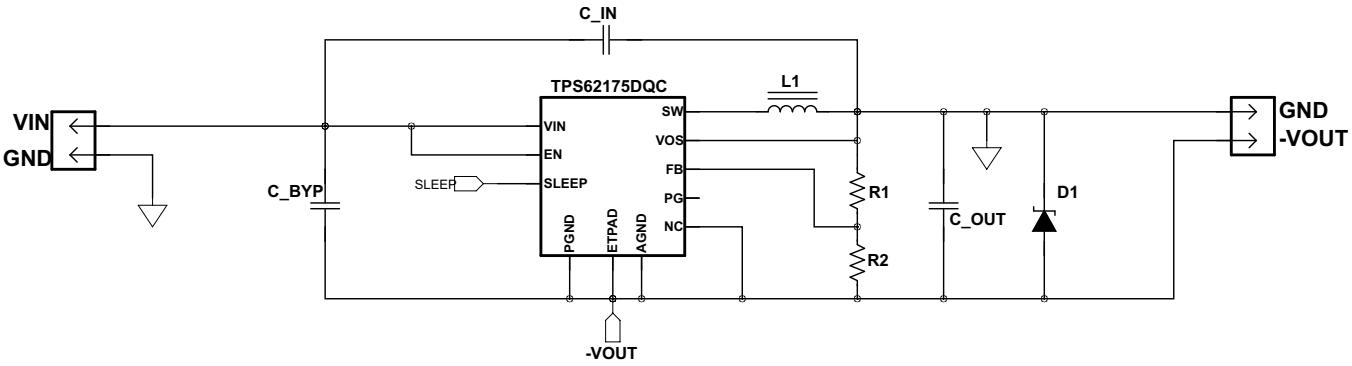


Figure 13. If Installing C_BYP, Installing Schottky D1 is Required

4.3 Selecting L and C_{OUT} for Stability

The switch node, inductor current, and the output voltage ripple during steady state are signals that need to be checked first for the stability of the system. Oscillations on the output voltage and the inductor current, and jitter on the switch node are good indicators of the instability of the system. Figure 22 shows both the switch node and output voltage ripple of this topology. Load transient response is another good test for stability, as described in the SLVA381 application report.

The recommended inductance and capacitance values to use for this topology are in the range of 10 µH to 22 µH and from 47 µF to 100 µF, respectively. In this application report, a 10-µH inductor and a 47-µF capacitor are used.

The inverting buck boost topology contains a Right Half Plane (RHP) zero which significantly and negatively impacts the control loop response by adding an increase in gain along with a decrease in phase at a high frequency. This can cause instability. Equation 9 estimates the frequency of the RHP zero.

$$f_{(RHP)} = \frac{-(1-D)^2 \times V_{OUT}}{(D \times L \times I_{OUT} \times 2 \times \pi)} \quad (9)$$

It is recommended to keep the loop crossover frequency to 1/10th of the RHP zero frequency. Doing this requires either decreasing the inductance to increase the RHP zero frequency or increasing the output capacitance to decrease the crossover frequency. Note that the RHP zero frequency occurs at lower frequencies with lower input voltages, which have a higher duty cycle. A larger output capacitance is recommended for low input (< 12 V) voltage designs. SLVA465 explains how to measure the control loop of a DCS-Control™ device while Figure 14 shows the bode plot of Figure 15.

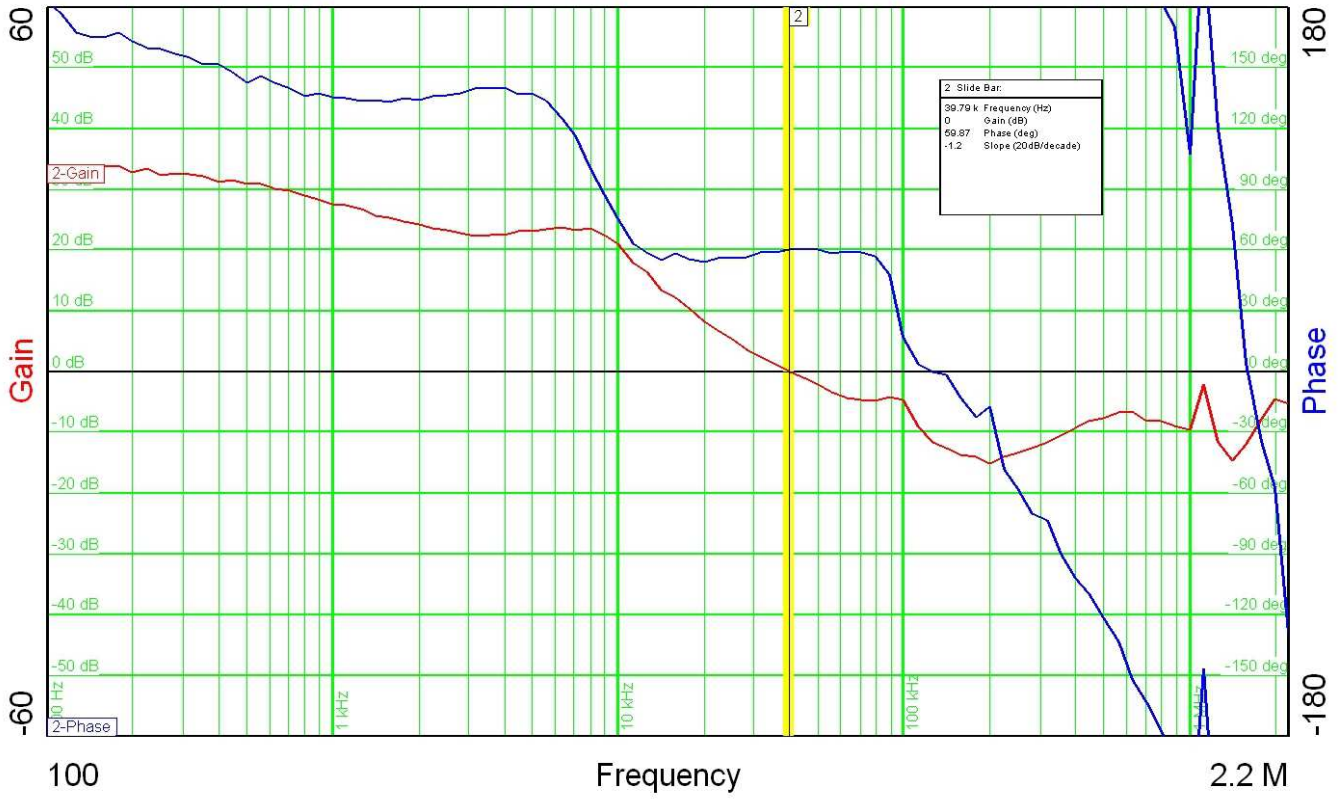


Figure 14. Bode Plot at 12-V V_{IN} and 400-mA Load

5 Typical Performance and Waveforms

The application circuit shown in Figure 15 is used to generate the data presented in Figure 16 – Figure 22. For Figure 16 (normal mode efficiency), L1 is a 10-µH 744 778 510 inductor from Wurth, whereas a 10-µH LPS4012-103ML from Coilcraft is used for Figure 17 (sleep mode efficiency). The output capacitor used is a 47-µF, 16-V, 1210, X5R ceramic capacitor. For a 5-V output, loss of capacitance from the DC bias effect can be significant. Unless otherwise specified, V_{IN} = 12 V and V_{OUT} = –5 V.

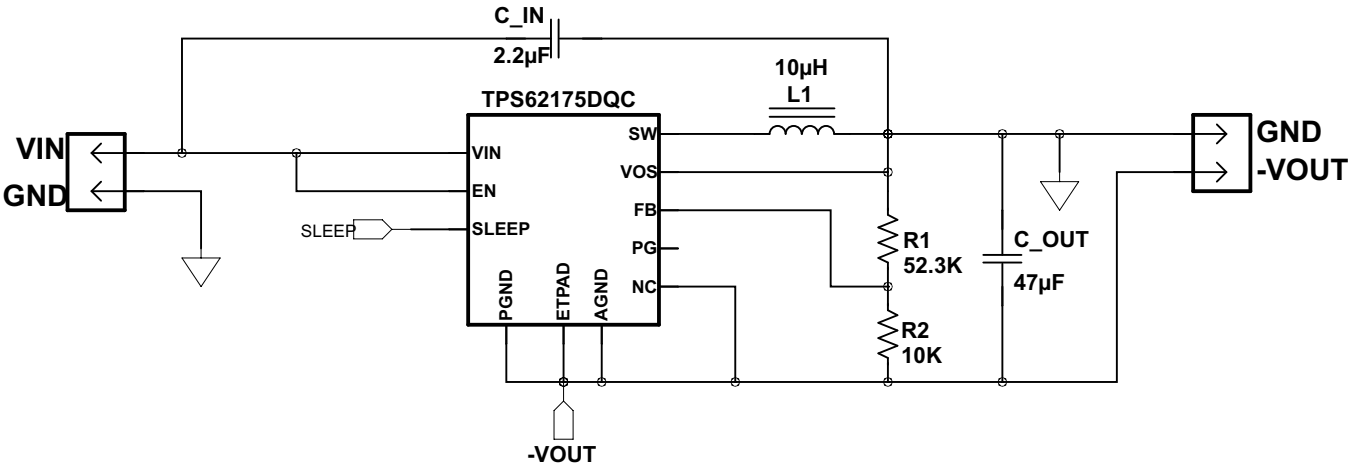


Figure 15. Schematic of Tested Circuit

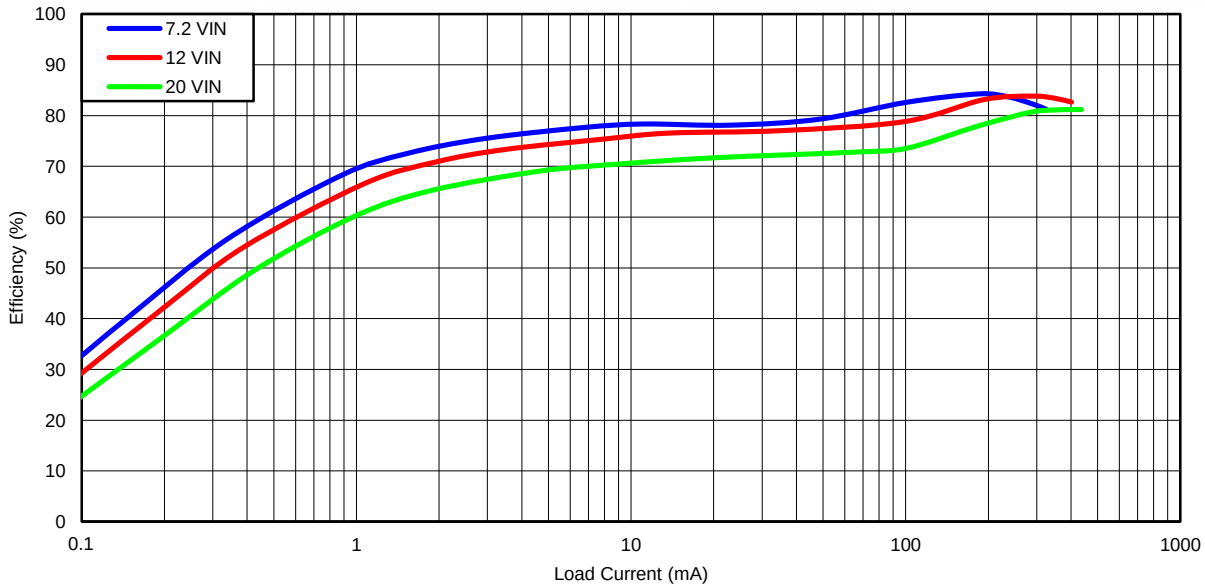


Figure 16. Normal Mode Efficiency vs. Load Current with V_{OUT} = –5 V

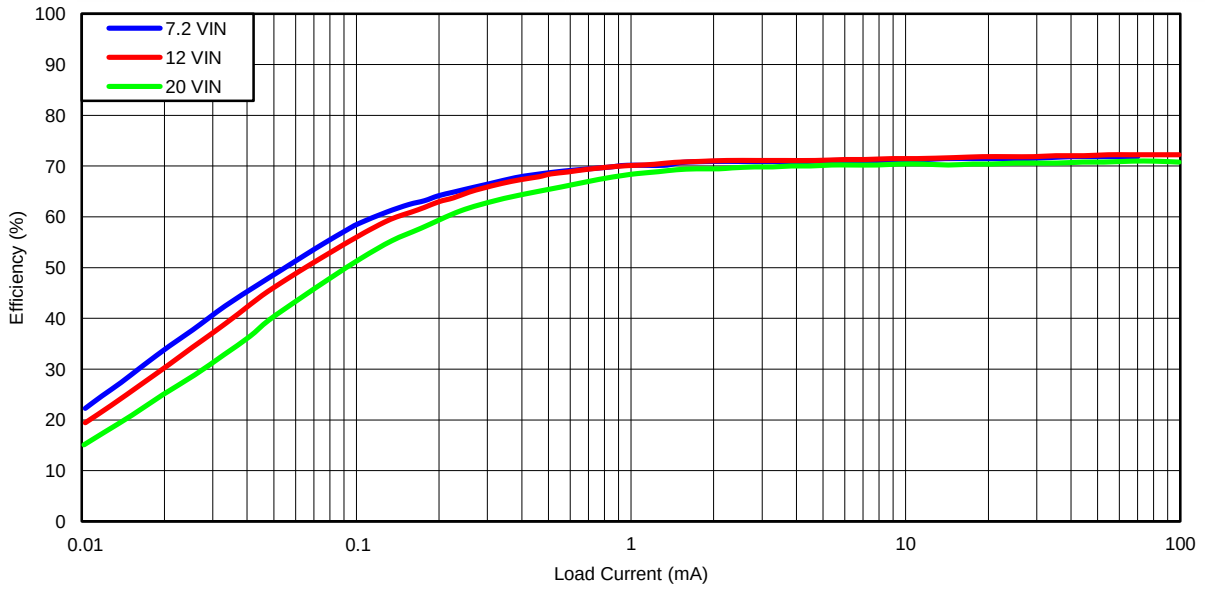


Figure 17. Sleep Mode Efficiency vs. Load Current with V_{OUT} = –5 V

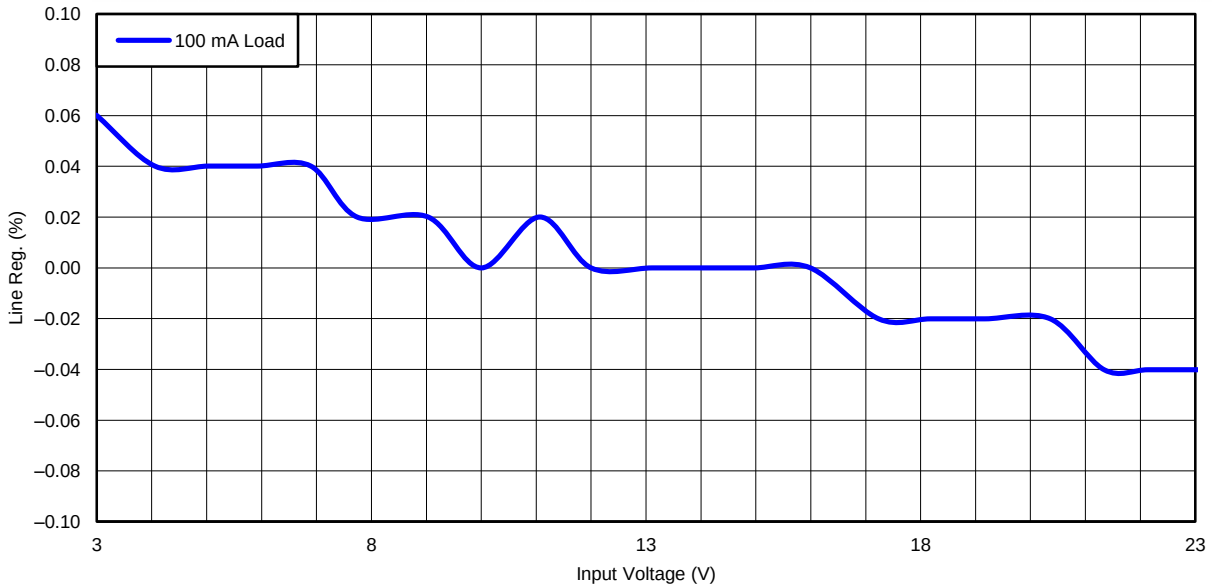


Figure 18. Line Regulation with V_{OUT} = –5 V and 100-mA Load

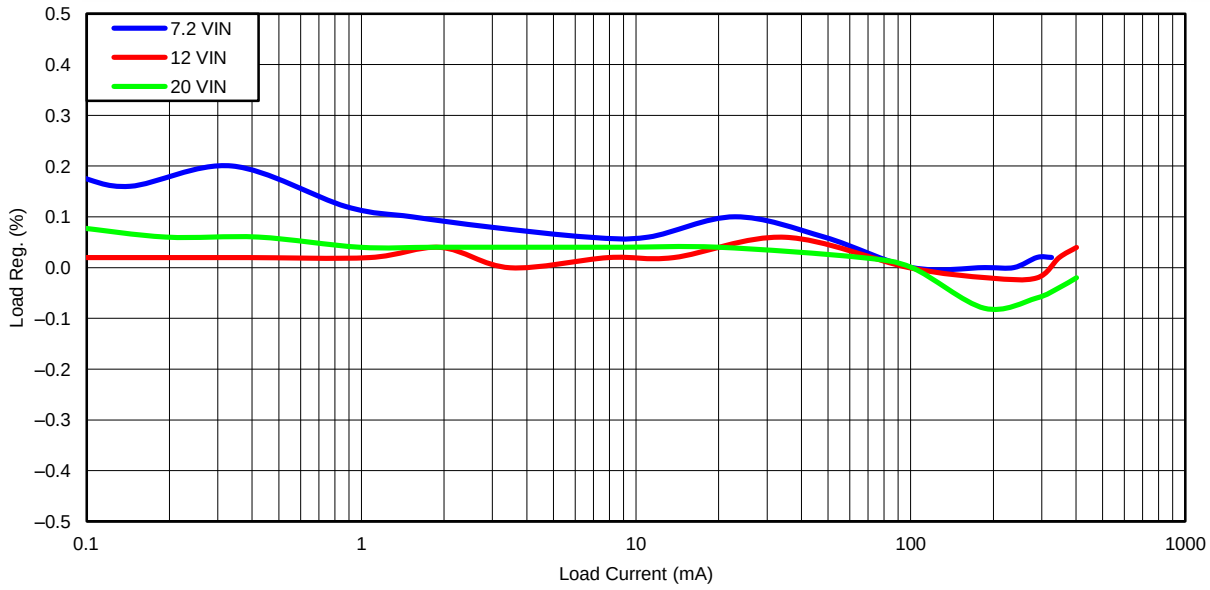


Figure 19. Load Regulation with V_{OUT} = –5 V

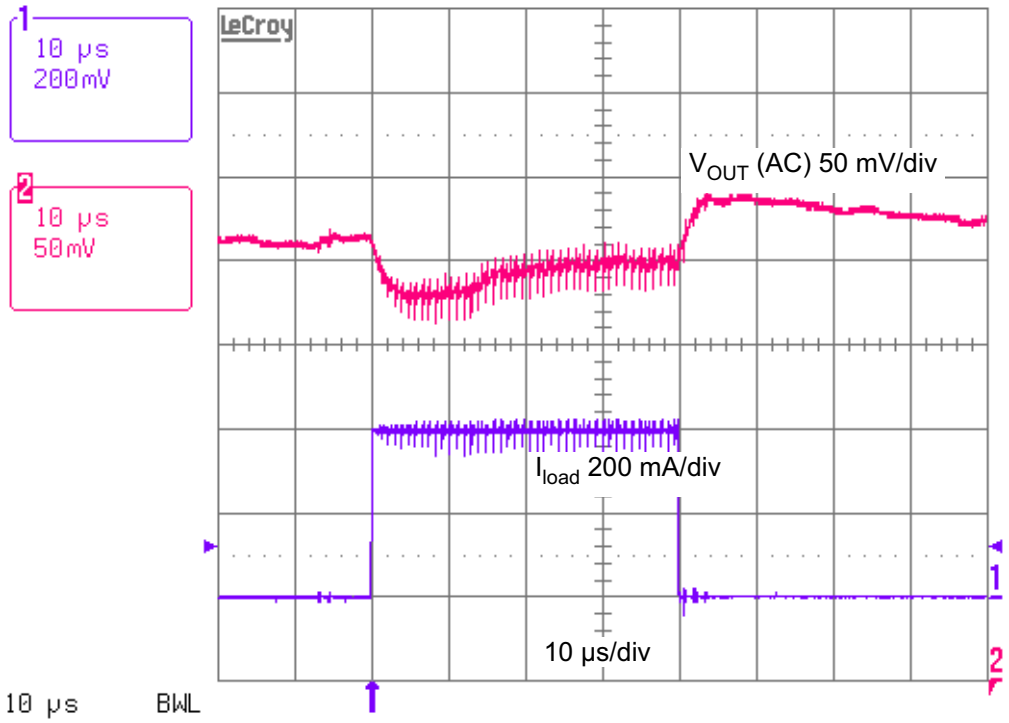


Figure 20. Load Transient Response 10 mA to 400 mA with V_{IN} = 12 V

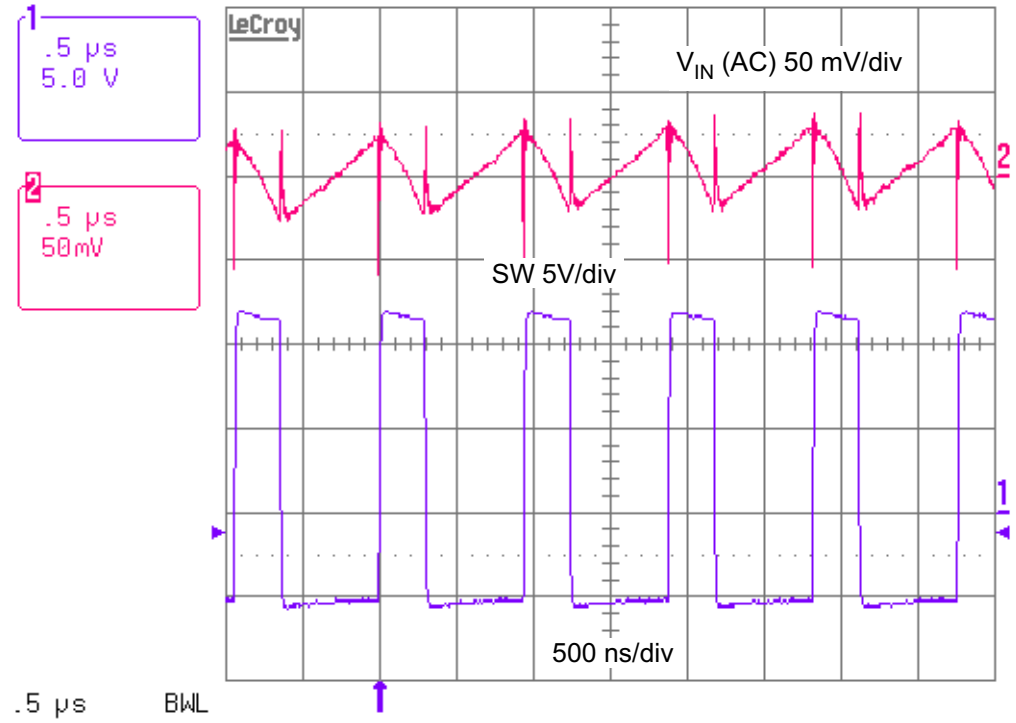


Figure 21. Input Voltage Ripple, V_{IN} = 12 V and I_{OUT} = 400 mA

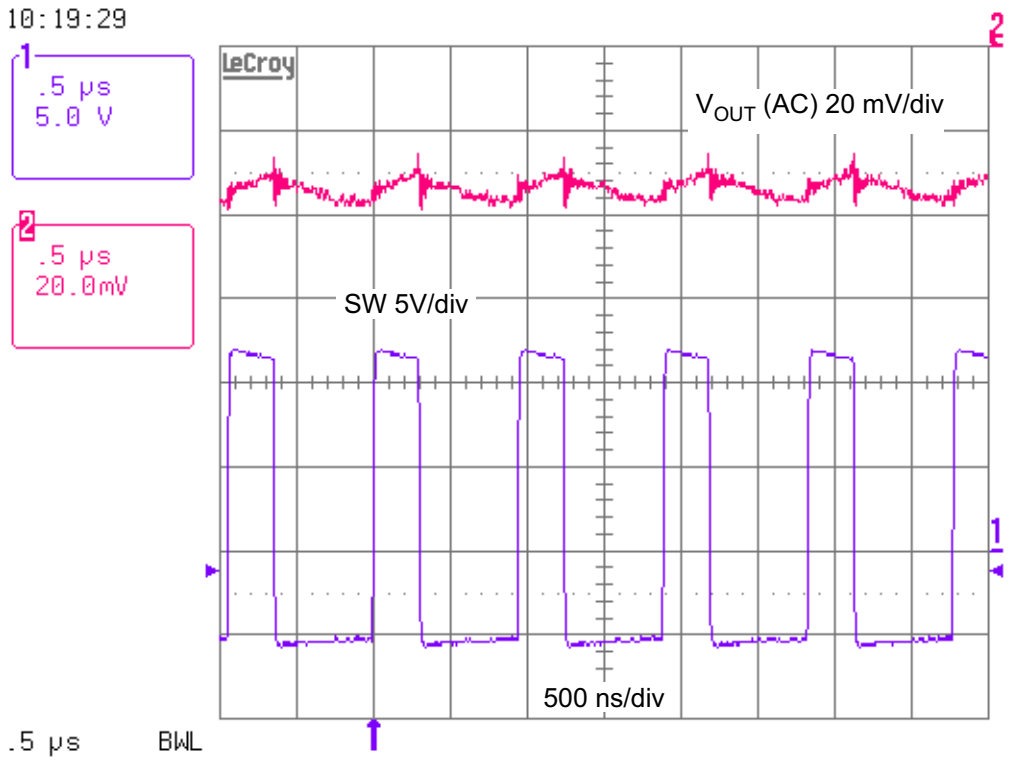


Figure 22. Output Voltage Ripple, V_{IN} = 12 V and I_{OUT} = 400 mA

6 Conclusion

The TPS62175 can be configured as an inverting buck boost converter to generate a negative output voltage. The inverting buck boost topology changes some system characteristics, such as input voltage range and maximum output current. This application report explains the inverting buck boost topology and how to select the external components with the changed system characteristics. Measured data from the example design is provided.

7 References

1. *Creating an Inverting Power Supply From a Step-Down Regulator* (SLVA317)
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3. *Using a Buck Converter in an Inverting Buck-Boost Topology* (SLYT286)
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7. *How to Measure the Control Loop of DCS-Control™ Devices* (SLVA465)
8. *Simplifying Stability Checks* (SLVA381)
9. DCS-Control™ Landing Page: www.ti.com/dcs-control

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