Application Report
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Powering the TMS320DM365 using the TPS650061

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ABSTRACT

The TMS320DM365 processor requires a specific power-on and power-off sequence for reliable operation. This sequence is described and an inexpensive, discrete sequencing solution is provided. This sequence uses the TPS650061 Power Management integrated circuit (IC). The circuit can be adapted for other Power Management ICs and processors as well.

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1 TPS650061 Overview

The TPS650061 is a versatile, high-efficiency power management IC that is designed with portable applications in mind. It incorporates a single 2.25-MHz step-down switching regulator and two low-dropout (LDO) regulators in a compact 3 mm × 3 mm QFN package.

Power-sequencing with the TPS650061 is simplified since the switching regulator and LDOs have independent voltage inputs and enable controls. The device further extends functionality by adding a Supply Voltage Supervisor (SVS) circuit which is used to release the $\overline{\text{RESET}}$ pin of the load processor when the supply rails have reached minimum regulation.

2 TMS320DM365 Power Requirements

Some of the power requirements are dependent on the processor operating frequency and user preference (for example, the VDD_AEMIF1_18_33 supply can operate at 1.8 V or 3.3 V). Further information on voltage tolerance and maximum current requirements is found on the TI Processor Power Management website at www.ti.com/processorpower.

Table 1. Power Summary for TMS320DM365 Processor

Rail Name	Voltage (V)	Imax (mA)	Tolerance (%)	Power On	Power Off
CVDD, VDD12_PRTCSS, VDDA12_DAC, VPP	1.2	650	±5	First	Third
VDDS18, VDD18_PRTCSS, VDDMXI, VDD18_SLDO, VDD18_DDR, VDDA18_PLL, VDDA18_USB, VDDA18_ADC, VDDA18_DAC	1.8	95	±5	Second	Second
VDDS33, VDDA33_USB, VDDA33_VC, VDD_AEMIF1_1_18_3_3, VDD_AEMIF2_18_3_3, VDD_ISIF18_33	3.3	126	±5	Third	First

The TPS650061 meets these power requirements. Power sequencing is implemented using a simple sequencing circuit that controls the order at which the power supplies in the TPS650061 are enabled and disabled.

2.1 Power-On Sequence

The following sequence is required for powering on the TMS320DM365: the 1.2-V rail must power on first, then the 1.8-V rail, and then the 3.3-V rail powers on. After all three rails are powered on, $\overline{\text{RESET}}$ may be released.

Per the excerpt from the TMS320DM365 data sheet for Simple Power-On, the device must be powered on in the following order:

1. Power on PRTCSS/Main Core (1.2 V).
2. Power on PRTCSS/Main I/O (1.8 V).
3. Power on the Main/Analog I/O (3.3 V).

RESET must be low until all supplies are ramped up.

2.2 Power-Off Sequence

The power-down requirements state that the supplies must power off in the reverse order at which they were powered on. These requirements are described in the TMS320DM365 data sheet for Simple Power-Off:

1. Power off Main/Analog I/O (3.3 V).
2. Power off PRTCSS/Main I/O (1.8 V).
3. Power off PRTCSS/Main Core (1.35 V).

If RESET is low, steps 2 and 3 may be performed simultaneously.

If RESET is not low, these steps must be followed sequentially.

3 Schematic

The TPS650061 and the discrete sequencing circuit are shown in Figure 1. The output voltages were configured using the external feedback resistors so that VODC, VLDO1, and VLDO2 are 1.2 V, 3.3 V, and 1.8 V respectively. Additional bypass/decoupling capacitors not shown on the schematic are required at the processor.

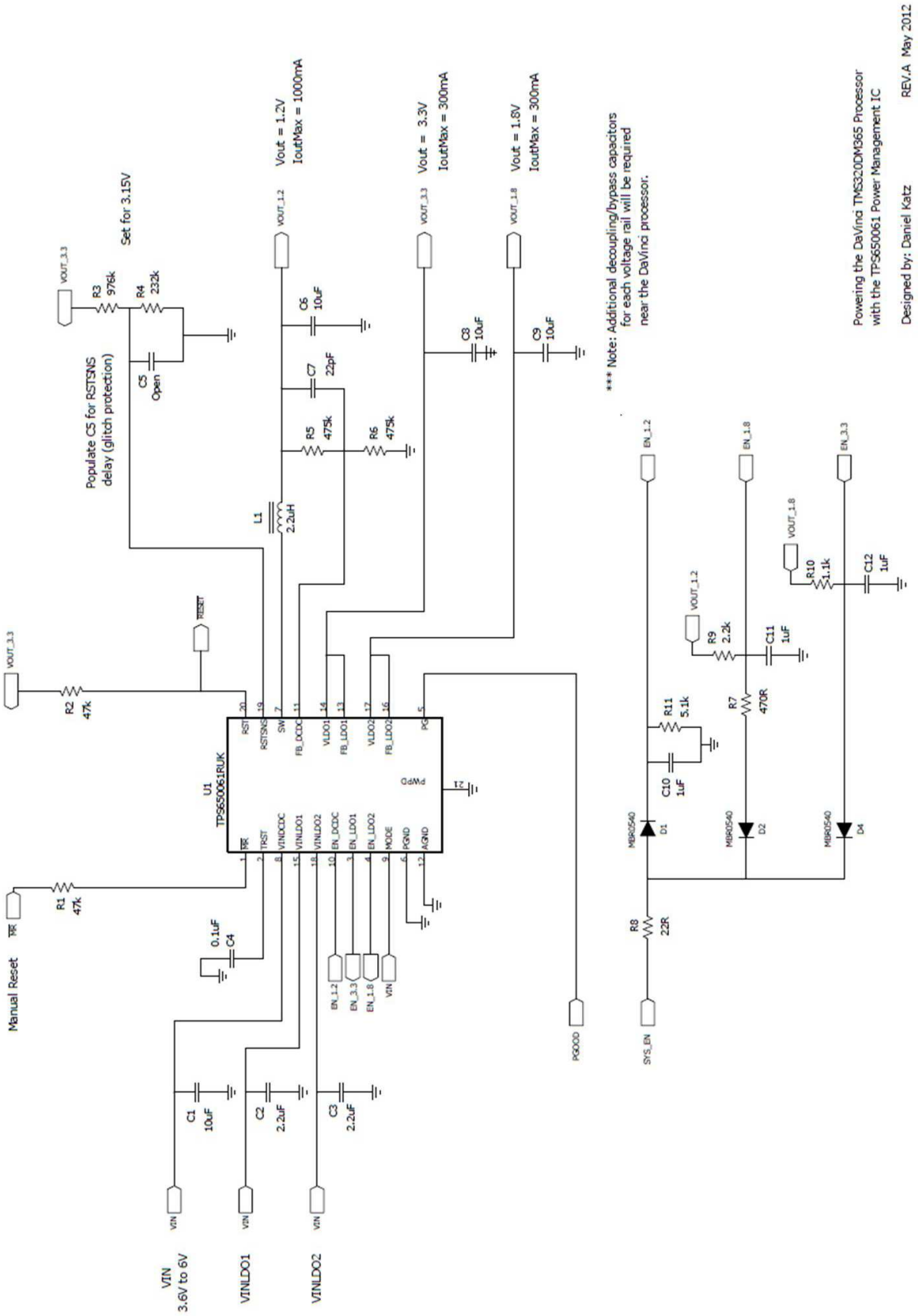

Figure 1. TPS650061 Schematic with Discrete Sequencing Components

4 Waveforms

The waveforms below and on the next page show typical operation of the sequencing circuit during power-on and power-off cycles:

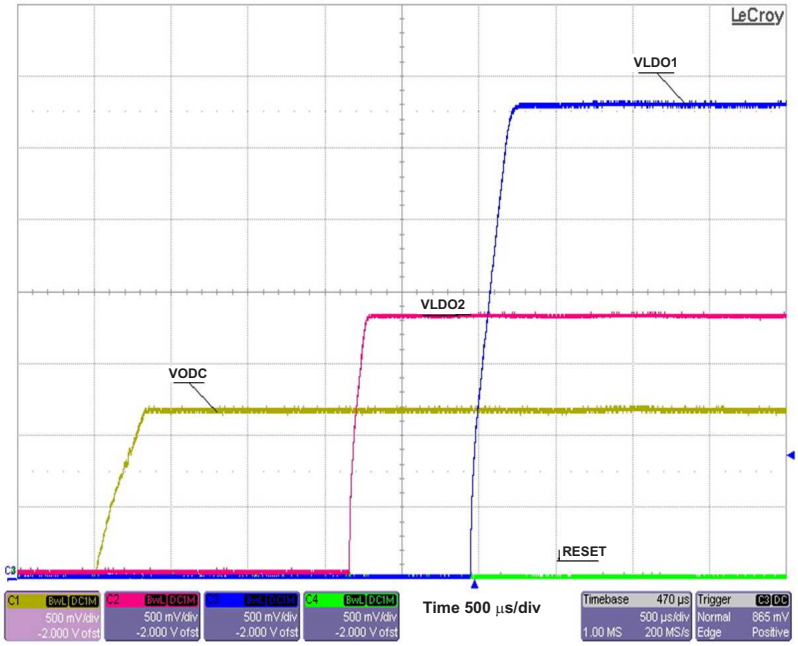

Figure 2. Power-On Sequence, 500 µs/div

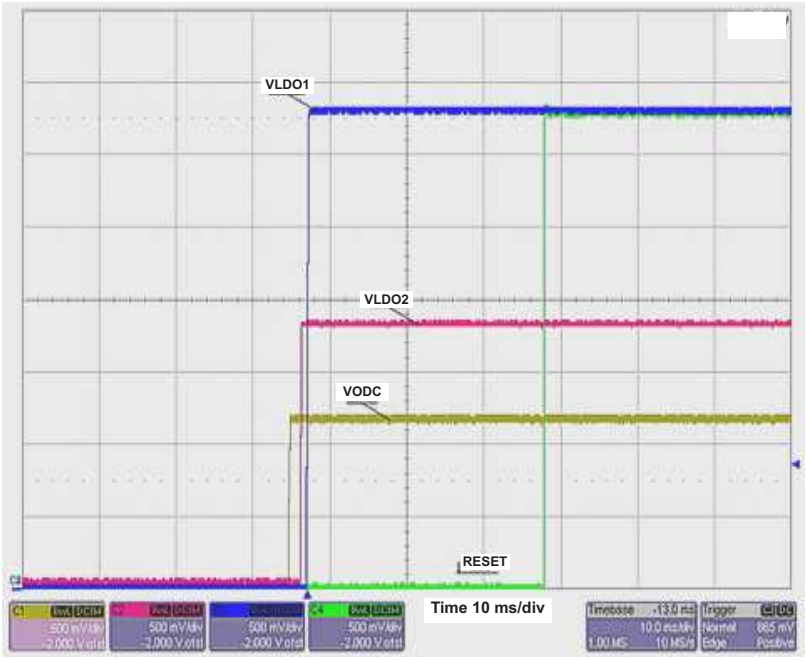

Figure 3. Power-On Sequence, 10 ms/div

For the turn-on sequence shown in Figure 2, note that the 1.2-V rail (VODC) rises first, followed by the 1.8-V (VLDO2), and 3.3-V (VLDO1) rails. The same turn-on sequence is shown in Figure 3 on a larger timescale to show the $\overline{\text{RST}}$ pin going high. The $\overline{\text{RST}}$ pin goes high after a delay time once the 3.3-V rail rises above 3.15 V, as detected by the RSTSNS pin. The delay time of the $\overline{\text{RST}}$ pin is controlled by an external capacitor on the TPS650061 TRST pin. Note that the 3.3-V rail is always less than 2 V above the 1.8-V rail, satisfying the voltage margin requirements.

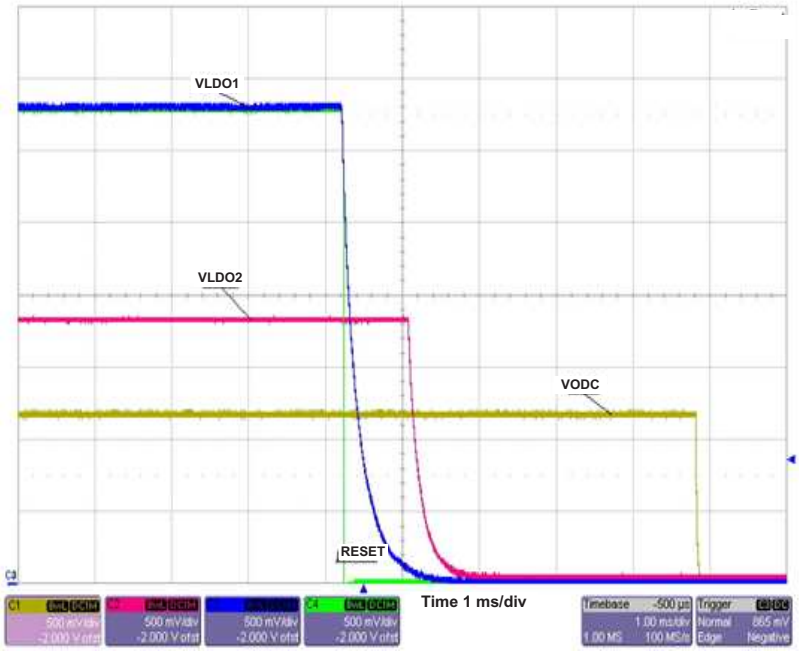

Figure 4. Power-Off Sequence, 1 ms/div

For the turn-off sequence shown in Figure 4, the 3.3-V rail (VLDO1) goes low first, followed by the 1.8-V (VLDO2) and 1.2-V (VODC) rails. The $\overline{\text{RST}}$ pin goes low when the 3.3-V rail drops below 3.15 V, as detected by the RSTSNS pin. Note that the 3.3-V rail is always less than 2 V above the 1.8-V rail, satisfying the voltage margin requirements.

The circuit in Figure 1 was implemented on a TPS650061 Evaluation Module (TPS650061EVM-584) with the sequencing circuitry soldered to a small prototyping PCB. The waveforms above were taken at VIN = 4.2 V with resistive loads at the full load conditions that are expected for the TMS320DM365 device:

Table 2. Test Waveform Load Specifications

Supply Name	Voltage (V)	Current (mA)
VODC	1.2	650
VLDO2	1.8	95
VLDO1	3.3	126

5 Theory of Operation

This sequencing configuration uses a RC circuit on each of the TPS650061 enable pins to ensure that the voltage rails turn on and off at different times. The values of the resistors and capacitors in the RC circuits determine the length of time between each successive voltage rail turn-on/off. The processor is turned on or off by bringing the System Enable (SYS_EN) node on the sequencing circuit high or low, respectively.

5.1 Startup

When SYS_EN is brought high, the 1.2-V enable (EN_1.2) quickly goes high and the 1.2-V output (VOUT_1.2) turns on. Because of the orientation of diodes D2 and D4, EN_1.8 and EN_3.3 remain low at this time. As VOUT_1.2 rises, it charges the capacitor C11 through resistor R9. When the voltage at the EN_1.8 node exceeds the EN_1.8 threshold voltage, VOUT_1.8 turns on. A similar process occurs to turn on VOUT_3.3.

Once VOUT_3.3 reaches the threshold of the RSTSNS pin, the reset pin ($\overline{RST}$) goes high to enable the processor. The threshold is set at 3.15 V for the schematic shown in Figure 1; it is changed by adjusting the values of resistors R3 and R4. There is a delay between the triggering of the RSTSNS pin and the $\overline{RST}$ pin going high. This delay time is adjusted by changing the capacitor value on the TRST pin of the TPS650061 per the equation in the TPS650061 datasheet (SLVS810B).

5.2 Shutdown

Once the TPS650061 has been turned on, SYS_EN must be pulled to ground for power-down to occur. The outputs of the regulator keep the enable pins in a high state unless a path to ground through SYS_EN is provided.

When SYS_EN is pulled to ground, the capacitor on EN_3.3 discharges quickly since there is a low-resistance path to ground. The voltage on EN_3.3 drops, and VOUT_3.3 turns off. Once VOUT_3.3 drops below 3.15 V, the $\overline{RST}$ pin is pulled low to disable the processor.

The capacitor on the EN_1.8 node begins to discharge at the same time as EN_3.3, but at a slower rate due to the resistor R7 in the capacitor's discharge path. This delays the turn-off of VOUT_1.8. The capacitor on the EN_1.2 node is discharged by the parallel resistor, R11, since the polarity of the diode, D1, does not allow a path to ground.

5.3 Supply Voltage Supervisor

The output of the Supply Voltage Supervisor (SVS), the $\overline{RST}$ pin, connects to the active-low RESET pin of the processor. When the SVS is triggered, the $\overline{RST}$ pin goes low, putting the processor into reset mode. The SVS is triggered by the voltage on the RSTSNS analog comparator pin or by a forced reset on the $\overline{MR}$ (Manual Reset) pin.

The sequencing circuit in this report takes advantage of the RSTSNS analog comparator to release the processor reset only when the VOUT_3.3 rail has reached approximately 3.15 V, and to assert the processor reset when the VOUT_3.3 rail drops below 3.15 V. The user can also use an external switch, transistor, or microcontroller to toggle the $\overline{MR}$ pin and trigger a processor reset as needed.

6 Design Considerations

Although the discrete sequencing circuit is simple, care must be taken to ensure the circuit operates in a specific application.

6.1 Enable Pin Thresholds

A voltage divider is formed at the EN_1.8 node due to R9 and R7; when SYS_EN is low, the voltage at the EN_1.8 node should be less than the threshold for the EN_1.8 pin (0.4 V max). If R7 and R9 prevent the voltage from dropping low enough, VOUT_1.8 will not turn off. The value for R7 should be large enough to delay the EN_1.8 turn-off, but small enough for turn-off to occur.

6.2 Inrush Current

Inrush current in excess of 1 A can occur on SYS_EN when it is pulled high due the low-impedance path to the capacitor on the EN_1.2 node. Use a small-value resistor in series with SYS_EN to limit the inrush current (R8 is 22 Ω in the schematic). Using too high a resistor value influences the EN_1.8 voltage divider ratio since R7 is connected to ground in series with R8 (see Section 6.1). If controlling SYS_EN with a microcontroller or other logic device, be sure that any inrush current does not exceed the maximum ratings of that device.

6.3 Diode Selection

Due to their low forward voltage drop (0.15–0.45 V) and fast switching speed, Schottky diodes are recommended in the sequencing circuit. Schottky diodes also have a shorter reverse recovery time compared to other types of diodes, minimizing reverse current overshoot when changing from forward conducting to the reverse blocking state.

6.4 Load Turn-off Time

A factor that may affect the turn-off time is the capacitance and load resistance on the TPS650061 outputs. Since the DC/DC switching converter and the LDOs in the TPS650061 will look *open* to the output when disabled, the output voltage decay will depend partly on the capacitance and load resistance on the output. Design the output capacitance to meet the ripple requirements of the processor and adjust the sequencing circuit component values, if necessary, to ensure proper sequence timing.

6.5 Output Capacitors

The TMS320DM365 processor requires several local bypass/decoupling capacitors in addition to the bulk output capacitors shown in Figure 1. The values of these capacitors depends on the ripple tolerance of the voltage rails and the activity (load) of the processor and I/O peripherals. Ripple-tolerance specifications are found in the Recommended Operating Conditions table, Section 5.2, in the processor datasheet. Design the output capacitance to meet the ripple requirements of the processor and adjust the sequencing circuit component values, if necessary, to ensure proper sequence timing.

6.6 Power Good

The Power Good (PG) pin on the TPS650061 is an open-drain output that indicates the condition of the enabled step down converter and LDOs. The PG pin is pulled low only if all three outputs are regulating correctly. In the event one of the TPS650061 outputs fails because of a short or other means, the PG pin will change to a High-Z state. This can provide an additional level of protection to the system; an external transistor or microprocessor is used to monitor the state of PG and disable SYS_EN to avoid possible damage to the processor.

6.7 RESET Pull-up Resistors

The active-low $\overline{\text{RESET}}$ pin should be pulled high through an external pull-up resistor; in this case, the $\overline{\text{RESET}}$ line *is pulled up to VOUT_3.3 through a 47-kΩ resistor*.

7 References

1. *TPS650061, 2.25 MHz Step-Down Converter* Datasheet (SLVS810B).
2. *TMS320DM365, Digital Media System-on-Chip* Datasheet (SPRS457E).
3. *Powering the TMS320DM368 With TPS650061* (SLVA486).
4. *Powering the OMAP-L132/OMAP-L137/OMAP-L138 Processors with the TPS650061 Power Management IC* (SLVA513).

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8 Bill of Materials

Below is the Bill of Materials for the circuit shown in Figure 1. Note that the RefDes numbers do not correspond to those on the TPS650061 Evaluation Board (TPS650061EVM-584).

Table 3. Bill of Materials

Qty	RefDes	Value	Description	Size	Part Number	Mfr
4	C1, C6, C8, C9	10 µF	Capacitor, ceramic, 10 V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata
2	C2, C3	2.2 µF	Capacitor, ceramic, 16 V, X5R, 10%	0603	GRM188R61C225KE15D	Murata
1	C4	0.1 µF	Capacitor, ceramic, 50 V, X7R, 10%	0805	GRM21BR71H104KA01L	Murata
0	C5	0.1 µF	Capacitor, ceramic, 25 V, X7R, 10%	0603	Std	Std
1	C7	22 pF	Capacitor, ceramic, 50 V, C0G, 5%	0603	Std	Std
3	C10, C11, C12	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0603	Std	Std
3	D1, D2, D3	MBR0540	Diode, Schottky, 0.5 A, 40 V	SOD-123	MBR0540	Fairchild
1	L1	2.2 µH	Inductor, SMT, 2.0 A, 110 mΩ	0.118 × 0.118 in	LPS3015-222ML	Coilcraft
2	R1, R2	47 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R3	976 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R4	232 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
2	R5, R6	475 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R7	470 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R8	22 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R9	2.2 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R10	1.1 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R11	5.1 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS650061	IC, 2.25-MHz Step-Down Converter with Dual LDOs and SVS	QFN	TPS650061RUK	TI

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