Design Guidelines for TPS54120 as a 3-A Switcher and 1-A Switcher Plus LDO

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ABSTRACT

This application report is presented to help designers utilize both power rails of the TPS54120. Although the low-dropout regulator (LDO) is internally limited at 1 A, the integrated switching regulator can support up to a 3-A load. This allows the switcher to handle an additional 2-A load on top of driving the LDO's 1-A output power rail. A step-by-step guide explaining how to fully utilize TPS54120 as a 3-A switcher and a 1-A LDO is provided.

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1   Introduction

The TPS54120 combines the high efficiency of a step-down switching converter with a low-noise LDO to provide an ultra low-noise and highly-efficient power supply. With a wide input range of 4.5 V to 17 V, the TPS54120 is ideally suited for systems with 12-V power busses. A continuous output current of 1 A is supported through the LDO and up to 3 A through the switcher output.

The TPS54120 is ideal for applications that require two power-supply rails. In addition to the clean 1-A power rail produced by the LDO, the rail produced by the switching regulator can be used to drive heavier loads (up to 3 A) with less restriction on noise performance, as shown in Figure 1. The output voltages of the LDO and switcher can be set independently using external resistors. For optimal performance, the output of the switching regulator must be set at least 0.8 V above the LDO output voltage.
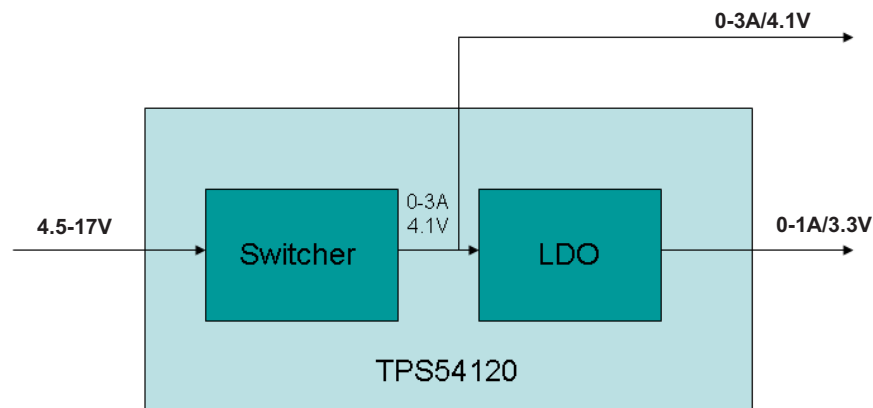
Figure 1. TPS54120 as a 3-A Switcher or a 1-A Switcher Plus LDO

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2   Design Set Up

In order to support 3-A loads at the switcher output, the inductor (L), and compensation components (R4, C6, Cc and C8) must be properly designed. The remaining peripheral components are unaffected by switcher load current and do not require special consideration in this application report, please use the TPS54120EVM-103 as a reference. The equations necessary to determine the current-sensitive components, L, R4, and C8, are provided in this section. Additional information regarding component calculations can be found in the TPS54120 datasheet and the EVM User's guide (see Figure 2).
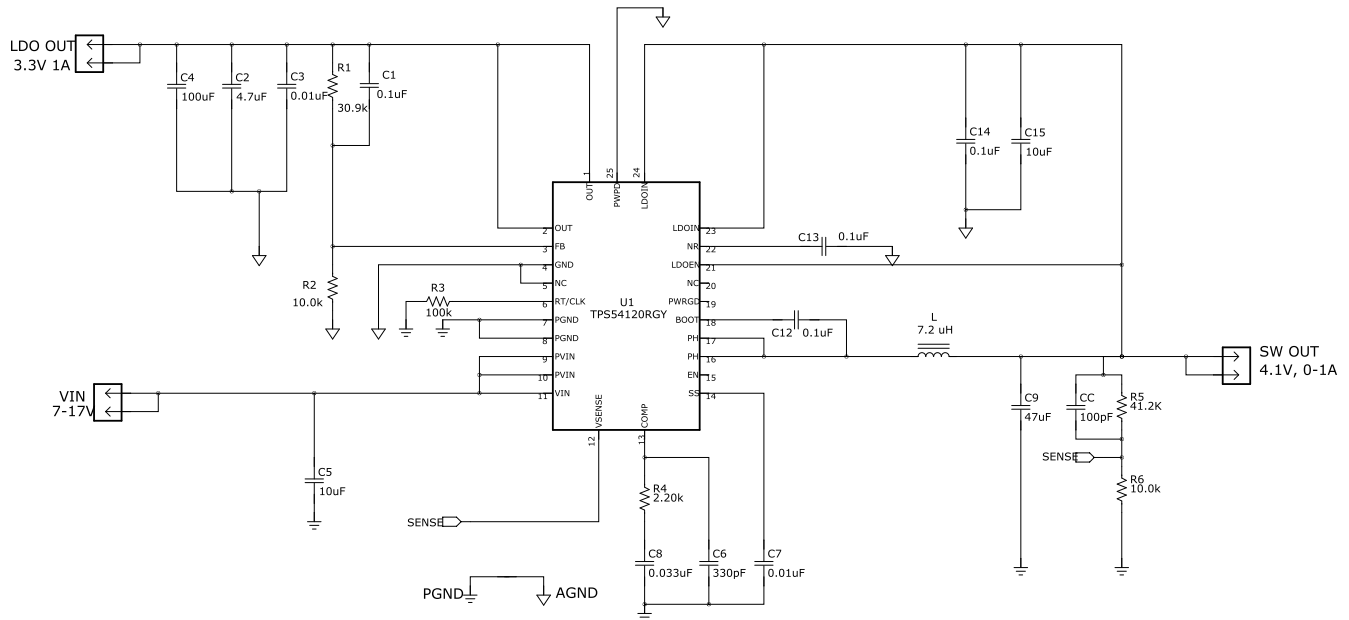
Figure 2. Typical TPS54120 Application Circuit

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2.1 SW Cout

There are three primary considerations for selecting the value of the output capacitor:

- Minimum capacitance to meet the load transient requirement
- Minimum capacitance to meet the output voltage ripple requirement
- Maximum ESR to meet the output voltage ripple requirement

The output capacitor is selected based on the most stringent of these three criteria. Use the same capacitor as selected in the TPS54120EVM user's guide and recommended in the data sheet. In this design example, a 47-µF capacitor is used.

2.2 Compensation Component Selection

There are several compensation techniques for DC-DC converters as discussed in *Understanding the Compensation Network for the TPS54120* (SLVA503). In this design example, Type III-A compensation is used for high bandwidth and high phase margin. The targeted bandwidth in this design is set to 22.8 kHz, the input voltage range for this design example is 7-17V, LDO V_{out} = 3.3 V, SW V_{out} = 4.1 V.

First, calculate the value of R4 using Equation 1 which sets the gain of the compensated network at the crossover frequency. In this example, a 2.2-kΩ resistor was calculated.

$$R_4 = \frac{2\pi \times f_c \times Vout \times Cout}{gmea \times Vref \times gmps}$$

$$R_4 = \frac{2\pi \times 22.8\,kHz \times 4.1\,V \times 47\,\mu F}{1300\,\mu A \times 0.8\,V \times 12 A/V}$$

$$R_4 = 2.2\,K\Omega \tag{1}$$

Where:

gmea: is the GM amplifier gain (1300 µA/V).
gmps: is the power-stage gain (12 A/V).
f_C: is the target crossover frequency.
C_{out}: output cap of the SW.

Next, calculate the value of C8. Together with R4, C8 places a compensation zero at the modulator pole frequency. Use Equation 2 to determine the value of C8. Under these requirements, Equation 2 yields 29.2 nF.

$$C_8 = \frac{Vout \times Cout}{Iout \times R4}$$

$$C_8 = \frac{4.1\,V \times 47\,\mu F}{3 \times 2.2\,K\Omega}$$

$$C_8 = 29.2\,nF \tag{2}$$

In Type III-A, an additional capacitor (Cc) is added in the feedback network providing a zero around the crossover frequency to boost the phase at crossover. The nearest standard value for Cc is 100 pF.

An additional high-frequency pole is used in Type III to attenuate any high-frequency signals that might couple into the control loop. This is accomplished by adding a capacitor (C6) in parallel with the series combination of R4 and C8. This pole is set at roughly half of the switching frequency using a 330-pF capacitor for C6.

2.3   Inductor Selection

Use Equation 3 to calculate the value of the output inductor. KIND is a coefficient that represents the amount of inductor-ripple current relative to the maximum output current. The inductor-ripple current is filtered by the output capacitor. Therefore, choosing a high inductor-ripple current impacts the selection of the output capacitor since the output capacitor must have a ripple current rating greater than or equal to the inductor-ripple current. Normally, the inductor-ripple value is at the discretion of the designer, however, KIND is normally from 0.2–0.4 for the majority of applications. Under the 3-A, V_{OUT} = 4.1 V requirements, Equation 3 yields 7.2 µH.

$$L = \frac{Vinmax - Vout}{Iout \times Kind} \times \frac{Vout}{Vin \times fsw}$$

$$L = \frac{17\ V - 4.1\ V}{3A \times 0.3} \times \frac{4.1\ V}{17\ V \times 480\ kHz}$$

$$L = 7.2\ \mu H \tag{3}$$

During component selection, L saturation current must be rated greater than 3 A.

2.4   Input Capacitor

The TPS54120 requires a high-quality ceramic, type X5R or X7R, input-decoupling capacitor of 4.7 µF on each input voltage rail.

2.5   Boost Capacitor

A 0.1-µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation.

2.6   Other components

Use the same values as in the TPS54120EVM-103.

3   Test Results

Figure 3 and Figure 4 illustrate the TPS54120's ability to drive loads in excess of 1 A. Two resistive loads are used to draw current at the LDO and switcher outputs simultaneously. The resistive load at the output of the switcher was adjusted to draw between 0 A and 3 A, while the resistive load at the output of the LDO was adjusted to draw between 0 A and 1 A; the summation of these two load currents never exceeded 3 A.
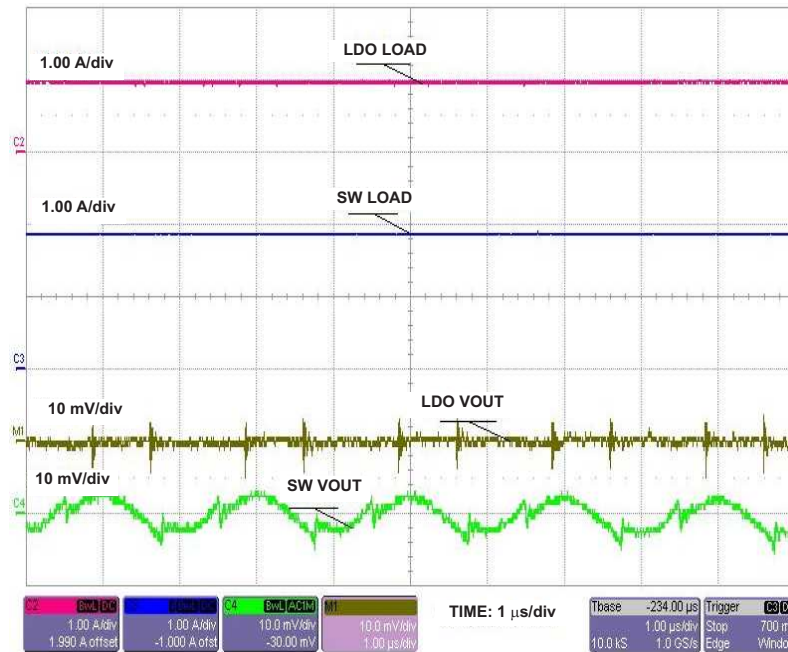
Figure 3. 1-A Load at LDO Output, 2-A Load at Switcher Output
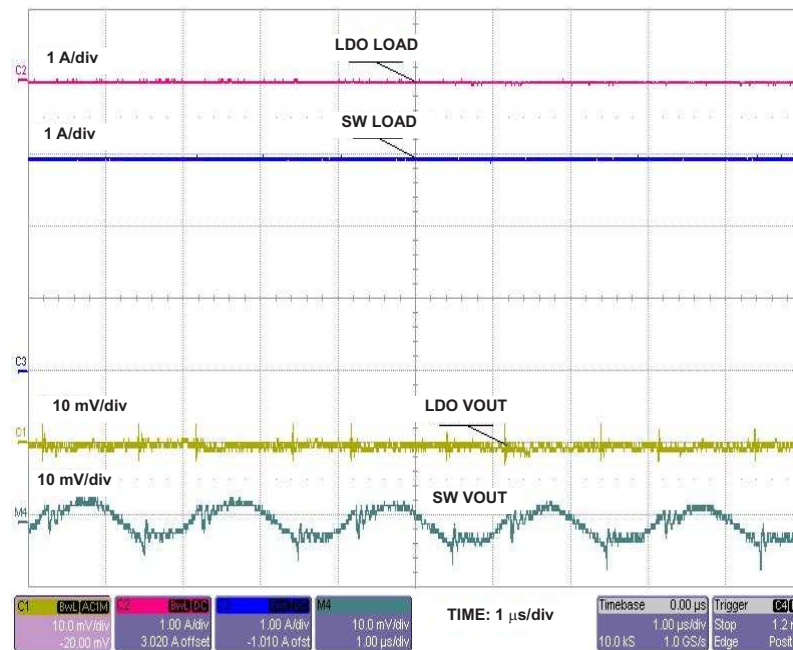
Figure 4. No load at LDO Output, 3-A Load at Switcher Output

Load transients response of the LDO and the switcher are provided in Figure 5 and Figure 6. In Figure 5, a load step from 750 mA to 1.5 A is applied to the switcher output while the LDO output load is kept constant. An approximate 200-mV ripple is observed at the output voltage of the switcher. As expected, the LDO output voltage does not experience any voltage ripples. In Figure 6, a 0- to 500-mA load step is applied at the LDO output and a voltage ripple is experienced at both the LDO and the switcher output voltages.
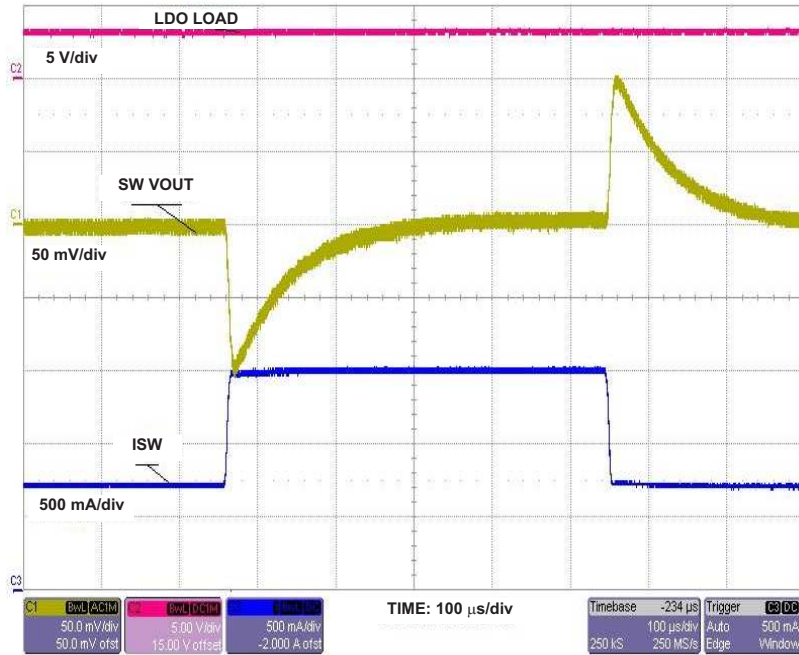
Figure 5. 750-mA Load Transient at Switcher Output
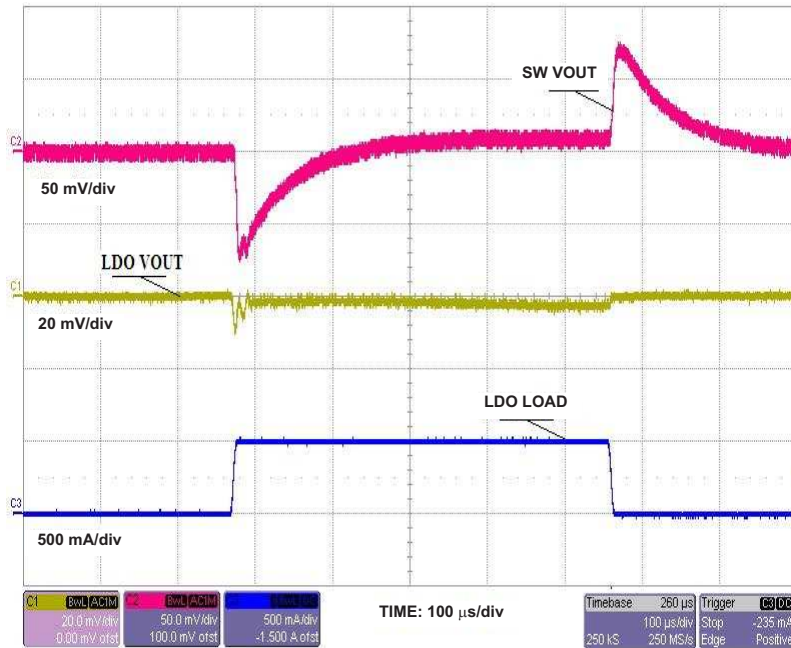
Figure 6. 500-mA Load Transient at LDO Output

4 Conclusion

The TPS54120 can simultaneously support multiple loads by using the switching regulator's output rail in conjunction with the LDO's output rail. Some parameters need to be designed properly for the required specification. This application report provides the user step-by-step design guidelines on how to use and design the TPS54120 for a 3-A switcher or a 2-A SW plus 1-A LDO.

IMPORTANT NOTICE