TPS54120 Sequencing and Tracking

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ABSTRACT

The TPS54120 is an integrated switcher and low-dropout (LDO) regulator optimized for high efficiencies and a low-noise output. This application report describes how to use the Enable, Power Good, and Slow Start pins in tracking and sequencing applications. Three different tracking and sequencing methods are described in this report: sequential, ratiometric, and simultaneous. Each of these methods is tested and the results are included in this report.

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1 Device Description

The TPS54120 is a 1-A switcher and LDO converter. It combines the high efficiency of a step-down switching converter with the ultralow noise of an LDO. With its wide input range of 4.5 V to 17 V and adjustable output from 0.8 V to 6 V, it is suitable for many applications with 12-V power buses and contains multiple output voltage rails.

The device is easy to use and suited for applications that require tracking and sequencing. It has a built-in power-good function to indicate the status of the device, a slow-start circuit to control the output voltage slope during start-up, a noise reduction with start-up time for the LDO, and an enable function for independently controlling the turnon of both the LDO and the switcher. Each of these functions is useful for tracking and sequencing applications.

In the sequential start-up, two or more devices are programmed to start in some order using the EN and PWRG pins. In ratiometric start-up, all devices turn on at the same time and have the same ramp-up time. With simultaneous start-up, two devices start at the same rate. With adjustments to resistor values, one device can ramp up at a slightly faster or slower rate compared to the other device.

1.1 SS – Slow Start

1.1.1 Slow Start of Switcher

The rate in which the output voltage of the switcher rises up to the full operational level during the start-up phase is controlled through the SS pin (Soft Start pin). A capacitor (C_{SS}) is connected between the SS pin and the IC ground. The size of the slow-start capacitor determines the slow-start ramp-up time (T_{SS}, 10% to 90%) per Equation 1.

$$Tss(ms) = (C_{SS(nF)} \times V_{ref\ (V)}) / I_{SS(\mu A)} \quad (1)$$

Basically, the device has an internal pullup current source of 2.3 µA = I_{SS} that charges the external slow-start capacitor C_{SS}. The voltage reference $V_{ref(V)}$ for this part is 0.8 V. Thus, by sourcing a constant current onto the capacitor C_{SS} as shown in Figure 1, the device linearly ramps up the voltage on the SS pin, which corresponds to the voltage on the FB pin and thus the output voltage of the switcher.

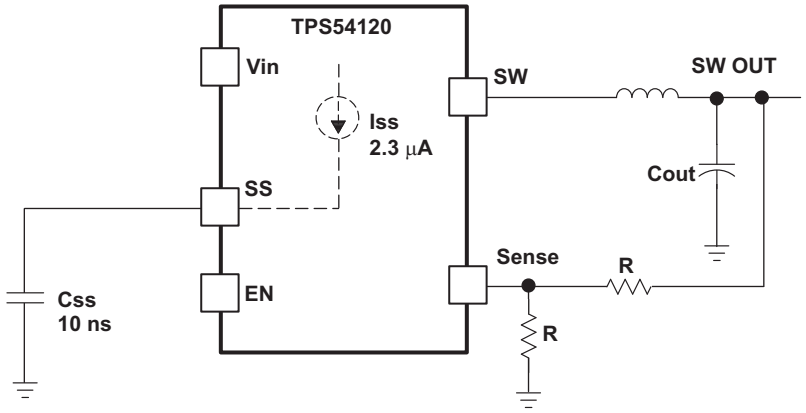


Figure 1. Slow-Start Circuit

Equation 2 shows the relationship between the SS pin voltage (V_{SS}) and Sense pin voltage $V_{(SENSE)}$.

$$V_{Sense} = 1 \times V_{SS} \quad (2)$$

Figure 2 shows the relationship between the tracking voltage with the output voltage and the sense voltage of the switcher.

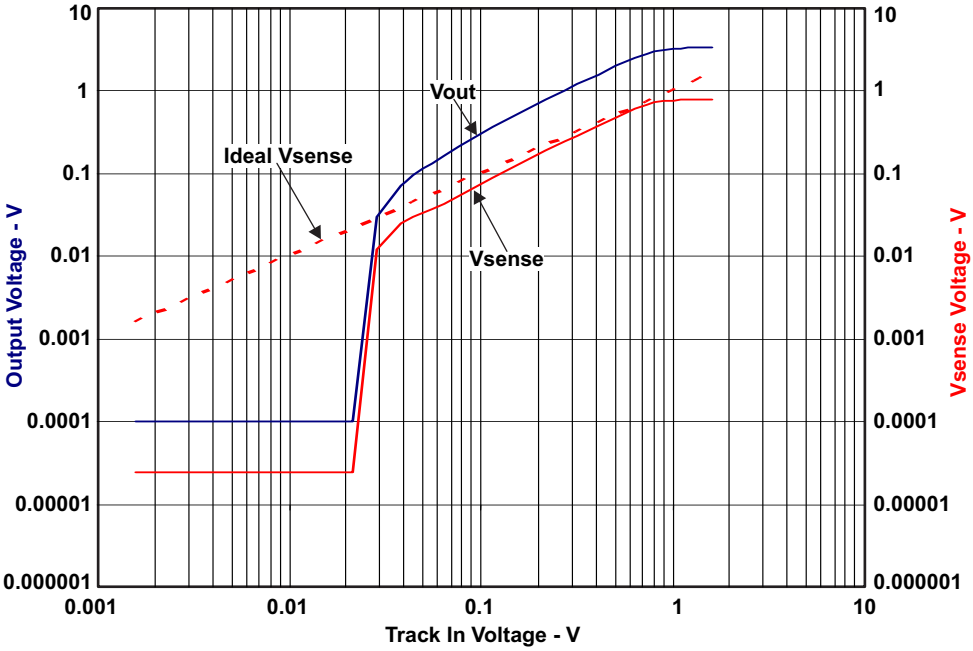


Figure 2. Relationship Between Tracking Voltage and Output Voltage

Figure 3 shows the typical start-up ramp for a TPS54120 set to a 4.1-V output at the switcher with a 12-V input, and C_{SS} = 10 ns. Based on Equation 1, the start-up time is 3.48 ms. T_{SS} is the time it takes the output voltage to go from 10% to 90% of the regulation. Figure 3 shows clearly that the ratio between the sense pin and the slow-start pin voltage is one until approximately 0.7 V.

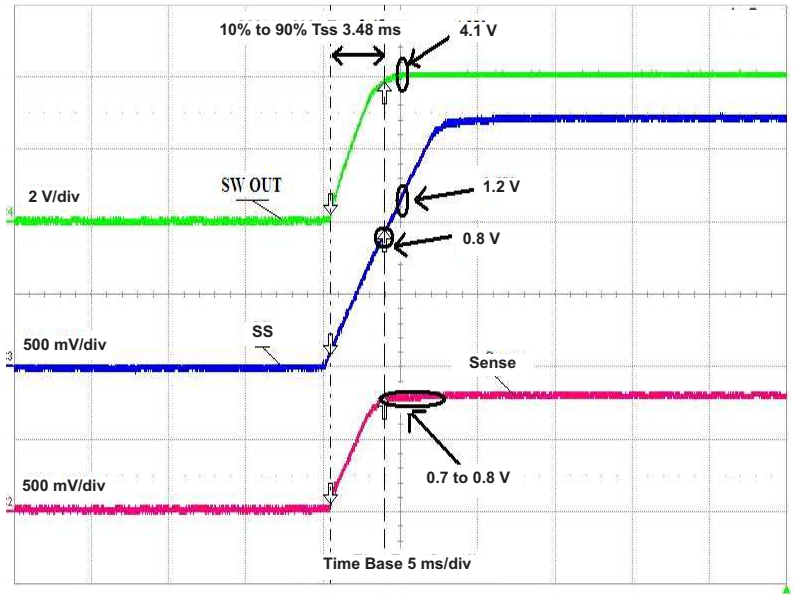


Figure 3. Slow-Start, Ramp-Up Time of Switcher

1.1.2 Start Time of LDO

In addition to noise-reduction purposes, the capacitor on the NR pin is used for slow start-up time. The noise-reduction effect is nearly saturated at 0.01 µF. The start-up time of the LDO can be adjusted by changing the value of C_{NR}. Use Figure 4 to estimate the required value of C_{NR} for a desired start-up time.

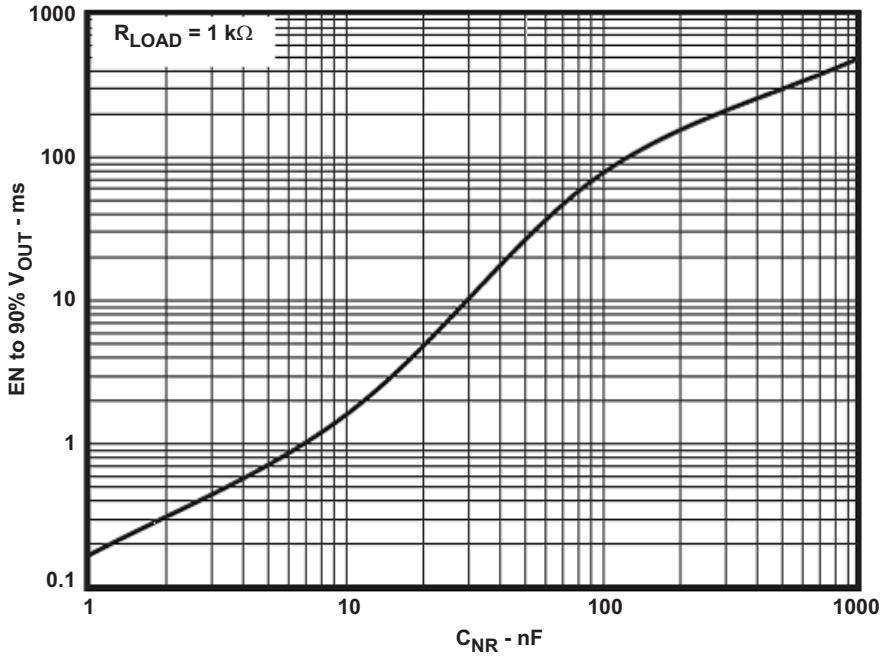


Figure 4. LDO Start-Up Time vs Noise Reduction Capacitor

Figure 5 shows the slow start of the LDO and the switcher at the same time. In this configuration, the enable pin of the LDO is connected to the output of the switcher. Thus, as the switcher gets to regulation level, the LDO gets enabled. The input voltage is 12 V, the switcher output is set to 4.1 V, and the LDO is set to 3.3 V. No load is connected to both the output of the LDO and the switcher. In this test, the C_{NR} capacitor is set for 100 nF, and the C_{SS} is set to 10 nF. From Figure 5, the slow start for the LDO and the switcher is approximately 80 ms and 4 ms, respectively.

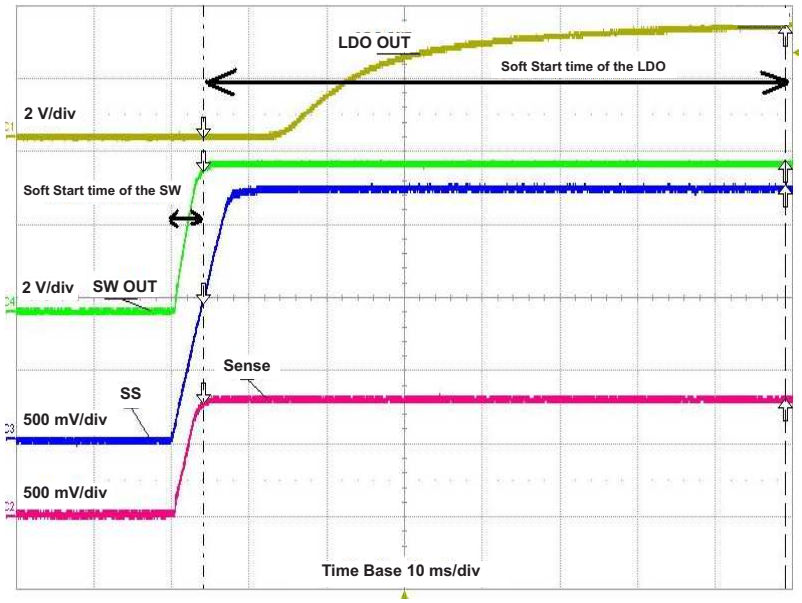


Figure 5. Slow Start of Both Switcher and LDO Output Voltages at Turnon

1.2 EN – Enable

The TPS54120 has two enable pins, EN and LDO EN. EN is used to control the turnon of the switcher, and the LDO EN is used for the LDO. Setting the EN pin to logic low disables the device. Conversely, the device starts up when the enable pin is logic high. It has an internal pullup current source that allows the user to float the EN pin to enable the switcher. The enable threshold for rising is typically 1.2 V and for falling is 1.17 V. Figure 6(a) shows enabling the switcher using 10 nF as the slow-start capacitor. For enabling the LDO, the enable has to be driven high. Driving the pin low puts the regulator into shutdown mode. Figure 6(b) shows the LDO enabling time.

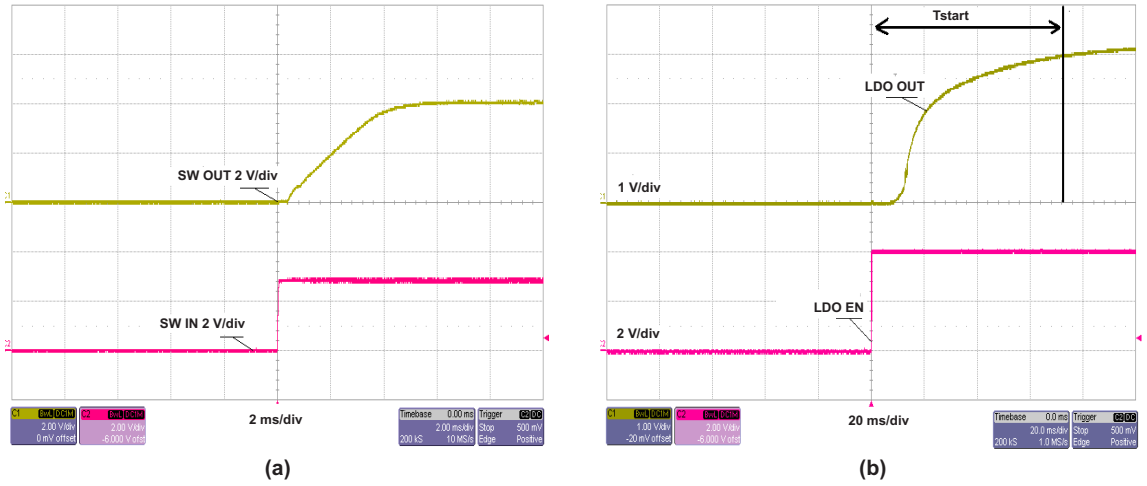


Figure 6. Switcher and LDO Output Voltage Turnon, LDO Enable With C_{NR} = 100 nF

1.3 PWRGD – Power Good

The power-good output is used to indicate that the switcher output voltage has reached regulation. It floats high when the switcher output voltage reaches its appropriate level and is pulled low by the device when the switcher is enabled and the output voltage is below the regulated level. The PWRG pin is an open-drain output that requires an external pullup resistor. This pin can be used for enabling other devices in the system when the output voltage reaches the desired level.

2 Sequential Start-Up Using Enable and Power Good

The sequential start-up method uses the PWRG, and LDO EN functions to turn on a second device after the switcher or the LDO of the first device has reached regulation. In this section, two different configurations are explored: In the first configuration, the PWRG is pulled up to the switcher output; in the second configuration, the PWRG is pulled up to the LDO OUT.

2.1 Sequential Start-Up Using LDO EN and PWRG With Pullup at SW OUT

This sequential start-up configuration method uses the LDO EN and PWRG functions to turn on a second device after the switcher of the first device has reached regulation. Figure 7 shows two TPS54120 devices in a system. The PWRG pin of the first device is used to enable the second device and is pulled up to switcher OUT1. When the SW OUT1 voltage reaches its appropriate level after getting enabled, the PWRG pin turns high. As a consequence, the LDO of the second device is enabled. Note that both SS pins are connected independently, so the slow-start times can be different for each device. Also, the switcher of the second device needs to be enabled before enabling the LDO.

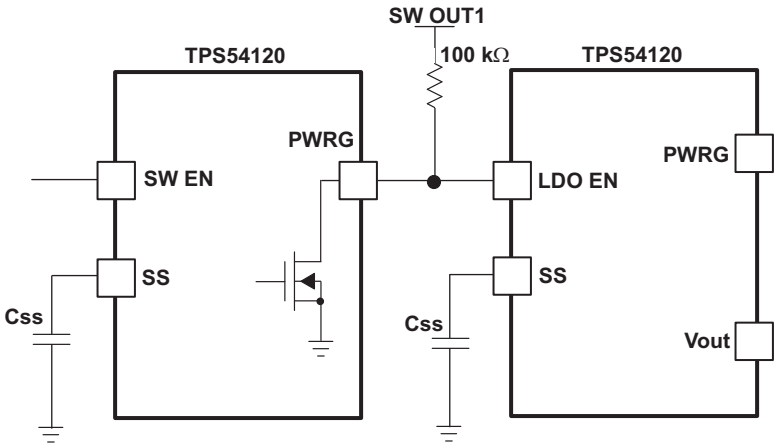
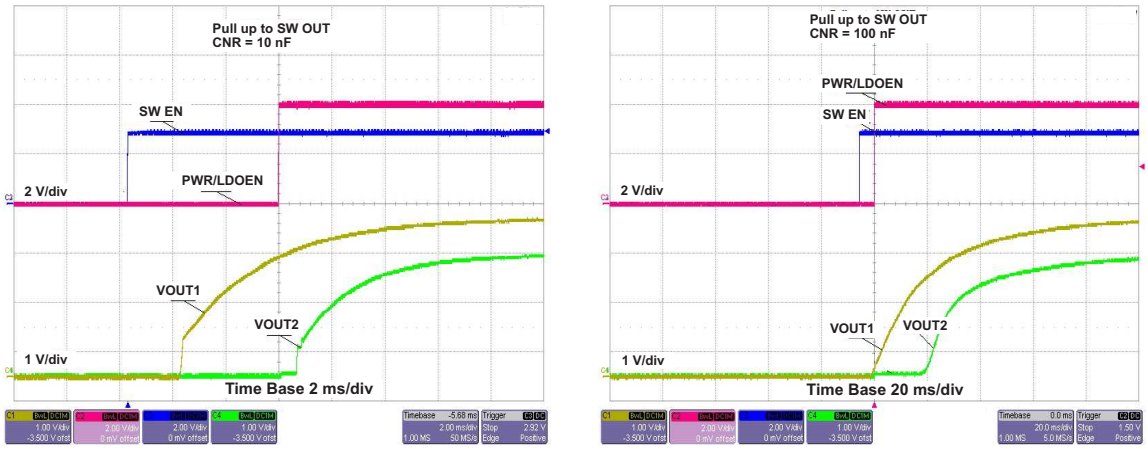


Figure 7. Sequential Start-Up Using EN and PWRG Pins With Pullup at SW OUT

Figure 8 shows the result of the sequential start-up circuit drawn in Figure 7. The switcher enable pin of the first device turns high to enable the first converter, and its output voltage, Vout1, starts rising up. After its slow-start time, the output voltage reaches 3.3 V, which is its regulation voltage. Note that, the power good goes high as the SW OUT1 reaches regulation and enables the second device. Once the second converter gets enabled, its output voltage rises up to its full operation level of 2.5 V after its programmed slow-start time. Two different slow-start times of the LDO are used. In Figure 8(a), a 10-nF, noise-reduction capacitor is used. Thus, the slow-start time is faster than Figure 8(b) where a 100-nF, noise-reduction capacitor is used. Note in this configuration, the time difference between the SW EN and the PWRG is not affected by the slow-start time of the LDO.



(a) (b)

Figure 8. Sequential Start-Up Using EN and PWRG (Pullup at SW OUT)

2.2 Sequential Start-Up Using LDO EN and PWRG With Pullup at LDO OUT

The only difference from the previous configuration is on the PWRGD pullup. In this configuration, it is pulled up to LDO OUT1 instead of the SW OUT 1. Figure 9 shows two TPS54120 devices in a system. The PWRG pin of the first device is used to enable the second device. When the first LDO output voltage reaches its appropriate level after getting enabled, the PWRG pin turns high. As a consequence, the LDO of the second device is enabled. Note that in this configuration, if LDO1 does not get enabled, the PWRG is never pulled up and thus the second device is never activated.

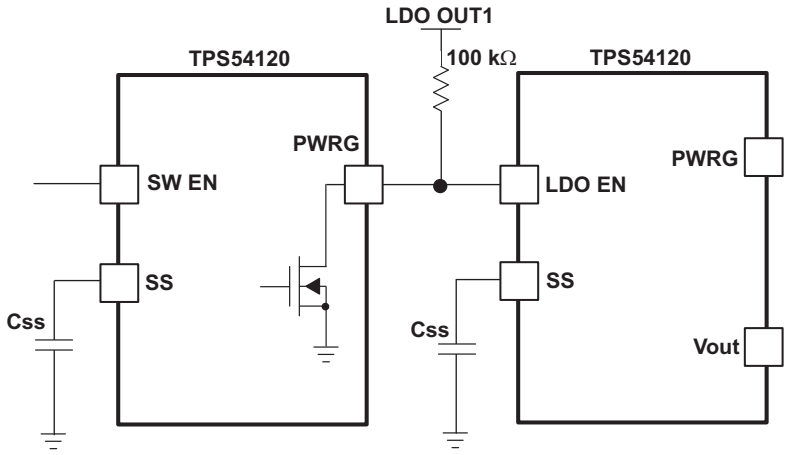


Figure 9. Sequential Start-Up Using EN and PWRG Pins With Pullup at LDO OUT

Figure 10 shows the result of the sequential start-up circuit drawn in Figure 9. The same result is obtained in this configuration except on the time between the SW EN and PWRG, and the time difference between the VOUT1 and VOUT2. In this configuration, the change in the slow-start time of the LDO directly affects the time between the SW EN and PWRG. As a consequence, it also affects the time difference between the VOUT1 and VOUT2. In Figure 10(a), a 10-nF, noise-reduction capacitor is used. Thus, the slow-start time is faster than Figure 10(b) where a 100-nF, noise-reduction capacitor is used.

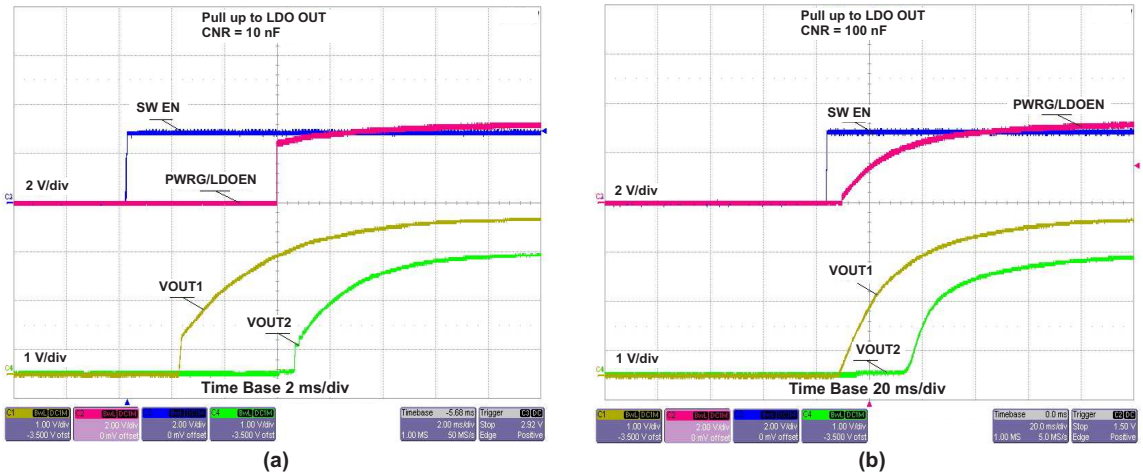


Figure 10. Sequential Start-Up Using EN and PWRG (Pullup at LDO OUT)

3 Ratiometric Start-Up Using Connected SS and EN Pins

In the ratiometric start-up sequence, the EN and SS pins of both devices are connected together, as shown in Figure 11 and Figure 13. The TPS54120 has independent enable pins for the switcher and the LDO. In this section, two configurations are explored.

3.1 Ratiometric Start-Up Using Connected SS and LDO EN Pins

In the ratiometric start-up sequence configuration, the LDO EN and SS pins of both devices are connected together, as shown in Figure 11. A single, slow-start capacitor and the same values of the noise reduction capacitors are used. This configuration forces both devices to start up at the same time when their common enable pin turns high. Also, because the SS pins are connected together and the same value of C_{NR} is used, the slow-start time (T_{SS}) is the same for both devices, and both devices reach regulation at the same time as shown in Figure 12.

Note that the slow-start time of the switcher, as calculated from Equation 1, is half of what it should be because both devices' SS pin current sources are feeding into a single, slow-start capacitor. To achieve the desired slow-start time with Equation 1, double the I_{ss} value to account for the second current source. Regarding the noise-reduction capacitors, they can be set to different values, but the regulation is not achieved at the same time.

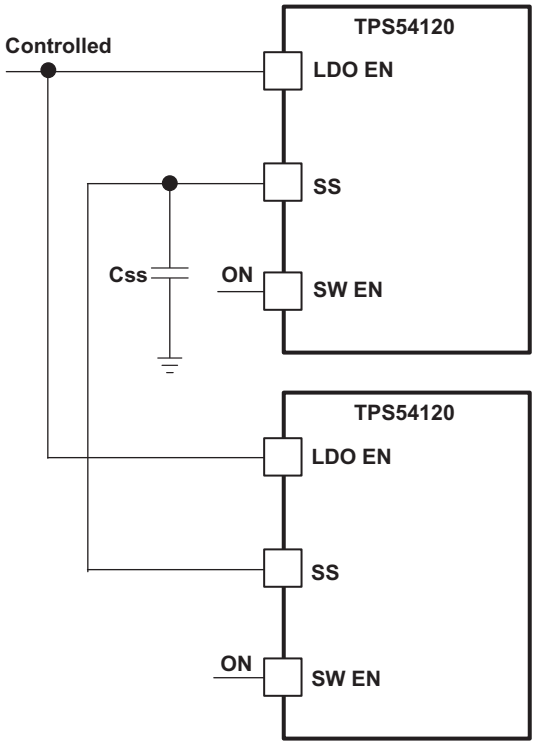


Figure 11. Ratiometric Start-Up Using SS Pins and Enabling LDO

In Figure 12, both output voltages start once the enable pin goes high and both voltages reach regulation at the same time. Because the output voltages are not the same but the slow-start time is equal, their slopes are different. Note that, in this configuration, only the starting time of the LDO is accounted for.

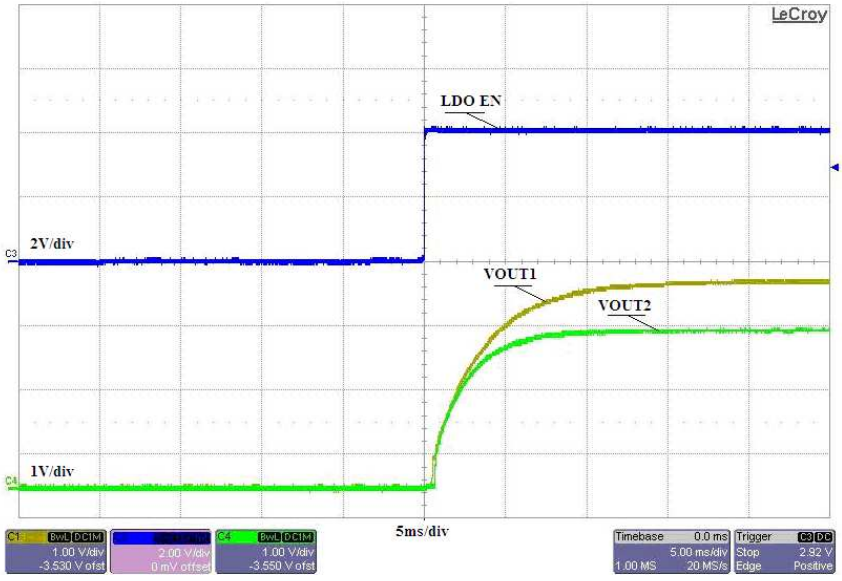


Figure 12. Ratiometric Start-Up Result of Circuit in Figure 11

3.2 Ratiometric Start-Up Using Connected SS and SW EN Pins

In this ratiometric start-up sequence configuration, the SW EN and SS pins of both devices are connected together, as shown in Figure 13. A single, slow-start capacitor and the same values of the noise-reduction capacitors are used. This configuration forces both devices to start-up at the same time when their common enable pin turns high. Also, because the SS pins are connected together and the same value of C_{NR} is used, the slow-start time (T_{SS}) is the same for both devices, and both devices reach regulation at the same time.

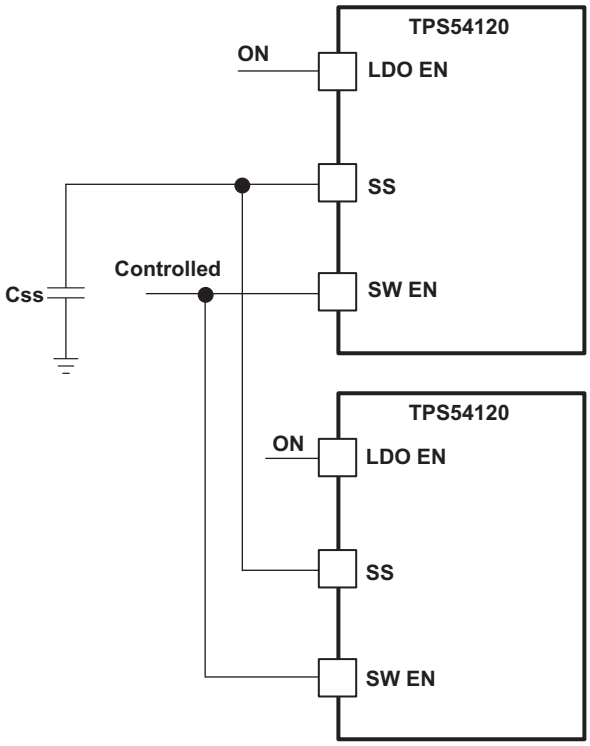


Figure 13. Ratiometric Start-Up Using SS Pins and Enabling Switcher

The only difference in this configuration from the previous one is the start time. In this configuration, in addition to the start time of the LDO, the switcher slow-start time is added to the time it takes the output voltage to reach regulation from the time the switcher is enabled, as shown in Figure 14.

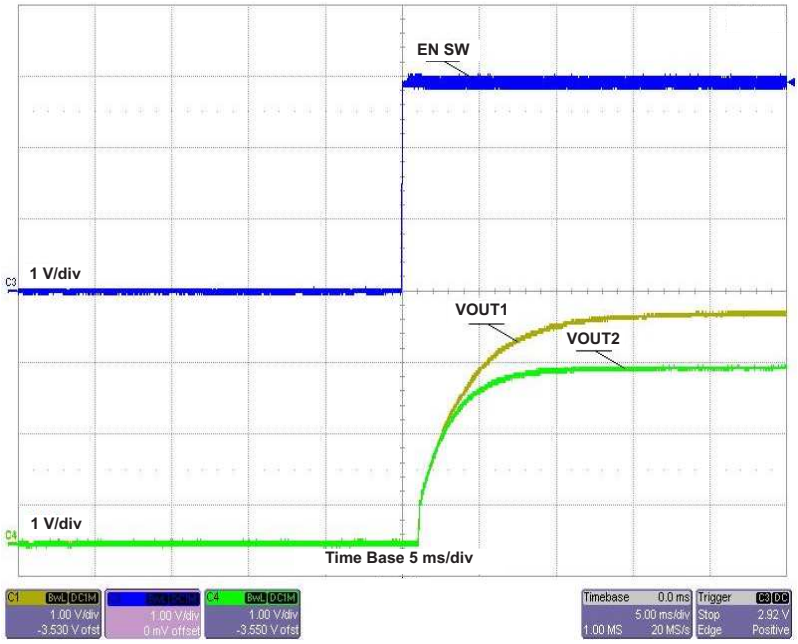


Figure 14. Ratiometric Start-Up Result of Circuit in Figure 13

4 Ratiometric and Simultaneous Start-Up

In ratiometric and simultaneous start-up, the switcher enable pins of both converters are connected together; thus, both devices start at the same time. The SS pin of the first device is connected to ground through its C_{SS} capacitor. The C_{SS} capacitor value defines the slow-start, ramp-up time as expressed in Equation 1. However, the SS pin in the second device is connected to the output voltage of the first converter through two resistors, R1 and R2, as shown in Figure 15.

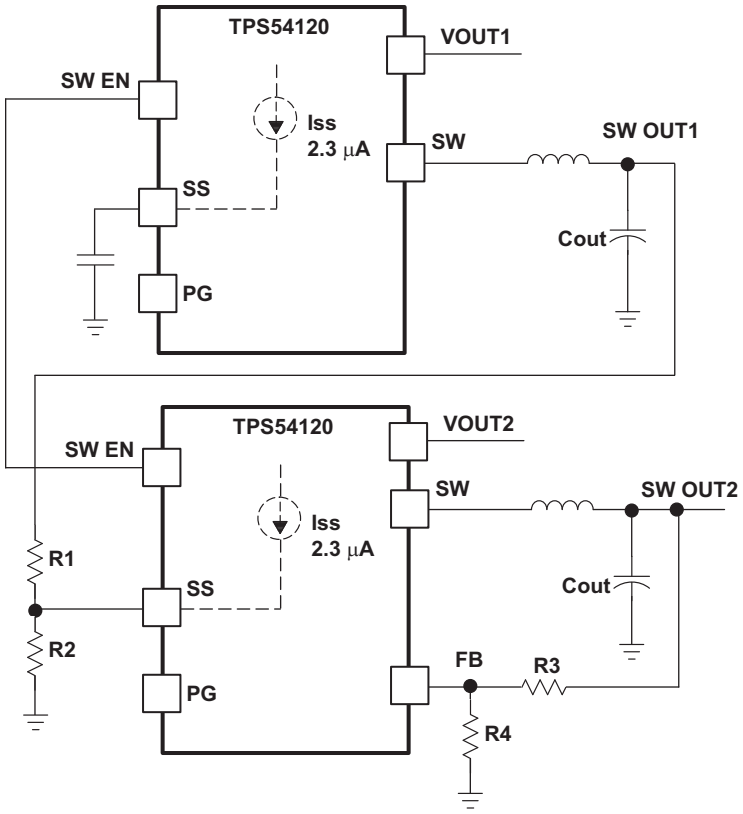


Figure 15. Ratiometric and Simultaneous Start-Up Sequence

In this configuration, because the SS pin of the second converter is connected to the switcher output voltage of the first converter, the VOUT2 start-up slope is related to the start-up slope of SW OUT1. Also, the VOUT2 start-up curve depends on the values of R1 and R2. Equation 3 and Equation 4 can be used to calculate R1 and R2:

$$R1 = (SWOUT2 + \Delta V)/Vref \times (Vssoffset/Iss) \quad (3)$$

$$R2 = (Vref \times R1)/(SWOUT2 + \Delta V - Vref) \quad (4)$$

The tracking resistors can be calculated to initiate the VOUT2 slightly before, after, or at the same time as Vout1. Equation 5 is the voltage difference between VOUT1 and VOUT2.

$$\Delta V = SWOUT1 - SWOUT2 \quad (5)$$

The ΔV variable is 0 V for simultaneous sequencing. Vref is the reference voltage equal to 0.8 V. To minimize the effect of the inherent slow start to VSENSE offset (Vssoffset, 29 mV) in the slow-start circuit and the offset created by the pullup current source (I_{ss}, 2.3 µA) and tracking resistors, the Vssoffset and I_{ss} are included as variables in the equations. Also, to ensure proper operation of the device, R1 must be greater than the value calculated using Equation 6.

$$R1 > 2800 \times SWOUT1 - 180 \times \Delta V \quad (6)$$

With the configuration of Figure 15, three situations are possible: Vout1 ramps up faster than Vout2, Vout2 ramps up faster than Vout1, and Vout 1 ramps up at the same rate as Vout2. The next sections explain how to calculate the values of R1 and R2 for the desired ramp-up relationship.

4.1 Vout1 Leading Vout2

In this configuration, the output voltage of the first converter leads the output voltage of the second converter. In Figure 16, Vout1 and Vout2 are regulated to 3.3 V and 2.5 V, respectively, and SW OUT1 and SW OUT2 are regulated to 4.1 V and 3.3 V, respectively. Table 1 provides the calculated values of R1 and R2 for this configuration.

Table 1. Vout1 Leading Vout2 Calculations

Vref	0.8 V
Vssoffoset	29 mV
Iss	2.3 µA
SW OUT1	4.1 V
SW OUT2	3.3 V
ΔVOUT	1 V
R1	67.8 kΩ
R2	15.49 kΩ

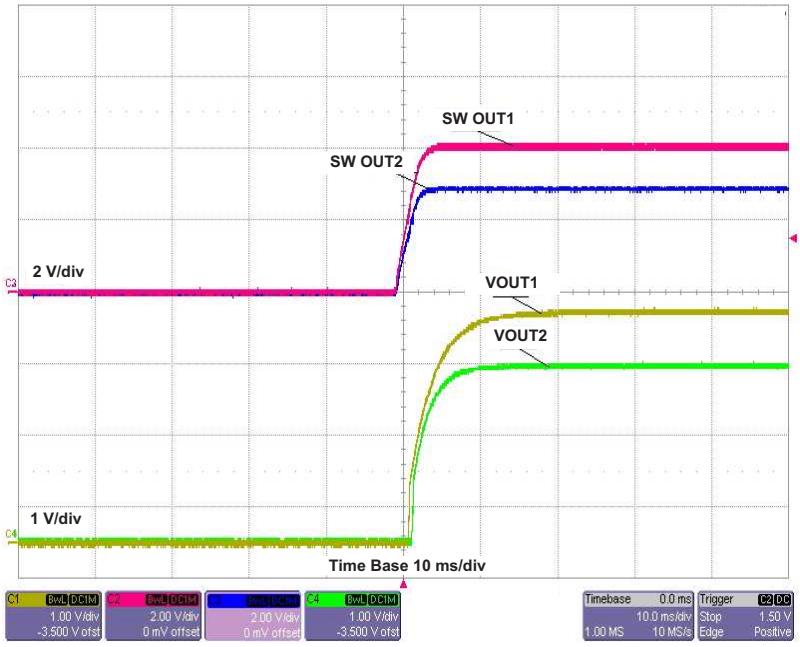


Figure 16. Ratiometric Start-Up With Vout1 Leading Vout2

4.2 Vout2 Leading Vout1

With this configuration, the output voltage of the second converter leads the output voltage of the first converter. In Figure 17, Vout1 and Vout2 are regulated to 3.3 V and 2.5 V, respectively, and SW OUT1 and SW OUT2 are regulated to 4.1 V and 3.3 V, respectively. Table 2 provides the calculated values of R1 and R2 for this configuration.

Table 2. Vout2 Leading Vout1 Calculations

Vref	0.8 V
Vssoffoset	29 mV
Iss	23 µA
SW OUT1	4.1 V
SW OUT2	3.3 V
ΔVOUT	–2 V
R1	20.5 kΩ
R2	32.782 kΩ

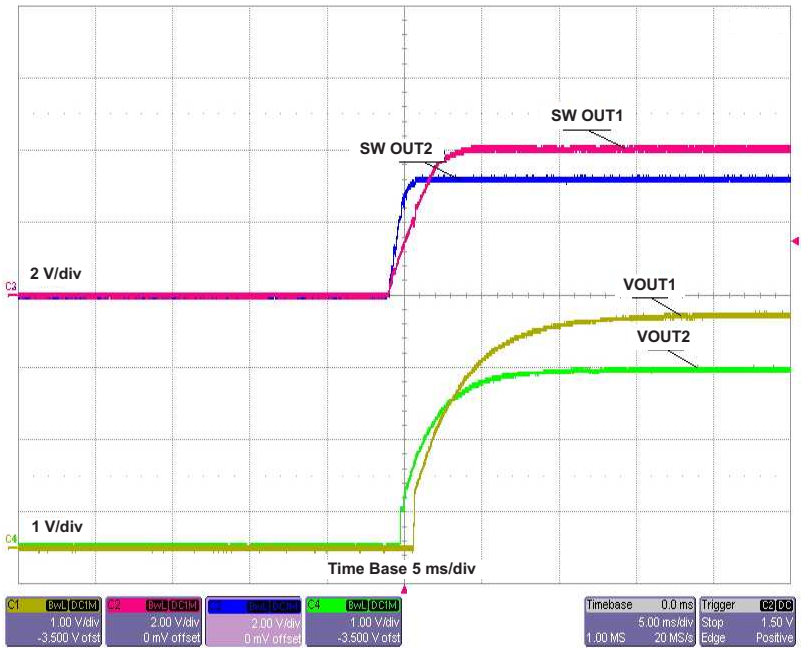


Figure 17. Ratiometric Start-Up With Vout2 Leading Vout1

4.3 Simultaneous Start-Up

In the simultaneous start-up, the slopes of the both output voltages are the same as shown in Figure 18. Thus, both voltages reach regulation at two different times. Table 3 provides the calculated values of R1 and R2 for this configuration. The settings of SW OUT1 and 2 and VOUT1 and 2 are the same as in the previous sections.

Table 3. Simultaneous Start-Up Calculations

Vref	0.8 V
Vssoffoset	29 mV
Iss	2.3 µA
SW OUT1	4.1 V
SW OUT2	3.3 V
ΔVOUT	0 V
R1	50.2 kΩ
R2	16.65 kΩ

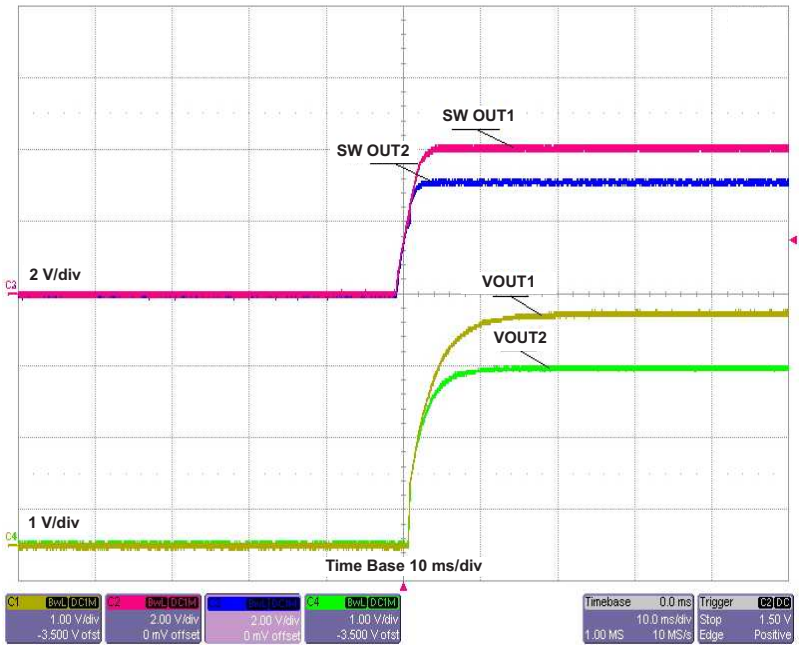


Figure 18. Simultaneous Start-Up

5 Conclusion

This application report described three different tracking and sequencing methods: sequential, ratiometric, and simultaneous. Sequential start-up using the LDO, EN, and PWRG pins starts two or more devices in some order, one device after another. The ramp-up time and slope of each device are independent. In ratiometric start-up with connected SS pins, all devices turn on at the same time and have the same ramp-up time. With simultaneous start-up, two devices start up at the same rate. With small adjustments to resistor values, one device can ramp up at a slightly faster or slower rate compared to the other device.

5.1 References

1. *TPS54120, Low-Noise, 1-A Power Supply With Integrated DC-DC Converter and Low-Dropout Regulator* data sheet (SBVS180)
2. *TPS54320, 4.5V to 17V Input, 3A Synchronous Step Down SWIFT™ Converter* data sheet (SLVS982)
3. *TPS62130/40/50 Sequencing and Tracking* application report (SLVA470)

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