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High-Integration, High-Efficiency Power Solution Using DC/DC Converters With DVFS

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PMP - DC/DC Low-Power Converters

ABSTRACT

This reference design helps those desiring to design-in the TMS320C6742, TMS320C6746, TMS320C6748 and OMAP-L138. This design, employing sequenced power supplies, describes a system with an input voltage of 5V, and uses a high-efficiency DC/DC Converter with integrated FETs and DVFS for a small, simple system.

Sequenced power supply architectures are becoming commonplace in high-performance microprocessor and digital signal processor (DSP) systems. To save power and increase processing speeds, processor cores have small-geometry cells that require lower supply voltages than the system-bus voltages. Power management in these systems requires special attention. This application note addresses these topics and suggests solutions for output-voltage sequencing.

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1 Introduction

In dual-voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power-up and power-down operations.

Sequencing refers to the order, timing and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long term reliability of the dual-voltage device, while the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data-converter ICs.

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Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bi-directional bus during power up. Bus contention may also affect I/O reliability. Power supply designers should check the requirements regarding bus contention for individual devices.

The power-on sequencing for the OMAP-L138, TMS320C6742, TMS320C6746, and TMS320C6748 are shown in the Power Requirements table below. There is no specific required voltage ramp rate for any of the supplies as long as the 3.3V rail never exceeds the 1.8V rail by more than 2V.

Also, in order to reduce the power consumption of the processor core, the Dynamic Voltage and Frequency Scaling (DVFS) is used in the reference design. DVFS is a power management technique used while the system-on-chip (SoC) is actively processing. This technique matches the operating frequency of the hardware to the performance requirement of the active application scenario. Whenever clock frequencies are lowered, operating voltages are also lowered as well to achieve power savings. In the reference design, the TPS65023 is used that can scale its output voltage. It supports all five DVFS voltage values (0.95V, 1V, 1.2V, 1.27V, and 1.35V) defined for VDD_MPU.

2 Power Requirements

The power requirements are as specify in the table.

	PIN NAME	VOLTAGE [(1)] [(2)] (V)	Imax (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY
I/O	RTC_CVDD	1.2	1	–25%, +10%	1[(3)]	
Core	CVDD[(4)]	1.0 / 1.1 / 1.2	600	–9.75%, +10%	2	
I/O	RVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2	200	–5%, +10%	3	
I/O	USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8	180	±5%	4	
I/O	USB0_VDDA33, USB1_VDDA33	3.3	24	±5%	5	
I/O	DVDD3318_A, DVDD3318_B, DVDD3318_C	1.8 / 3.3	50 / 90[(5)]	±5%	4 / 5	

(1) If 1.8-V LVCMOS is used, power rails up with the 1.8-V rails. If 3.3-V LVCMOS is used, power it up with the ANALOG33 rails (VDDA33_USB0/1)

(2) There is no specific required voltage ramp rate for any of the supplies LVCMOS33 (USB0_VDDA33, USB1_VDDA33) never exceeds STATIC18 (USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18) by more than 2 V.

(3) If RTC is not used/maintained on a separate supply, it can be included in the STATIC12 (fixed 1.2 V) group.

(4) If using CVDD at fixed 1.2 V, all 1.2-V rails may be combined.

(5) If DVDD3318_A, B, and C are powered independently, maximum power for each rail will be 1/3 the above maximum power.

3 Features

The design uses the following high-efficiency DC/DC Converter with integrated FETs .

INPUT VOLTAGE	**~5V**
	HIGH EFFICIENCY AND INTEGRATION (w DVFS)
COMBINE RTC AND STATIC 1.2	
Core 1.2 V at 600 mA	TPS65023
Static 1.2 V + VRTC at 251 mA	
Static 1.8 V at 230 mA	
Static 3.3 V at 115 mA	

Here, VRTC is included in the STATIC12 (fixed 1.2 V) group.

TPS65023

- 1.5-A, 90% Efficient Step-Down Converter for Processor Core (VDCDC1)
- 2 × 200-mA General-Purpose LDO
- 1.2-A, Up to 95% Efficient Step-Down Converter for System Voltage (VDCDC2)
- 1-A, 92% Efficient Step-Down Converter for Memory Voltage (VDCDC3)
- Dynamic Voltage Management for Processor Core
- I^2C™ Compatible Serial Interface

More information on the device can be found from the data sheets

- TPS65023, http://focus.ti.com/lit/ds/symlink/tps65023.pdf

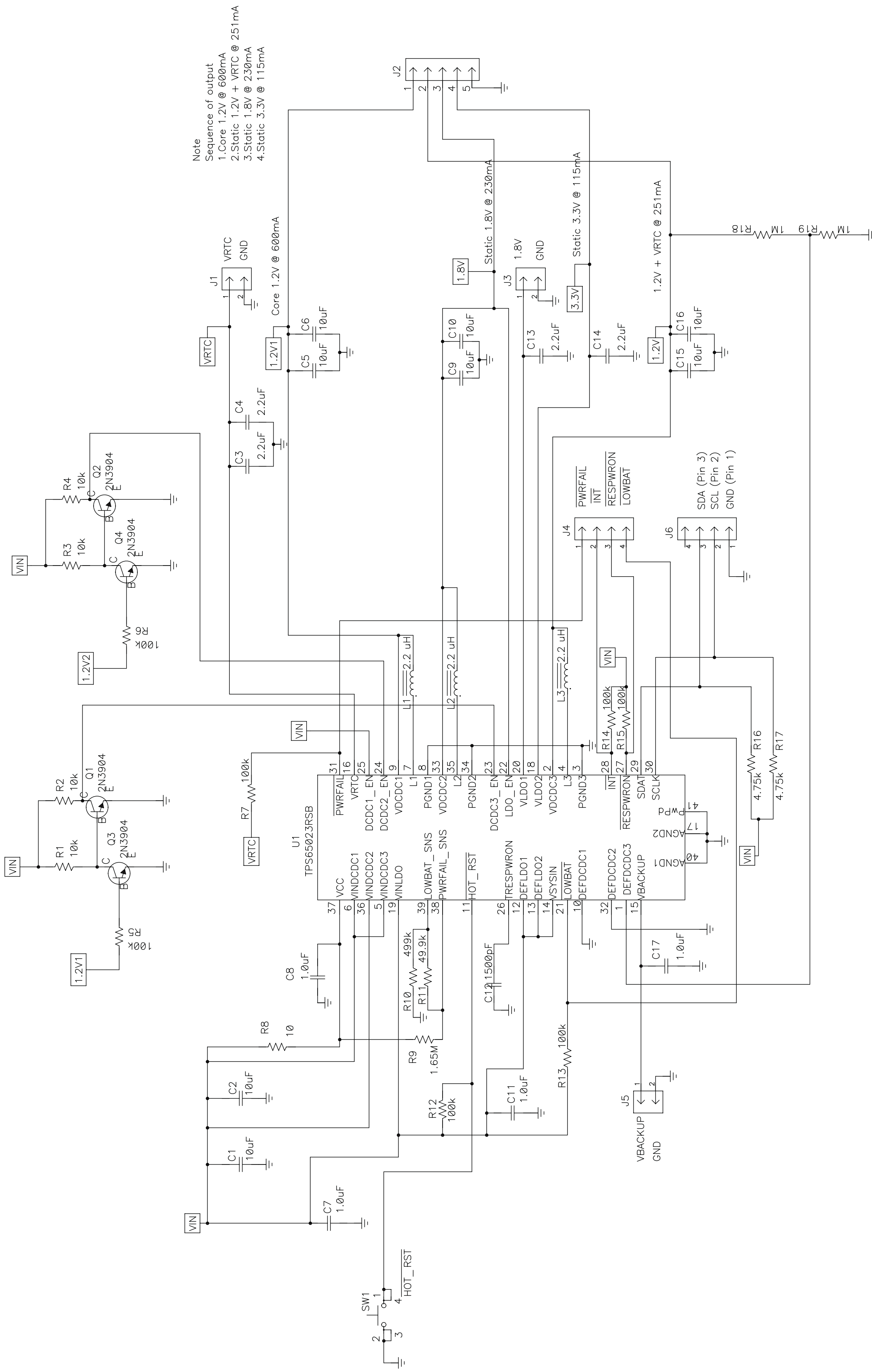
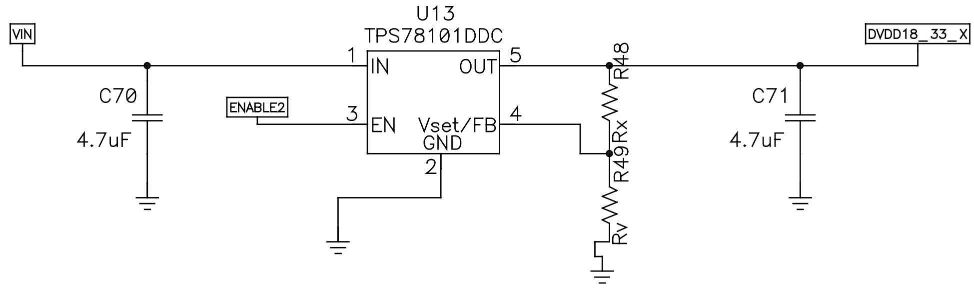


Figure 1. PMP4977 Reference Design Schematic

Proper sequencing is ensured in the design with the use of simple circuits involving the use of NPN transistors as required. Core 1.2 V at 600 mA comes first ,which in turn is level-shifted to input voltage using NPN transistors to enable the DCDC3_EN ; hence, static 1.2 V + VRTC at 251 mA comes up which also enable the DCDC2_EN and sequentially static 1.8 V at 230 mA comes up. This 1.8-V output from DCDC2 converter enable the LDO and hence at last static 3.3 V at 115 mA comes up.



(1) Use three such LDOs to power up DVDDA, DVDDB, and DVDDC. (It can either be 1.8 V or 3.3 V.)

(2) Rx = 0.499 MΩ, Ry = 1 MΩ for Vout = 1.8 V

(3) Rx = 1.8 MΩ, Ry = 1 MΩ for Vout = 3.3 V

(4) For proper sequencing of output, enable of the LDOs are fed either from 1.2-V output from DCDC3 converter if DVDDX is 1.8 V or from 1.8-V output from DCDC2 converter if DVDDX is 3.3 V.

Figure 2. Optional circuit for DVDD_A, DVDD_B and DVDD_C

4 List of Material

Table 1. PMP4977 List of Material

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
8	C1	10 μF	Capacitor, Ceramic, 6.3V, X5R, 10%	805	C2012X5R0J106K	TDK	10560
	C2	10 μF	Capacitor, Ceramic, 6.3V, X5R, 10%	805	C2012X5R0J106K	TDK	10560
2	C3	2.2 F	Capacitor, Ceramic, 6.3V, X5R, 10%	603	C1608X5R0J225K	TDK	5650
	C4	2.2 F	Capacitor, Ceramic, 6.3V, X5R, 10%	603	C1608X5R0J225K	TDK	5650
	C5	10 F	Capacitor, Ceramic, 6.3V, X5R, 10%	805	C2012X5R0J106K	TDK	10560
	C6	10 F	Capacitor, Ceramic, 6.3V, X5R, 10%	805	C2012X5R0J106K	TDK	10560
4	C7	1.0 F	Capacitor, Ceramic, 6.3V, X5R,10%	603	C1608X5R0J105K	TDK	5650
	C8	1.0 F	Capacitor, Ceramic, 6.3V, X5R,10%	603	C1608X5R0J105K	TDK	5650
	C9	10 F	Capacitor, Ceramic, 6.3V, X5R, 10%	805	C2012X5R0J106K	TDK	10560
	C10	10 F	Capacitor, Ceramic, 6.3V, X5R, 10%	805	C2012X5R0J106K	TDK	10560
	C11	1.0 F	Capacitor, Ceramic, 6.3V, X5R,10%	603	C1608X5R0J105K	TDK	5650
1	C12	1500 pF	Capacitor, Ceramic, 50V, X7R, 10%	603	C1608X7R1H152K	TDK	5650
2	C13	2.2 F	Capacitor, Ceramic, 6.3V, X5R,10%	603	C1608X5R0J225K	TDK	5650
	C14	2.2 F	Capacitor, Ceramic, 6.3V, X5R,10%	603	C1608X5R0J225K	TDK	5650
	C15	10 F	Capacitor, Ceramic, 6.3V, X5R, 10%	805	C2012X5R0J106K	TDK	10560
	C16	10 F	Capacitor, Ceramic, 6.3V, X5R, 10%	805	C2012X5R0J106K	TDK	10560
	C17	1.0 F	Capacitor, Ceramic, 6.3V, X5R,10%	603	C1608X5R0J105K	TDK	5650
3	J1	PTC36SAAN	Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins	23100
1	J2	PEC36SAAN	Header, Male 5-pin, 100mil spacing, (36-pin strip)	0.100 inch x 5	PEC36SAAN	Sullins	60000
	J3	PTC36SAAN	Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins	23100
1	J4	PTC36SAAN	Header, 4 pin, 100mil spacing, (36-pin strip)	0.100 x 4	PTC36SAAN	Sullins	45100
	J5	PTC36SAAN	Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins	23100
1	J6	22-05-3041	Header, Friction Lock Ass'y, 4 pin Right Angle	0.400 x 0.500	22-05-3041	Molex	227,900
2	L1	2.2 μH	Inductor, SMT, 1.72A, 59 mΩ	0.157 x 0.157 inch	VLCF4020T-2R2N1R7	TDK	36.8
	L2	2.2 μH	Inductor, SMT, 1.72A, 59 mΩ	0.157 x 0.157 inch	VLCF4020T-2R2N1R7	TDK	36.8

Table 1. PMP4977 List of Material (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
1	L3	2.2 μH	Inductor, SMT, 1.5A, 87 mΩ	0.137 X 0.147 inch	VLF4012AT-2R2M1R5	TDK	29320
4	Q1	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
	Q2	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
	Q3	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
	Q4	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
4	R1	10k	Resistor, Chip, 1/16W, 1%	603	CRCW0603-xxxx-F	Vishay	9100
	R2	10k	Resistor, Chip, 1/16W, 1%	603	CRCW0603-xxxx-F	Vishay	9100
	R3	10k	Resistor, Chip, 1/16W, 1%	603	CRCW0603-xxxx-F	Vishay	9100
	R4	10k	Resistor, Chip, 1/16W, 1%	603	CRCW0603-xxxx-F	Vishay	9100
2	R5	100k	Resistor, Chip, 1/16W, 1%	603	CRCW0603-xxxx-F	Vishay	9100
	R6	100k	Resistor, Chip, 1/16W, 1%	603	CRCW0603-xxxx-F	Vishay	9100
5	R7	100k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
1	R8	10	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
1	R9	1.65M	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
1	R10	499k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
1	R11	49.9k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
	R12	100k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
	R13	100k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
	R14	100k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
	R15	100k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
2	R16	4.75k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
	R17	4.75k	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
2	R18	1M	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
	R19	1M	Resistor, Chip, 1/16W, 1%	603	Std	Std	9100
1	SW1	KT11P2JM	Switch, SPST, PB Momentary, Sealed Washable	0.245 X 0.251	KT11P2JM	C & K	111,600
1	U1	TPS65023RSB	IC, Power Management IC for Li-Ion Powered Systems	QFN	TPS65023RSB	TI	69696

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.1 Test Results

The start-up waveform shown in Figure 3 specifies the required sequence.

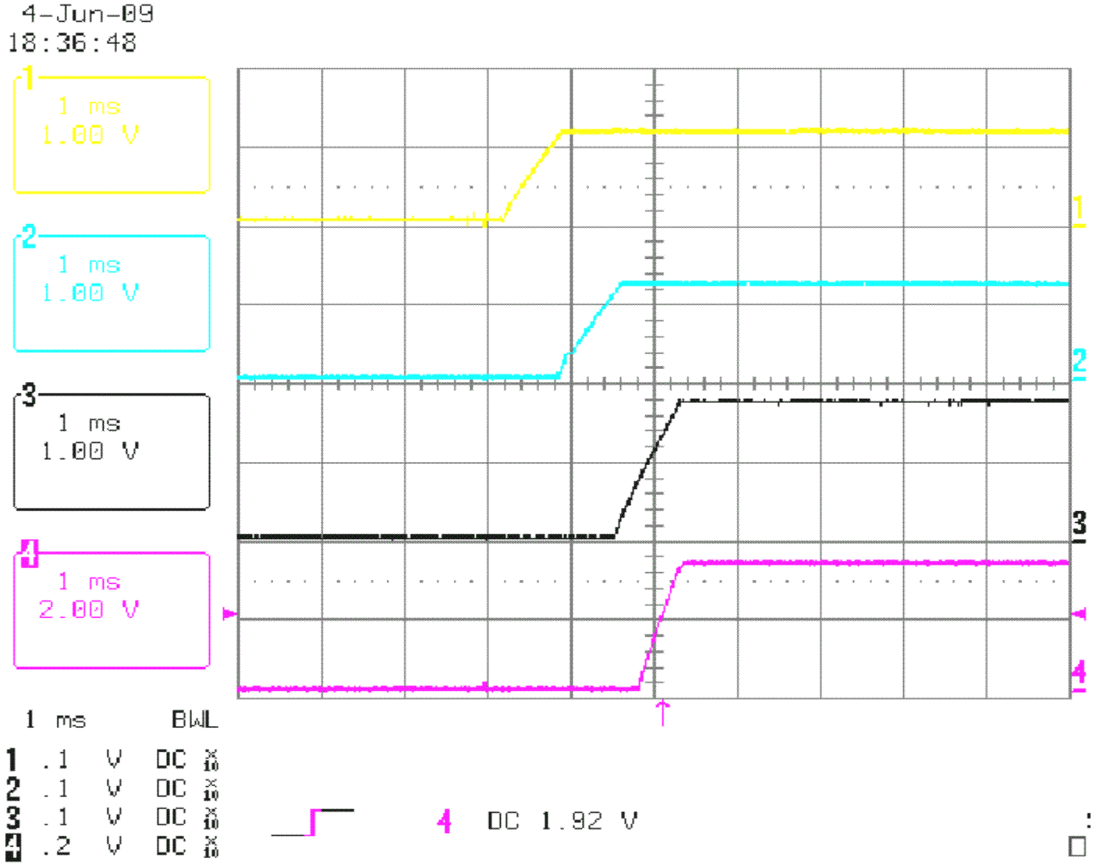


Figure 3. Shows Sequencing in Start-Up Waveform

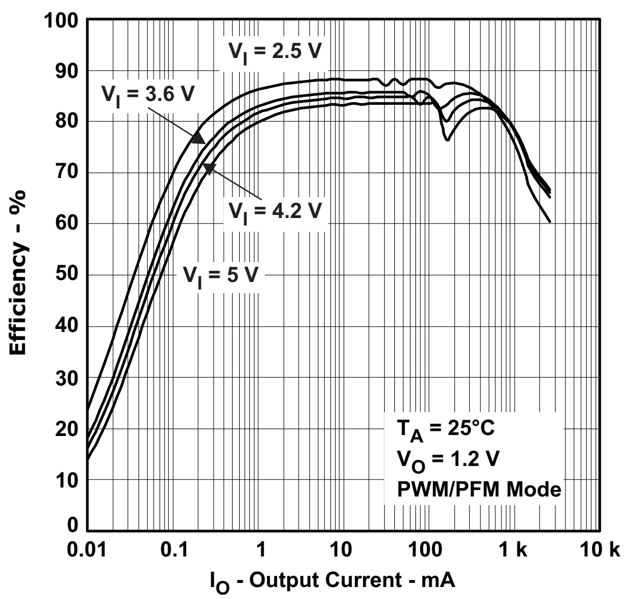


Figure 4. DCDC1: Efficiency vs Output Current

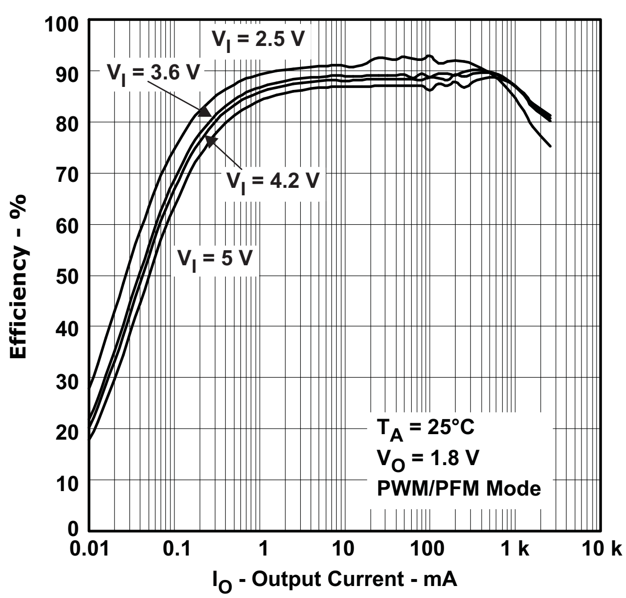


Figure 5. DCDC2: Efficiency vs Output Current

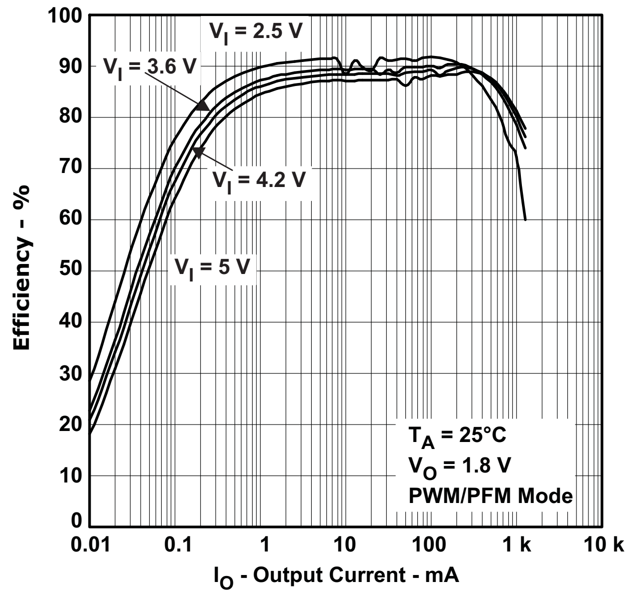


Figure 6. DCDC3: Efficiency vs Output Current

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