Input to Output Isolation for the TPS61170

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ABSTRACT

Many boost converters have an external rectifier diode. The input voltage of the TPS61170 main boost converter is connected to the output voltage when the device is disabled. Due to the direct pass from the input to the output, the input supply is not isolated from the output voltage when the IC is disabled. This application report describes how to use a PMOS transistor to disconnect the boost converter's input voltage from the output voltage (known as load disconnect or input to output isolation) when the device is disabled.

Figure 1 shows the schematic for a TPS61170EVM (SLVU222) that has been modified to include a PMOS transistor $Q_{(LD)}$, and a resistor $R_{(LD)}$ which form the load disconnect circuit. Capacitor C4 is the minimum capacitor necessary for control loop stability, and C5 represents additional load capacitance.
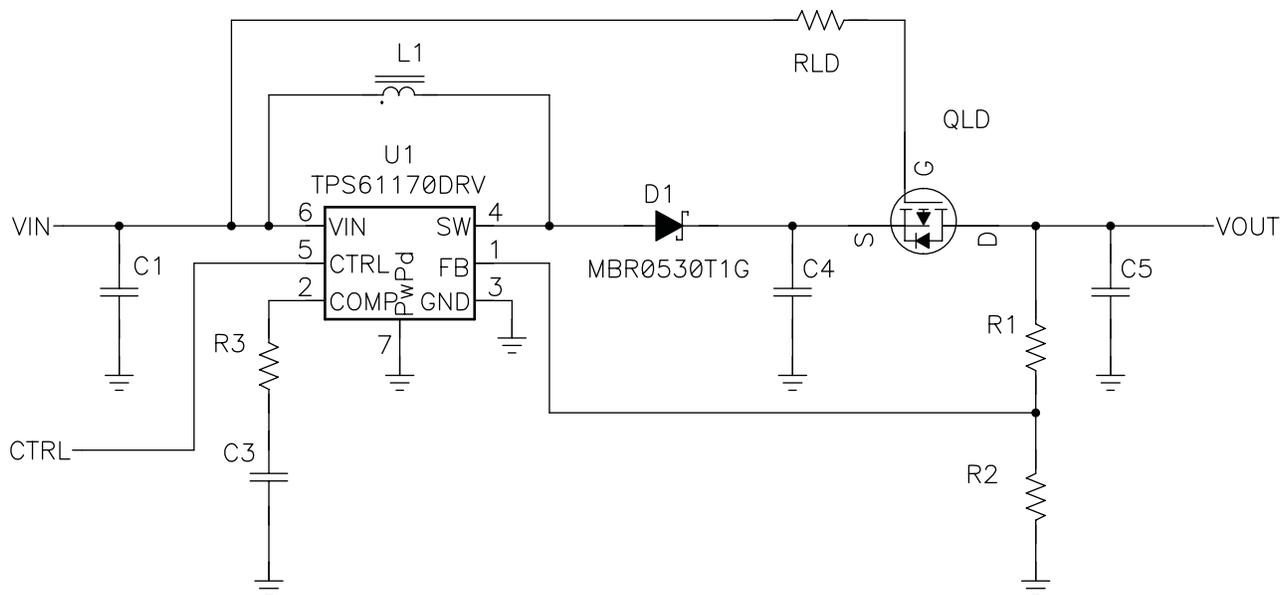

Figure 1. TPS61170 with Input to Output Isolation

The boost converter's diode is connected to the source of $Q_{(LD)}$, but the feedback network and output capacitor are connected after $Q_{(LD)}$. This allows a regulated output voltage even with the use of the transistor $Q_{(LD)}$. Select $Q_{(LD)}$ to have the following characteristics:

1. a V_{SD} breakdown voltage higher than V_{OUT}
2. a V_{GS} breakdown voltage higher than $V_{OUT} - V_{IN}$min
3. a low drain to source resistance ($R_{DS(on)}$) such that the voltage drop created by the maximum output current ($I_O$max) times $R_{DS(on)}$ does not take the output voltage below the required minimum regulated voltage for the application.

Capacitor C4 provides a defined bias operation point for $Q_{(LD)}$ and can should be in the 0.1uF to 1uF range. $R_{(LD)}$of approximately 100 Ω is recommended to prevent the input voltage from capacitively coupling to the boost converter output. UsingFigure 1 with V_{IN} = 5V and V_{OUT} set to 24 V by R1 and R2, and R_{LOAD} = 240 Ω (I_{OUT} = 100 mA), Figure 2 shows the circuit starting up while Figure 3 shows the circuit at shutdown. In both figures, CH1 shown in yellow and set to 5 V/div, shows output voltage before $Q_{(LD)}$, CH2 shown in pink and set to 5 V/div, shows the output voltage after $Q_{(LD)}$, and CH3 shown in blue, shows CTRL.
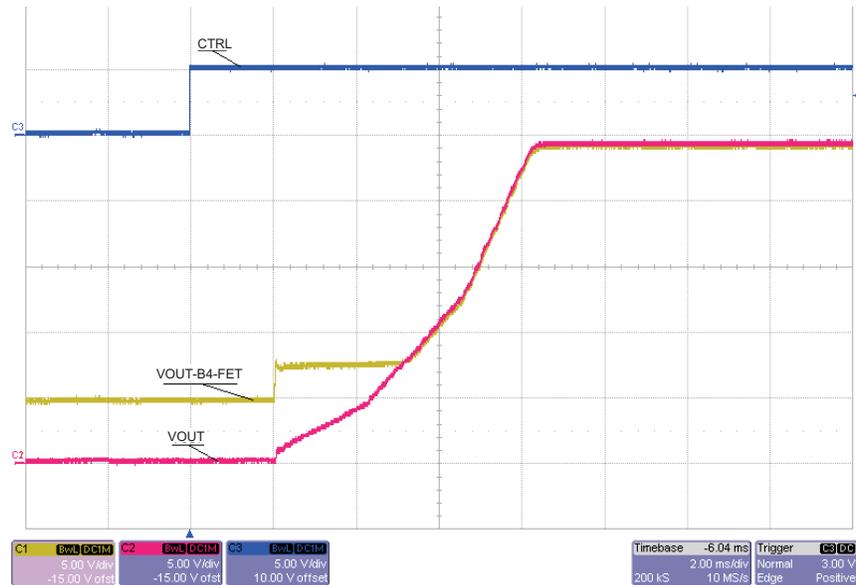
Figure 2. TPS61170 with Input to Output Isolation at Startup
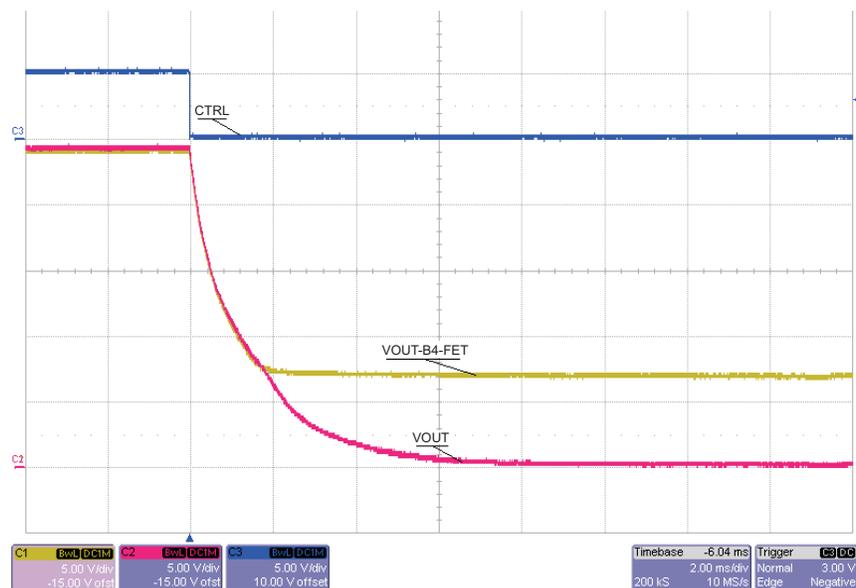
Figure 3. TPS61170 with Input to Output Isolation at Shutdown

Note that the load regulation at large loads is degraded by the $I_{OUT} \times R_{DS(on)}$ drop across the FET, i.e.,

$V_{OUT} = V_{REF} \times (1 + R1/R2) - I_{OUT} \times R_{DS(on)}$.

Note also that efficiency will be degraded slightly due to the $I_{OUT}^2 \times R_{DS(on)}$ additional power loss across the FET, i.e. $\eta = ((V_{REF} \times (1 + R1/R2) - I_{OUT} \times R_{DS(on)}) \times I_{OUT})/(V_{IN} \times I_{IN})$. In this example, the Si2343 -30-V PFET with $R_{DS(on)}$= 45 mΩ at V_{GS} = 10V was used. So, with V_{IN} = 12V, the change in load regulation and efficiency is negligible. At lower input voltages, higher currents, or when using FETs with higher $R_{DS(on)}$, the degradation in load regulation and efficiency is more apparent.

IMPORTANT NOTICE